KAE-04471

2096 (H) x 2096 (V) Interline Transfer EMCCD Image Sensor

ON Semiconductor®

www.onsemi.com

The KAE−04471 Image Sensor is a 4.4 Mp, 4/3″ format, Interline Transfer EMCCD image sensor that provides exceptional imaging performance in extreme low light applications. Each of the sensor's four outputs incorporates both a conventional horizontal CCD register and a high gain EMCCD register.

An intra-scene switchable gain feature samples each charge packet on a pixel-by-pixel basis. This enables the camera system to determine whether the charge will be routed through the normal gain output or the EMCCD output based on a user selectable threshold. This feature enables imaging in extreme low light, even when bright objects are within a dark scene, allowing a single camera to capture quality images from sunlight to starlight.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Interline CCD; with EMCCD
Resolution	4.4 Megapixels
Total Number of Pixels	2168 (H) × 2144 (V)
Number of Effective Pixels	2120 (H) × 2120 (V)
Number of Active Pixels	2096 (H) × 2096 (V)
Pixel Size	7.4 μm (H) × 7.4 μm (V)
Active Image Size	15.51 mm (H) × 15.51 mm (V) 21.93 mm (Diagonal) 4/3″ Optical Format
Aspect Ratio	1:1
Number of Outputs	1, 2, or 4
Charge Capacity	40,000 electrons
Output Sensitivity Normal Gain, Intra-scene	33, 45 μV/e−
Quantum Efficiency Mono (500, 800 nm) / R,G,B	(50%, 12%) / 31%, 42%, 43%
Read Noise (20 MHz) Normal Mode (1× Gain) Intra-scene Mode (20× Gain)	< 10 electrons rms < 1 electron rms
Dark Current (−10°C) Photodiode, VCCD	< 0.1, 6 electrons/s
Dynamic Range Normal Mode (1× Gain) Intra-scene Mode (20× Gain)	72 dB 92 dB
Charge Transfer Efficiency	0.999999
Blooming Suppression	> 300 X
Smear	−110 dB
Image Lag	< 1 electron
Maximum Data Rate	40 MHz (HCCD, +20°C), 20 MHz (EMCCD)
Maximum Frame Rate	30 fps (40 MHz HCCD), 15 fps (20 MHz HCCD)
Power Consumption (Intra-scene, 15 fps)	1300 mW

NOTE: All Parameters are specified at T = −10°C unless otherwise noted.

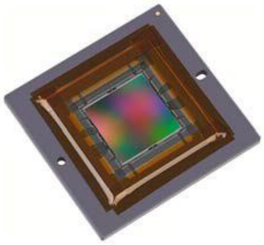


Figure 1. KAE−04471 Interline Transfer EMCCD Image Sensor

Features

- Intra-Scene Switchable Gain
- Wide Dynamic Range
- Low Noise Architecture
- Exceptional Low Light Imaging
- Global Shutter
- Excellent Image Uniformity and MTF
- Bayer Color Pattern and Monochrome

Applications

- Scientific Imaging
- Medical Imaging
- Defense Imaging
- Surveillance
- Intelligent Transportation Systems

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

US export controls apply to all shipments of this product designated for destinations outside of the US and Canada, requiring ON Semiconductor to obtain an export license from the US Department of Commerce before image sensors or evaluation kits can be exported.

Table 2. ORDERING INFORMATION − KAE−04471 IMAGE SENSOR

Part Number	Description	Marking Code
KAE−04471−ABA−JP−FA	Monochrome, Microlens, PGA Package, Taped Clear Cover Glass (No Coatings), Standard Grade	KAE−04471−ABA Serial Number
KAE−04471−ABA−JP−EE	Monochrome, Microlens, PGA Package, Taped Clear Cover Glass (No Coatings), Engineering Grade	
KAE−04471−FBA−JP−FA	Color (Bayer RGB), Microlens, PGA Package, Taped Clear Cover Glass (No Coatings), Standard Grade	KAE−04471−FBA Serial Number
KAE−04471−FBA−JP−EE	Color (Bayer RGB), Microlens, PGA Package, Taped Clear Cover Glass (No Coatings), Engineering Grade	

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

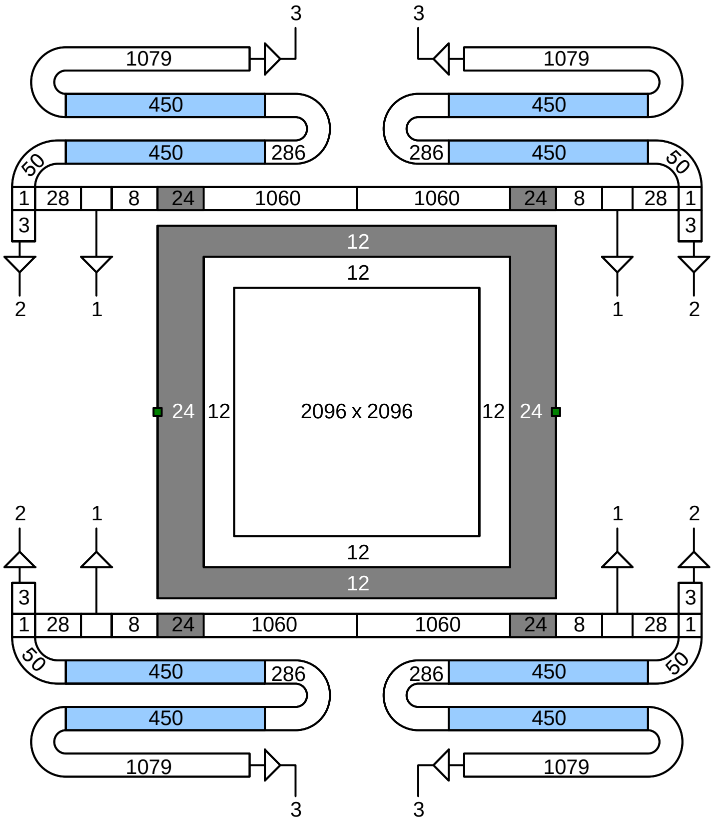


Figure 2. Block Diagram

Dark Reference Pixels

There are 12 dark reference rows at the top and bottom of the image sensor, as well as 24 dark reference columns on the left and right sides. However, the rows and columns at the perimeter edges should not be included in acquiring a dark reference signal, since they may be subject to some light leakage.

Active Buffer Pixels

12 unshielded pixels adjacent to any leading or trailing dark reference regions are classified as active buffer pixels. These pixels are light sensitive but are not tested for defects and non-uniformities.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photo-site. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time and non-linearly dependent on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

Physical Description

Pin Grid Array Configuration

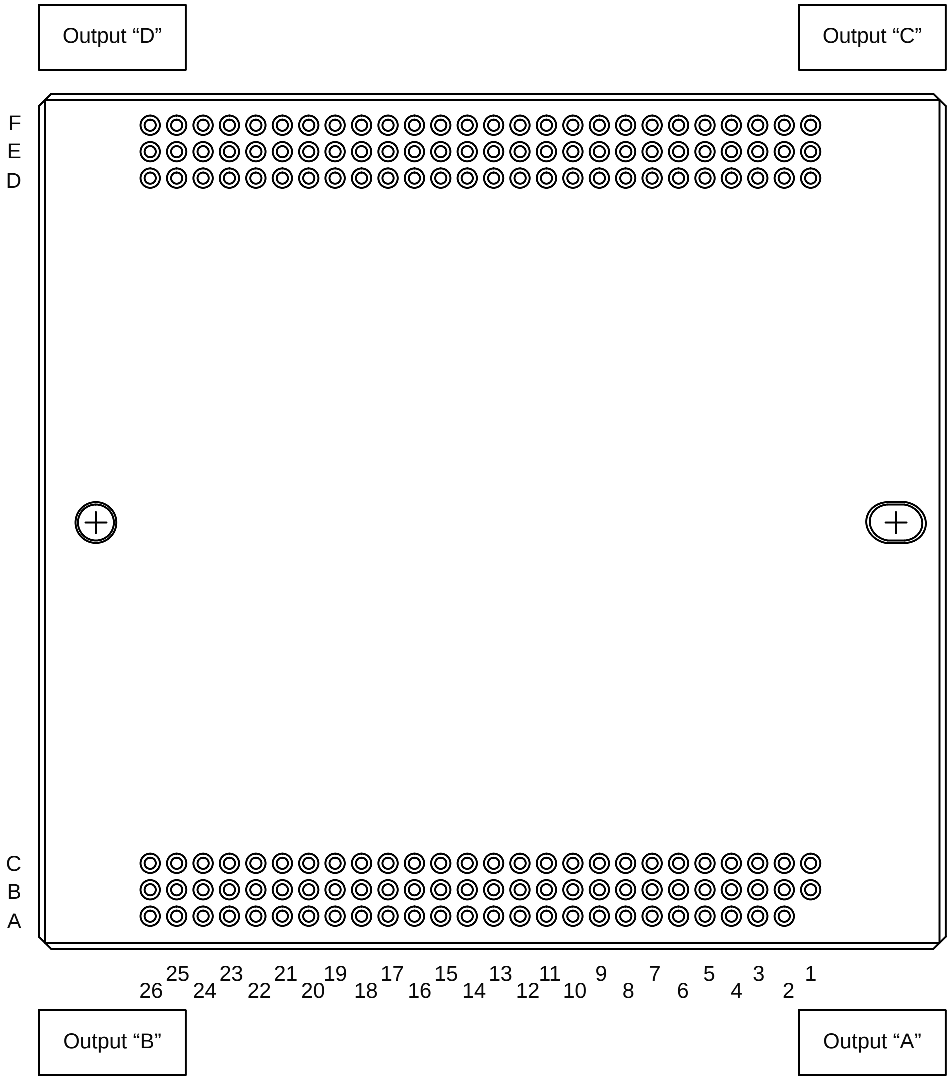


Figure 3. PGA Package Pin Designations (Bottom View)

Table 3. PIN DESCRIPTION

Pin No.	Label	Description
A7	VOUT2a	Video Output 2, Quadrant a
A13	GND	Ground
C7	H2SW2a	HCCD Output 2 Selector, Quadrant a
C8	H2SW3a	HCCD Output 3 Selector, Quadrant a
A8	H2La	HCCD Last Gate, Outputs 1, 2 and 3, Quadrant a
B7	RG23a	Amplifier 2 and 3 Reset, Quadrant a
A25	GND	Ground
A10	VOUT3a	Video Output 3, Quadrant a
A9	VDD3a	Amplifier 3 Supply, Quadrant a
C9	H2SEMa	EMCCD Storage Multiplier Phase 2, Quadrant a
C10	H1SEMa	EMCCD Storage Multiplier Phase 1, Quadrant a
B9	H2BEMa	EMCCD Barrier Phase 2, Quadrant a
B10	H1BEMa	EMCCD Barrier Phase 1, Quadrant a

Table 3. PIN DESCRIPTION (continued)

Pin No.	Label	Description
A11	H1a	HCCD Phase 1, Quadrant a
A12	H2a	HCCD Phase 2, Quadrant a
B4	GND	Ground
B11	H1Sa	HCCD Storage Phase 1, Quadrant a
B12	H2Sa	HCCD Storage Phase 2, Quadrant a
C11	H1Ba	HCCD Barrier Phase 1, Quadrant a
C12	H2Ba	HCCD Barrier Phase 2, Quadrant a
C13	SUB	Substrate
C15	H1Bb	HCCD Barrier Phase 1, Quadrant b
C14	H2Bb	HCCD Barrier Phase 2, Quadrant b
B14	H2Sb	HCCD Storage Phase 2, Quadrant b
B15	H1Sb	HCCD Storage Phase 1, Quadrant b
B8	GND	Ground
A14	H2b	HCCD Phase 2, Quadrant b
A15	H1b	HCCD Phase 1, Quadrant b
B16	H1BEMb	EMCCD Barrier Phase 1, Quadrant b
B17	H2BEMb	EMCCD Barrier Phase 2, Quadrant b
C16	H1SEMb	EMCCD Storage Multiplier Phase 1, Quadrant b
C17	H2SEMb	EMCCD Storage Multiplier Phase 2, Quadrant b
A17	VDD3b	Amplifier 3 Supply, Quadrant b
A16	VOUT3b	Video Output 3, Quadrant b
B13	GND	Ground
B19	RG23b	Amplifier 2 and 3 Reset, Quadrant b
A18	H2Lb	HCCD Last Gate, Outputs 1, 2 and 3, Quadrant b
C19	H2SW2b	HCCD Output 2 Selector, Quadrant b
C18	H2SW3b	HCCD Output 3 Selector, Quadrant b
B18	GND	Ground
A19	VOUT2b	Video Output 2, Quadrant b
A20	VDD2b	Amplifier 2 Supply, Quadrant b
C20	H2Xb	Floating Gate Exit HCCD Gate, Quadrant b
B20	RG1b	Amplifier 1 Reset, Quadrant b
B21	VSS1b	Amplifier 1 Return, Quadrant b
A21	VOUT1b	Amplifier 1 Output, Quadrant b
A22	VDD1b	Amplifier 1 Supply, Quadrant b
B22	GND	Ground
B23	V4B	VCCD Bottom Phase 4
C23	V3B	VCCD Bottom Phase 3
C22	V2B	VCCD Bottom Phase 2
C21	V1B	VCCD Bottom Phase 1
D24	VSUBREF	Substrate Voltage Reference
A23	VDD15bd	+15 V Supply, Quadrants b and d
B24	ESD	
A24	+9 V	+9 V Supply
E24	GND	Ground
F24	V2B	VCCD Bottom Phase 2
F23	ESD	
D21	V1T	VCCD Top Phase 1
D22	V2T	VCCD Top Phase 2
D23	V3T	VCCD Top Phase 3

Table 3. PIN DESCRIPTION (continued)

Pin No.	Label	Description
E23	V4T	VCCD Top Phase 4
E4	GND	Ground
F21	VOUT1d	Amplifier 1 Output, Quadrant d
F22	VDD1d	Amplifier 1 Supply, Quadrant d
E21	VSS1d	Amplifier 1 Return, Quadrant d
E20	RG1d	Amplifier 1 Reset, Quadrant d
D20	H2Xd	Floating Gate Exit HCCD Gate, Quadrant d
F20	VDD2d	Amplifier 2 Supply, Quadrant d
F19	VOUT2d	Video Output 2, Quadrant d
A6	VDD2a	Amplifier 2 Supply, Quadrant a
C6	H2Xa	Floating Gate Exit HCCD Gate, Quadrant a
B6	RG1a	Amplifier 1 Reset, Quadrant a
B5	VSS1a	Amplifier 1 Return, Quadrant a
A5	VOUT1a	Video Output 1, Quadrant a
A4	VDD1a	Amplifier 1 Supply, Quadrant a
E25	GND	Ground
F25	GND	Ground
B3	V4B	VCCD Bottom Phase 4
C3	V3B	VCCD Bottom Phase 3
C4	V2B	VCCD Bottom Phase 2
C5	V1B	VCCD Bottom Phase 1
B1	TD−	Temperature Sensor Negative Bias
C1	TD+	Temperature Sensor Positive Bias
C2	ID	Device ID
A3	VDD15ac	+15 V Supply
B2	ESD	
A2	+9 V	+9 V Supply
E1	N/C	No connect
E2	GND	Ground
F1	N/C	No connect
F2	V2B	VCCD Bottom Phase 2
F3	ESD	
E22	GND	Ground
D5	V1T	VCCD Top Phase 1
D4	V2T	VCCD Top Phase 2
D3	V3T	VCCD Top Phase 3
D2	N/C	No connect
D1	N/C	No connect
E3	V4T	VCCD Top Phase 4
B25	GND	Ground
F4	VDD1c	Amplifier 1 Supply, Quadrant c
F5	VOUT1c	Video Output 1, Quadrant c
E5	VSS1c	Amplifier 1 Return, Quadrant c
E6	RG1c	Amplifier 1 Reset, Quadrant c
D6	H2Xc	Floating Gate Exit HCCD Gate, Quadrant c
F6	VDD2c	Amplifier 2 Supply, Quadrant c
F7	VOUT2c	Video Output 2, Quadrant c
E18	GND	Ground
D8	H2SW3c	HCCD Output 3 Selector, Quadrant c

Table 3. PIN DESCRIPTION (continued)

Pin No.	Label	Description
D7	H2SW2c	HCCD Output 2 Selector, Quadrant c
F8	H2Lc	HCCD Last Gate, Outputs 1, 2 and 3, Quadrant c
E7	RG23c	Amplifier 2 and 3 Reset, Quadrant c
E13	GND	Ground
F10	VOUT3c	Video Output 3, Quadrant c
F9	VDD3c	Amplifier 3 Supply, Quadrant c
D9	H2SEMc	EMCCD Storage Phase 2, Quadrant c
D10	H1SEMc	EMCCD Storage Phase 1, Quadrant c
E9	H2BEMc	EMCCD Barrier Phase 2, Quadrant c
E10	H1BEMc	EMCCD Barrier Phase 1, Quadrant c
F11	H1c	HCCD Phase 1, Quadrant c
F12	H2c	HCCD Phase 2, Quadrant c
E8	GND	Ground
E11	H1Sc	HCCD Storage Phase 1, Quadrant c
E12	H2Sc	HCCD Storage Phase 2, Quadrant c
D11	H1Bc	HCCD Barrier Phase 1, Quadrant c
D12	H2Bc	HCCD Barrier Phase 2, Quadrant c
D13	SUB	Substrate
D14	H2Bd	HCCD Barrier Phase 2, Quadrant d
D15	H1Bd	HCCD Barrier Phase 1, Quadrant d
E14	H2Sd	HCCD Storage Phase 2, Quadrant d
E15	H1Sd	HCCD Storage Phase 1, Quadrant d
F13	GND	Ground
F14	H2d	HCCD Phase 2, Quadrant d
F15	H1d	HCCD Phase 1, Quadrant d
E16	H1BEMd	EMCCD Barrier Phase 1, Quadrant d
E17	H2BEMd	EMCCD Barrier Phase 2, Quadrant d
D16	H1SEMd	EMCCD Storage Multiplier Phase 1, Quadrant d
D17	H2SEMd	EMCCD Storage Multiplier Phase 2, Quadrant d
F17	VDD3d	Amplifier 3 Supply, Quadrant d
F16	VOUT3d	Video Output 3, Quadrant b
D25	GND	Ground
E19	RG23d	Amplifier 2 and 3 Reset, Quadrant d
F18	H2Ld	HCCD Last Gate, Outputs 1, 2 and 3, Quadrant d
D18	H2SW3d	HCCD Output 3 Selector, Quadrant d
D19	H2SW2d	HCCD Output 2 Selector, Quadrant d
C24	N/C	No connect
C25	GND	Ground
A26	N/C	No connect
B26	N/C	No connect
C26	N/C	No connect
D26	N/C	No connect
E26	N/C	No connect
F26	N/C	No connect

NOTE: For the 9 V bias on pins A2 and A24, the bias can be derived from the same supply as that for the V1 3rd level voltage using a voltage divider. The current load will be less than 10 μA.

Imaging Performance

Table 4. TYPICAL OPERATION CONDITIONS

(Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.)

Description	Condition
Light Source (Note 1)	Continuous Red, Green and Blue LED Illumination
Operation	Nominal Operating Voltages and Timing

1. For monochrome sensor, only green LED light source is used.

Table 5. SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Unit	Sampling Plan	Test Temperature (°C)
Dark Field Global Non-Uniformity	DSNU	–	–	2.0	mVpp	Die	−10
Bright Field Global Non-Uniformity (Note 2)		–	2.0	5.0	%rms	Die	−10
Bright Field Global Peak to Peak Non-Uniformity (Note 2)	PRNU	–	5.0	15.0	%pp	Die	−10
Bright Field Center Non-Uniformity (Note 2)		–	1.0	2.0	%rms	Die	−10
Maximum Photoresponse Nonlinearity (EMCCD gain = 1) (Note 3)	NL	–	2	–	%	Design	
Maximum Gain Difference Between Outputs (EMCCD gain = 1) (Note 8)	ΔG	–	10	–	%	Design	
Maximum Signal Error due to Nonlinearity Differences (EMCCD gain = 1) (Note 3)	ΔNL	–	1	–	%	Design	
Horizontal CCD Charge Capacity	H_{Ne}	–	50	–	ke^{-}	Design	
Vertical CCD Charge Capacity	V_{Ne}	–	50	–	ke^{-}	Design	
Photodiode Charge Capacity (Note 4)	P_{Ne}	–	40	–	ke^{-}	Die	−10
Horizontal CCD Charge Transfer Efficiency	HCTE	0.999995	0.999999	–		Die	−10
Vertical CCD Charge Transfer Efficiency	VCTE	0.999995	0.999999	–		Die	−10
Photodiode Dark Current (Average)	I_{PD}	–	0.1	3	e/p/s	Die	−10
Vertical CCD Dark Current		–	0.4	–	e/p/s	Die	−10
Image Lag	Lag	–	–	10	e−	Design	
Antiblooming Factor	X_{AB}	300	1000	–		Design	
Vertical Smear (Blue Light)	Smr	–	−100	–	dB	Design	
Read Noise (EMCCD Gain = 1) (Note 5)	n_{e-T}	–	9	–	e−rms	Design	
Read Noise (EMCCD Gain = 20)		–	< 1	–	e−rms		
EMCCD Excess Noise Factor (Gain = 20x)		–	1.4	–		Design	0
Dynamic Range (Gain = 1) (Notes 5, 6)	DR	–	72	–	dB	Design	
Dynamic Range (High Gain)		–	60	–	dB		
Dynamic Range (Intra-scene)		–	92	–	dB		
Output Amplifier DC Offset (VOUT2, VOUT3)	V_{ODC}	8.0	10	12.0	V	Die	−10
Output Amplifier DC Offset (VOUT1)	V_{ODC}	−0.5	1.0	2.5	V	Die	−10

Table 5. SPECIFICATIONS (continued)

Description	Symbol	Min.	Nom.	Max.	Unit	Sampling Plan	Test Temperature (°C)
Output Amplifier Bandwidth (Note 7)	f_{-3db}	−	250	−	MHz	Die	
Output Amplifier Impedance	R_{OUT}	−	140	−	Ω	Die	−10
Output Amplifier Sensitivity (EMCCD Output)	ΔV/ΔN	−	45	−	μV/e−	Design	
Output Amplifier Sensitivity (Floating Gate Amplifier)	ΔV/ΔN (FG)	−	7.8	−	μV/e−	Design	
Quantum Efficiency (Peak) Monochrome Red Green Blue	QE_{max}	 − − − −	 50% 31% 42% 43%	 − − − −	%	Design	
Power 4-output Mode (20MHz) (40MHz) 2-output Mode (20MHz) (40MHz) 1-output Mode (20MHz) (40MHz)		 − − − − − −	 0.8 0.7 0.5 0.5 0.4 0.4	 − − − − − −	W	Design	

2. Per color
3. Value is over the range of 10% to 90% of photodiode saturation.
4. The operating value of the substrate reference voltage, V_{AB}, can be read from V_{SUBREF}.
5. At 20 MHz.
6. Uses 20 LOG (P_{Ne}/n_{e-T})
7. Calculated from $f_{-3db} = 1 / 2\pi * R_{OUT} * C_{LOAD}$ where $C_{LOAD} = 5$ pF.
8. The output-to-output gain differences may be adjusted by independently adjusting the EMCCD amplitude for each output.

TYPICAL PERFORMANCE CURVES

Quantum Efficiency

Monochrome and Color with Microlens

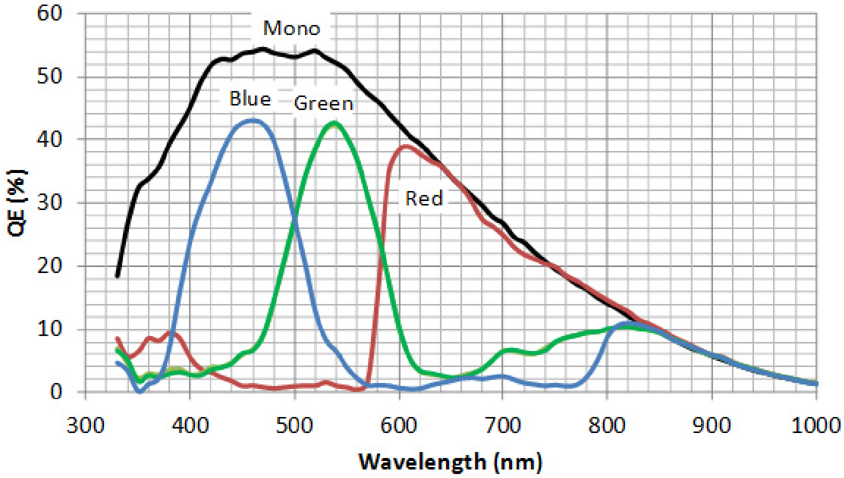


Figure 4. Monochrome and Color Quantum Efficiency

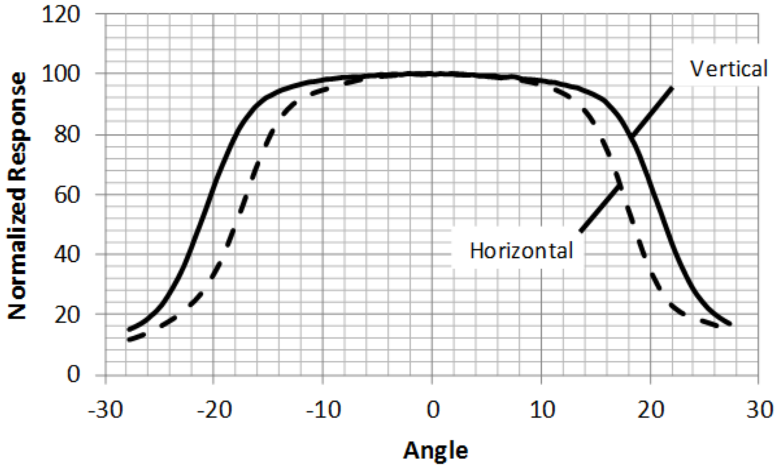


Figure 5. Angled Response for Monochrome Device

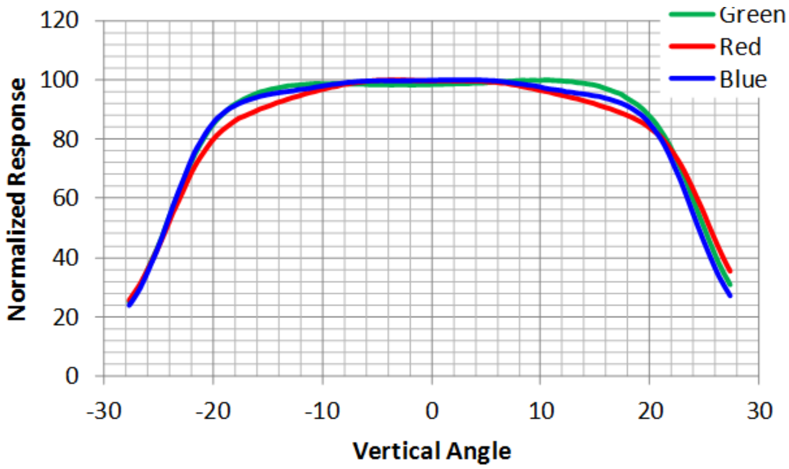


Figure 6. Vertical Angled Response for Color Device

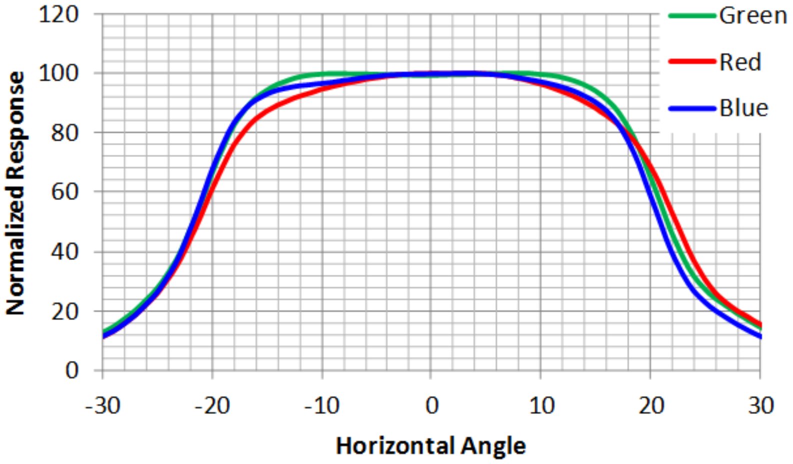


Figure 7. Horizontal Angled Response for Color Device

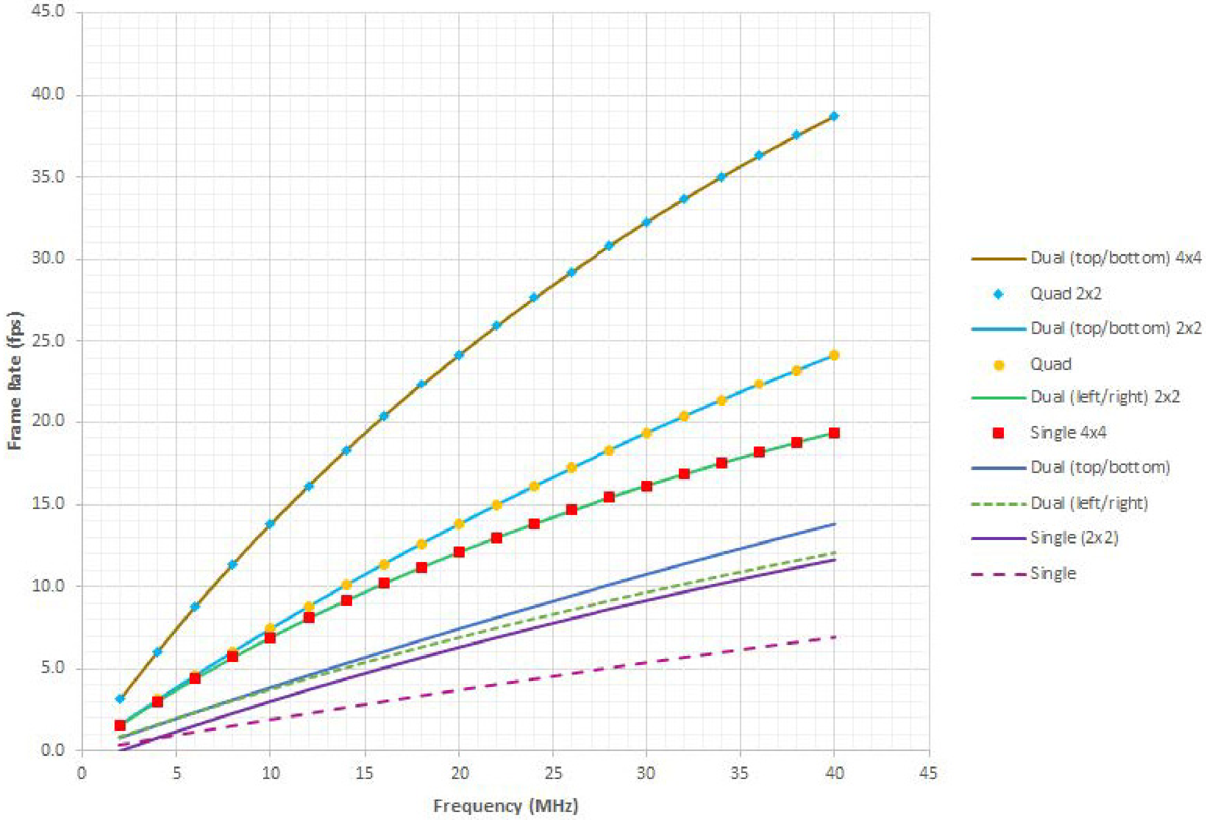


Figure 8. Frame Rates vs. Clock Frequency

DEFECT DEFINITIONS

Table 6. DEFECT DEFINITIONS

Description	Definition	Maximum Number Allowed
Major Dark Field Defective Bright Pixel	Defect ≥ 30 mV deviation from the mean, for all pixels in the active image area.	40
Major Bright Field Defective Dark Pixel	≥ 12%	
Minor Dark Field Defective Bright Pixel	Defect ≥ 15 mV deviation from the mean, for all pixels in the active image area.	400
Cluster Defect	A group of 2 to 10 contiguous major defective pixels, with no more than 2 adjacent defects horizontally.	8
Column Defect	A group of more than 10 contiguous major dark defective pixels along a single column or 10 contiguous bright defective pixels along a single column.	0

9. Low exposure dark column defects are not counted at temperatures above −10°C
10. For the color device, a bright field defective pixel deviates by 12% with respect to pixels of the same color.
11. Column and cluster defects are separated by no less than 2 good pixels in any direction (excluding single pixel defects).

OPERATION

Absolute Maximum Ratings

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged. Operation at these values will reduce MTTF.

Table 7. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Unit
Operating Temperature (Note 12)	T_{OP}	−30	+40	°C
Humidity (Note 13)	RH	+5	+90	%
Output Bias Current (Note 14)	I_{OUT}	−	60	mA
Off-chip Load	CL	−	10	pF

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

12. Noise performance will degrade at higher temperatures.
13. T = 25°C. Excessive humidity will degrade MTTF.
14. Total for all outputs. Maximum current is −15 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity).

Table 8. ABSOLUTE MAXIMUM VOLTAGE RATINGS BETWEEN PINS AND GROUND

Description	Minimum	Maximum	Unit
VDD2(a,b,c,d), VDD3(a,b,c,d)	−0.4	17.5	V
VOUT2(a,b,c,d), VOUT3(a,b,c,d)	−0.4	15	V
VDD1(a,b,c,d), VOUT1(a,b,c,d)	−0.4	7.0	V
V1B, V1T	ESD – 0.4	ESD + 22.0	V
V2B, V2T, V3B, V3T, V4B, V4T	ESD – 0.4	ESD + 14.0	V
H1(a,b,c,d), H2(a,b,c,d) H1S(a,b,c,d), H2S(a,b,c,d) H1B(a,b,c,d), H2B(a,b,c,d) H1BEM(a,b,c,d), H2BEM(a,b,c,d) H2SW2(a,b,c,d), H2SW3(a,b,c,d) H2L(a,b,c,d) H2X(a,b,c,d) RG1(a,b,c,d), RG23(a,b,c,d)	–0.4	+10	V
H1SEM(a,b,c,d), H2SEM(a,b,c,d)	−0.4	+20	V
ESD	−9.0	0.0	V
SUB (Notes 15 and 16)	6.5	40	V

15. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*
16. The measured value for VSUBREF is a diode drop higher than the recommended minimum VSUB bias.

Power Up and Power Down Sequence

SUB and ESD power up first, then power up all other biases in any order. No pin may have a voltage less than ESD at any time. All HCCD pins must be greater than or equal to GND at all times. The SUBREF pin will not become valid until VDD15ac and VDD15bd have been powered. The SUB pin should be at least 4 V before powering up VDD2(a,b,c,d) and VDD3(a,b,c,d).

Table 9. DC BIAS OPERATING CONDITIONS

Description	Pins	Symbol	Min.	Nom.	Max.	Unit	Maximum DC Current
Output Amplifier Return	VSS1(a,b,c,d)	VSS1	−8.3	−8.0	−7.7	V	4 mA
Output Amplifier Supply	VDD1(a,b,c,d)	VDD1	4.5	5.0	6.0	V	15 mA
Output Amplifier Supply	VDD2(a,b,c,d), VDD3(a,b,c,d)	VDD	+14.7	+15.0	+15.3	V	18.0 mA
Supply Voltage (Note 17)	VDD15ac, VDD15bd	VDD2, VDD3	+14.7	+15.0	+15.3	V	9 mA
Ground	GND	GND	0.0	0.0	0.0	V	17.0 mA
Substrate (Notes 18 and 19)	SUB	VSUB	6.0	VSUBREF − 0.5	VSUBREF + 28	V	Up to 1 mA (Determined by Photocurrent)
ESD Protection Disable	ESD	ESD	−8.3	−8.0	−7.7	V	2 mA
Output Bias Current	VOUT1(a,b,c,d), VOUT2(a,b,c,d), VOUT3(a,b,c,d)	I_{OUT}	2.0	2.5	5.0	mA	

17. VDD15ac and VDDD15bd bias pins must be maintained at 15 V during operation.
18. For each image sensor, the voltage output on the VSUBREF pin is programmed to be one diode drop, 0.5 V, above the nominal VSUB voltage. So, the applied VSUB should be one diode drop (0.5 V) lower than the VSUBREF value measured on the device, when VDD2(a,b,c,d) and VDD3(a,b,c,d) are at the specified voltage. This value corresponds to the VAB printed on the label for each sensor and applies to operation at 0°C. (For other temperatures, there is a temperature dependence of approximately 0.01 V/degree.) It is noted that VSUBREF is unique to each image sensor and may vary from 6.5 to 10.0 V. In addition, the output impedance of VSUBREF is approximately 100 k.
19. Caution: The EMCCD register must NOT be clocked while the electronic shutter pulse is high.

AC Operating Conditions

Clock Levels

Table 10. CLOCK LEVELS

Pin	Function	HCCD and RG					
		Low Level			Amplitude		
		Low	Nominal	High	Low	Nominal	High
H2B(a,b,c,d)	Reversible HCCD Barrier 2	−0.2	0.0	+0.2	3.1	3.3	3.6
H1B(a,b,c,d)	Reversible HCCD Barrier 1	−0.2	0.0	+0.2	3.1	3.3	3.6
H2S(a,b,c,d)	Reversible HCCD Storage 2	−0.2	0.0	+0.2	3.1	3.3	3.6
H1S(a,b,c,d)	Reversible HCCD Storage 1	−0.2	0.0	+0.2	3.1	3.3	3.6
H2SW2(a,b,c,d), H2SW3(a,b,c,d)	HCCD Switch 2 and 3	−0.2	0.0	+0.2	3.1	3.3	3.6
H2L(a,b,c,d)	HCCD Last Gate	−0.2	0.0	+0.2	3.1	3.3	3.6
H2X(a,b,c,d)	Floating Gate Exit	−0.2	0.0	+0.2	6.2	6.6	7.0
RG1(a,b,c,d)	Floating Gate Reset	Cap			3.1	3.3	3.6
RG23(a,b,c,d)	Floating Diffusion Reset	Cap			3.1	3.3	3.6
H1BEM(a,b,c,d)	Multiplier Barrier 1	−0.2	0.0	+0.2	4.6	5.0	5.4
H2BEM(a,b,c,d)	Multiplier Barrier 2	−0.2	0.0	+0.2	4.6	5.0	5.4
H1SEM(a,b,c,d)	Multiplier Storage 1	−0.3	0.0	+0.3	8.0	−	18.0
H2SEM(a,b,c,d)	Multiplier Storage 2	−0.3	0.0	+0.3	8.0	−	18.0

20. HCCD Operating Voltages. There can be no overshoot on any horizontal clock below −0.4 V: the specified absolute minimum. The H1SEM and H2SEM clock amplitudes need to be software programmable independently for each quadrant to adjust the charge multiplier gain.
21. Reset Clock Operation: The RG1, RG23 signals must be capacitive coupled into the image sensor with a 0.01 μF to 0.1 μF capacitor. The reset clock overshoot can be no greater than 0.3 V, as shown in Figure 9, below.

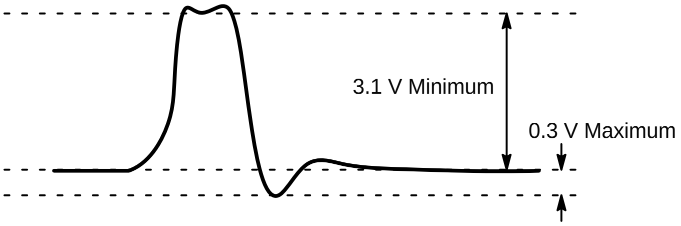


Figure 9. RG Clock Overshoot

Clock Capacitances

Pin	pF
H1SEMa	45
H2SEMa	45
H1BEMa	45
H2BEMa	45
H1a	65
H2a	65
H1Sa	75
H2Sa	75
H1Ba	75
H2Ba	75

Pin	pF
H1SEMb	45
H2SEMb	45
H1BEMb	45
H2BEMb	45
H1b	65
H2b	65
H1Sb	75
H2Sb	75
H1Bb	75
H2Bb	75

Pin	pF
H1SEMc	45
H2SEMc	45
H1BEMc	45
H2BEMc	45
H1c	65
H2c	65
H1Sc	75
H2Sc	75
H1Bc	75
H2Bc	75

Pin	pF
H1SEMd	45
H2SEMd	45
H1BEMd	45
H2BEMd	45
H1d	65
H2d	65
H1Sd	75
H2Sd	75
H1Bd	75
H2Bd	75

NOTE: The capacitances of all other HCCD pins is 15 pF or less.

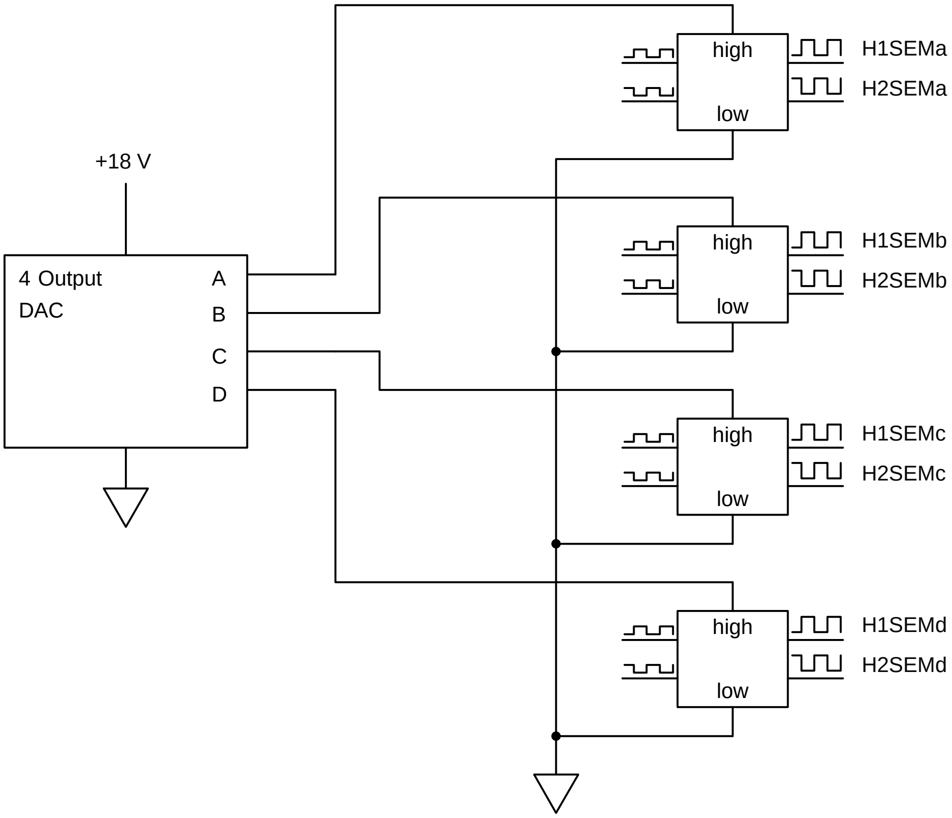


Figure 10. EMCCD Clock Adjustable Levels

For the EMCCD clocks, each quadrant must have independently adjustable high levels. All quadrants have a common low level of GND. The high level adjustments must be software controlled to balance the gain of the four outputs.

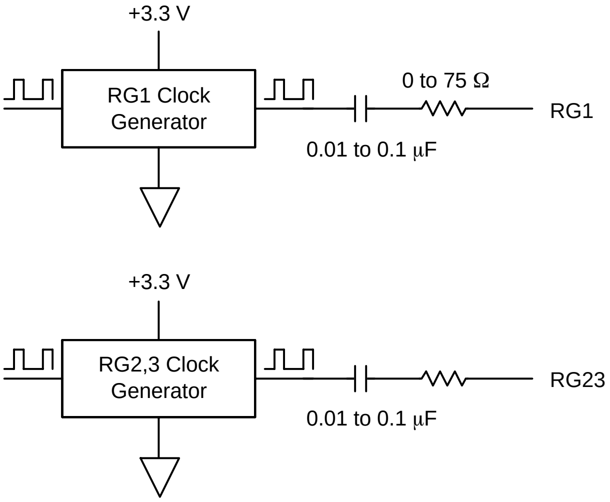


Figure 11. Reset Clock Drivers

The reset clock drivers must be coupled by capacitors to the image sensor. The capacitors can be anywhere in the range 0.01 to 0.1 μF. The damping resistor values would vary between 0 and 75 Ω depending on the layout of the circuit board.

Table 11. VCCD

Pin	Function	Low	Nominal	High
V1T, V1B, V2T, V2B, V3T, V3B, V4T, V4B	Vertical CCD Clock, Low Level	−8.0	−8.0	−6.0
V1T, V1B, V2T, V2B, V3T, V3B, V4T, V4B	Vertical CCD Clock, Mid Level	−0.2	0.0	+0.2
V1T, V1B	Vertical CCD Clock, High (3rd) Level	8.5	9.0	12.5

22. The Vertical CCD operating voltages. The VCCD low level will be −8.0 V for operating temperatures of −10°C and above. Below −10°C the VCCD low level should be increased for optimum noise performance.

Table 12. ELECTRONIC SHUTTER PULSE

Pin	Function	Low	High
SUB	Electronic Shutter	VSUBREF − 0.5	VSUBREF + 28

Device Identification

The device identification pin (DevID) may be used to determine which ON Semiconductor 5.5 micron pixel interline CCD sensor is being used.

Table 13. DEVICE IDENTIFICATION VALUES

Description	Pins	Symbol	Min.	Nom.	Max.	Unit	Maximum DC Current
Device Identification (Notes 23, 24 and 25)	ID	ID	63,000	70,000	84,000	Ω	0.3 mA

23. Nominal value subject to verification and/or change during release of preliminary specifications.
24. If the Device Identification is not used, it may be left disconnected.
25. After Device Identification resistance has been read during camera initialization, it is recommended that the circuit be disabled to prevent localized heating of the sensor due to current flow through the R_DeviceID resistor.

Recommended Circuit

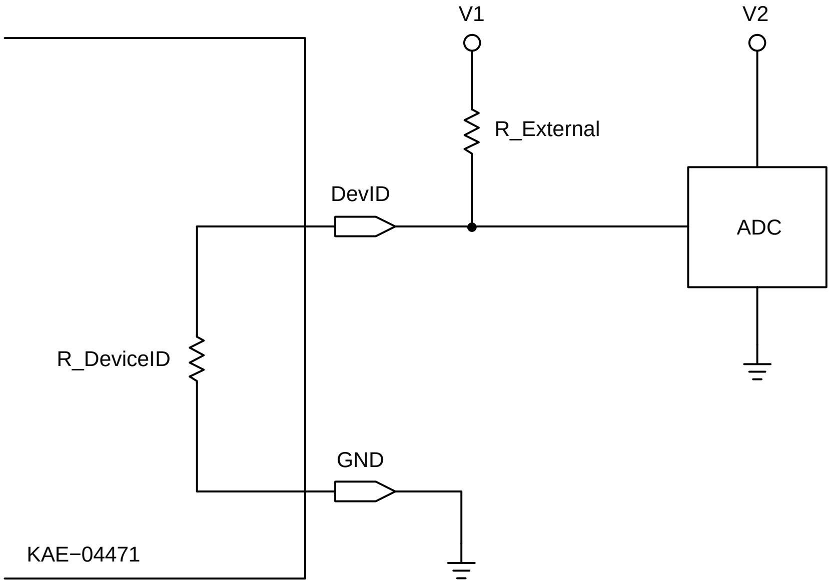


Figure 12. Device Identification Recommended Circuit

THEORY OF OPERATION

Image Acquisition

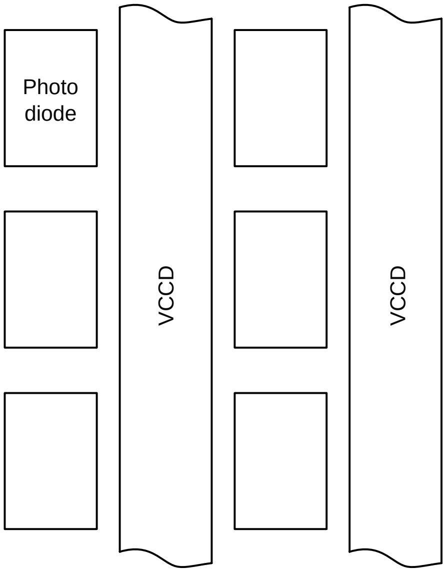


Figure 13. An Illustration of Two Columns and Three Rows of Pixels

This image sensor is capable of detecting up to 40,000 electrons with a small signal noise floor of 1 electron all within one image. Each 7.4 μm square pixel, as shown in Figure 13 above, consists of a light sensitive photodiode and a portion of the vertical CCD (VCCD). Not shown is a microlens positioned above each photodiode to focus light away from the VCCD and into the photodiode. Each photon incident upon a pixel will generate an electron in the photodiode with a probability equal to the quantum efficiency.

The photodiode may be cleared of electrons (electronic shutter) by pulsing the SUB pin of the image sensor up to a voltage of 30 V to 40 V (VSUBREF + 22 to VSUBREF + 28 V) for a time of at least 1 μs. When the SUB pin is above 30 V, the photodiode can hold no electrons, and the electrons flow downward into the substrate. When the voltage on SUB drops below 30 V, the integration of electrons in the photodiode begins. The HCCD clocks should be stopped when the electronic shutter is pulsed, to avoid having the large voltage pulse on SUB coupling into the video outputs and altering the EMCCD gain.

It should be noted that there are certain conditions under which the device will have no anti-blooming protection: when the V1T and V1B pins are high, very intense illumination generating electrons in the photodiode will flood directly into the VCCD. When the electronic shutter pulse overlaps the V1T and V1B high-level pulse that transfers electrons from the photodiode to the VCCD, then photo-electrons will flow to the substrate and not the VCCD. This condition may be desirable as a means to obtain very short integration times.

The VCCD is shielded from light by metal to prevent detection of more photons. For very bright spots of light, some photons may leak through or around the metal light shield and result in electrons being transferred into the VCCD. This is called image smear.

Image Readout

At the start of image readout, the voltage on the V1T and V1B pins is pulsed from 0 V up to the high level for at least 1 μs and back to 0 V, which transfers the electrons from the photodiodes into the VCCD. If the VCCD is not empty, then the electrons will be added to what is already in the VCCD. The VCCD is read out one row at a time. During a VCCD row transfer, the HCCD clocks are stopped. All gates of type H1 stop at the high level and all gates of type H2 stop at the low level. After a VCCD row transfer, charge packets of electrons are advanced one pixel at a time towards the output amplifiers by each complimentary clock cycle of the H1 and H2 gates.

The charge multiplier has a maximum charge handling capacity (after gain) of 20,000 electrons. This is not the average signal level. It is the maximum signal level. Therefore, it is advisable to keep the average signal level at 15,000 electrons or less to accommodate a normal distribution of signal levels. For a charge multiplier gain of 20x, no more than 15,000/20 = 750 electrons should be allowed to enter the charge multiplier. Overfilling the charge multiplier beyond 20,000 electrons will shorten its useful operating lifetime.

To prevent overfilling the charge multiplier, a non-destructive floating gate output amplifier (VOUT1) is provided on each quadrant of the image sensor as shown in Figure 14 below.

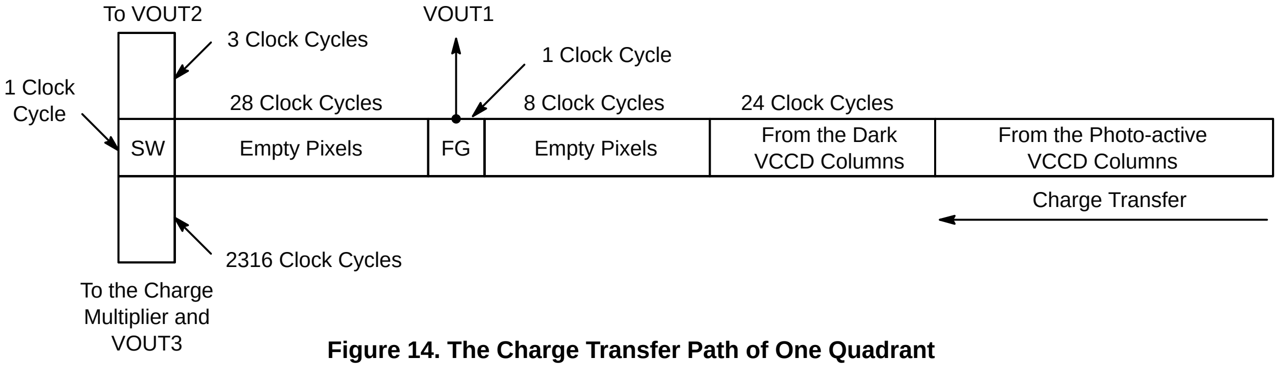
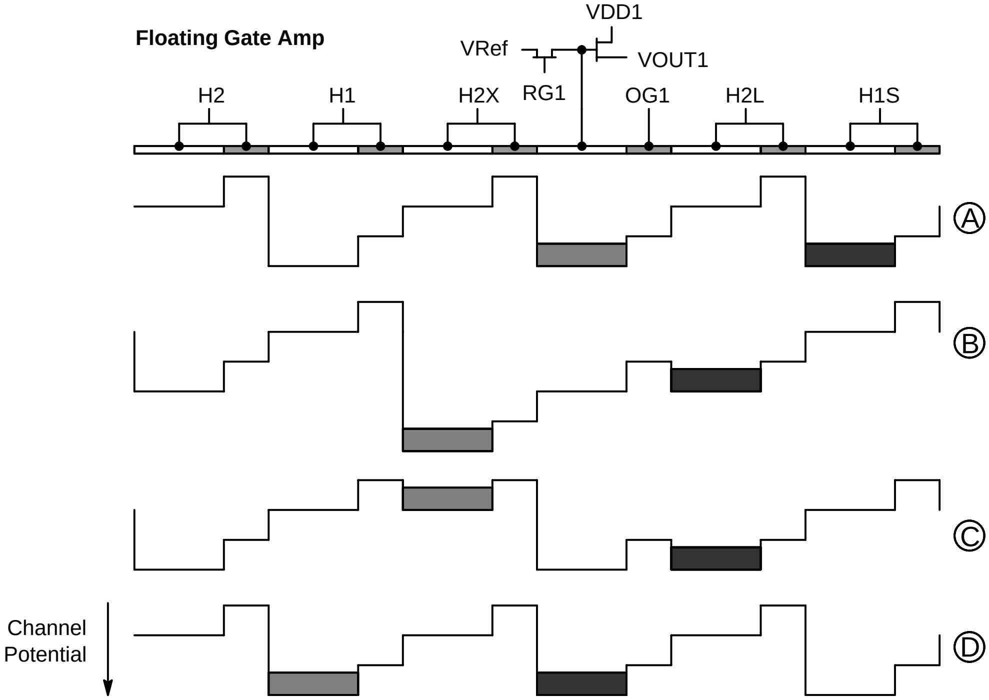


Figure 14. The Charge Transfer Path of One Quadrant

The non-destructive floating gate output amplifier is able to sense how much charge is present in a charge packet without altering the number of electrons in that charge packet. This type of amplifier has a low charge-to-voltage conversion gain (about 7.8 $\mu V/e^-$) and high noise (about 42 electrons), but it is being used only as a threshold detector, and not an imaging detector. Even with 42 electrons of noise, it is adequate to determine whether a charge packet is greater than or less than the recommended threshold of 120 electrons.

After one row has been transferred from the VCCD into the HCCD, the HCCD clock cycles should begin. After 8 clock cycles, the first dark VCCD column pixel will arrive at VOUT1. After another 24 (34 total) clock cycles, the first photo-active charge packet will arrive at VOUT1.

The transfer sequence of a charge packet through the floating gate amplifier is shown in Figure 15 below. The time steps of this sequence are labeled A through D, and are indicated in the timing diagram shown as Figure 16. The RG1 gate is pulsed high during the time that the H2X gate is pulsed high. This holds the floating gate at a constant voltage so the H2X gate can pull the charge packet out of the floating gate. The RG1 pulse should be at least as wide as the H2X pulse, and the H2X pulse width should be at least 12 ns. The rising edge of H2X relative to the falling edge of H1S is critical, specifically, the H2X pulse cannot begin its rising edge transition until the H1S edge is less than 0.4 V. If the H2X rising edge comes too soon then there may be some backward flow of charge for signals above 10,000 electrons.



NOTE: The differently shaded rectangles represent two separate charge packets. The direction of charge transfer is from right to left. Gates after H2X are connected to H1 or H2. Gates before H2X are connected to H1S or H2S.

Figure 15. Charge Package Transfer Sequence through the Floating Gate Amplifier

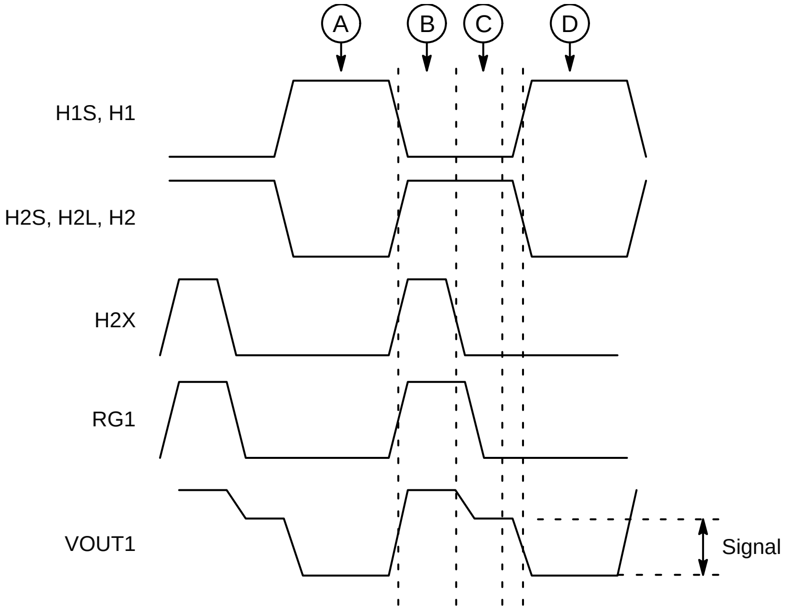


Figure 16. Timing Signals that Control the Transfer of Charge through the Floating Gate Amplifier

The charge packet is transferred under the floating gate on the falling edge of H2L. When this transfer takes place the floating gate is not connected to any voltage source. The presence of charge under the gate causes a change in voltage on the floating gate according to $V = Q/C$, where Q is the size of the charge packet and C is the capacitance of the floating gate. With an output sensitivity of $7.8\ \mu V/e^{-}$, each electron on the floating gate would give a $7.8\ \mu V$ change in VOUT1 voltage. Therefore if the decision threshold is to only allow charge packets of 126 electrons or less into the charge multiplier, this would correspond to $120 \times 7.8 = 936\ \mu V$. If the video output is less than $936\ \mu V$, then the camera must set the timing of the H2SW2 and H2SW3 pins to route the charge packet to the charge multiplier. This action must take place 28 clock cycles after the charge packet was under the floating gate amplifier. The 28 clock cycle delay is to allow for pipeline delays of the A/D converter inside the analog front end. The timing generator must examine the output of the analog front end and dynamically alter the timing on H2SW2 and H2SW3. To route a charge packet to the charge multiplier (VOUT3), H2SW2 is held at GND and H2SW3 is clocked with the same timing as H2 for that one clock cycle. To route a charge packet to the low gain output amplifier (VOUT2), H2SW3 is held at GND and H2SW2 is clocked with the same timing as H2S for that one clock cycle.

When operating the device at maximum (40 MHz) data rate, all the charge must be routed through the low gain amplifier (VOUT2). This is best accomplished with the floating gate reset (RG1) held at its high level while clocking the HCCD, and the H2X gate clocked with the same timing as H2S and H2B. During the line timing patterns L1 or L2, the RG1 gate should be clocked low. There is a diode on the sensor that sets the DC offset of the RG1 gate when it is clocked low. If the RG1 is not clocked low once per line then the RG1 DC offset will drift. This timing scheme is represented in the diagram shown below:

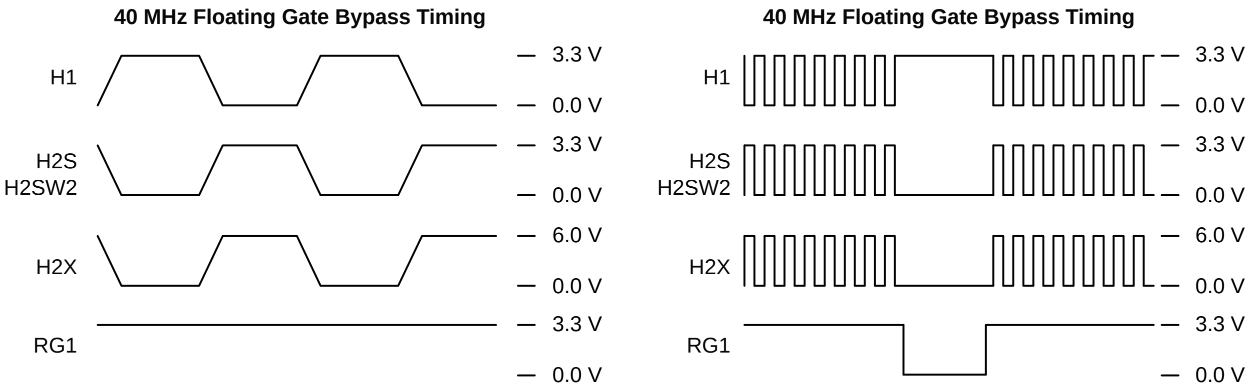
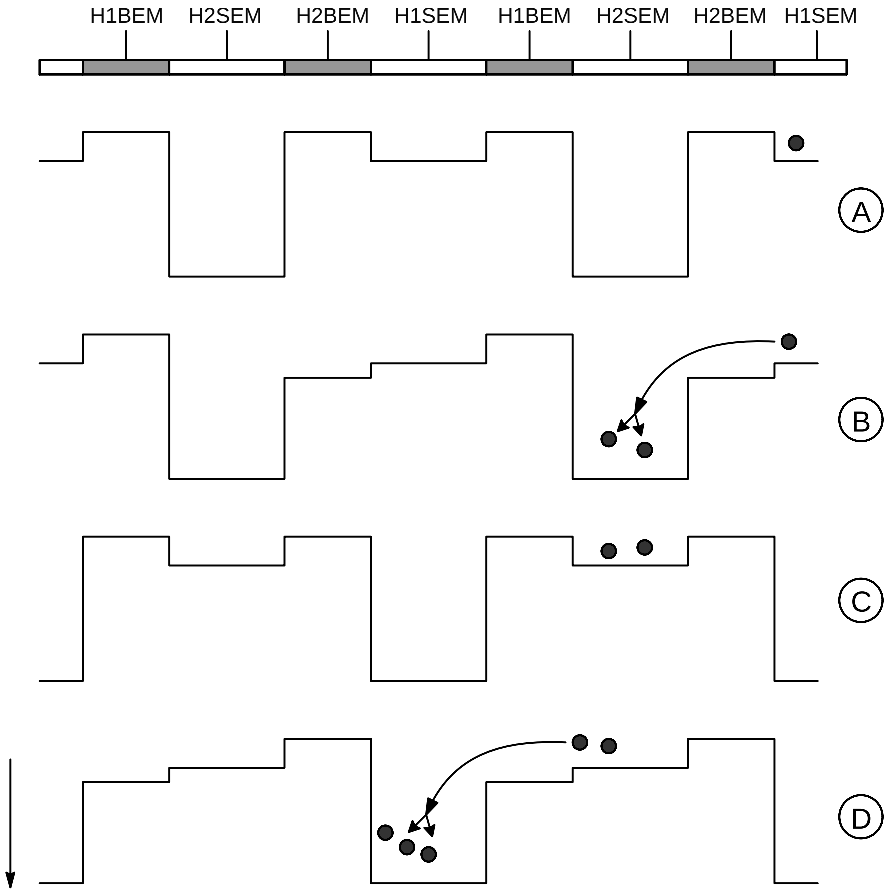


Figure 17. 40 MHz Floating Gate Bypass Timing

EMCCD OPERATION



NOTE: Charge flows from right to left.

Figure 18. The Charge Multiplication Process

The charge multiplication process, shown in Figure 18 above, begins at time step A, when an electron is held under the H1SEM gate. The H2BEM and H1BEM gates block the electron from transferring to the next phase until the H2SEM has reached its maximum voltage. When the H2BEM is clocked from 0 to +5 V, the channel potential under H2BEM increases until the electron can transfer from H1SEM to H2SEM. When the H2SEM gate is above 10 V, the electric field between the H2BEM and H2SEM gates gives the electron enough energy to free a second electron which is collected under H2SEM. Then the voltages on H2BEM and H2SEM are both returned to 0 V at the same time that H1SEM is ramped up to its maximum voltage. Now the process can repeat again with charge transferring into the H1SEM gate.

The alignment of clock edges is shown in Figure 19. The rising edge of the H1BEM and H2BEM gates must be delayed until the H1SEM or H2SEM gates have reached their maximum voltage. The falling edge of H1BEM and H2BEM must reach 0 V before the H1SEM or H2SEM reach 0 V. There are a total of 1,800 charge multiplying transfers through the EMCCD on each quadrant.

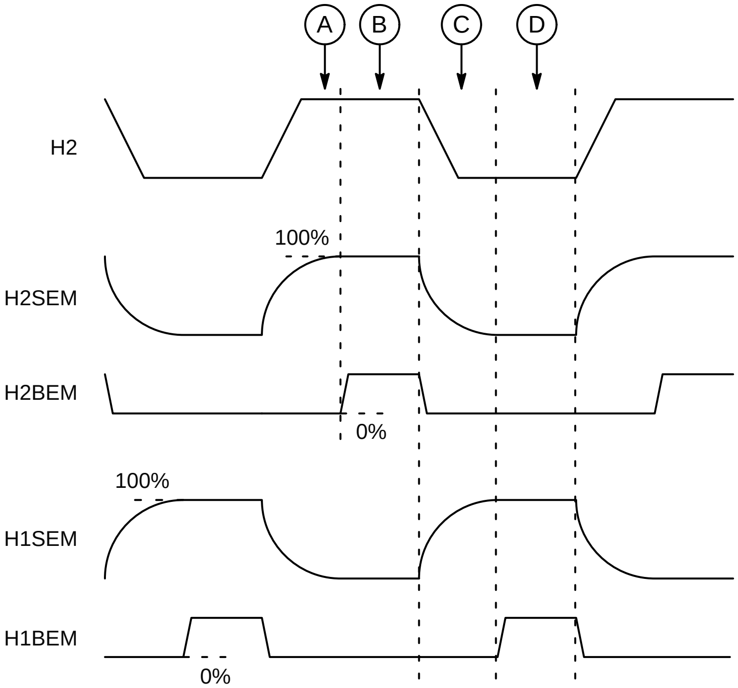
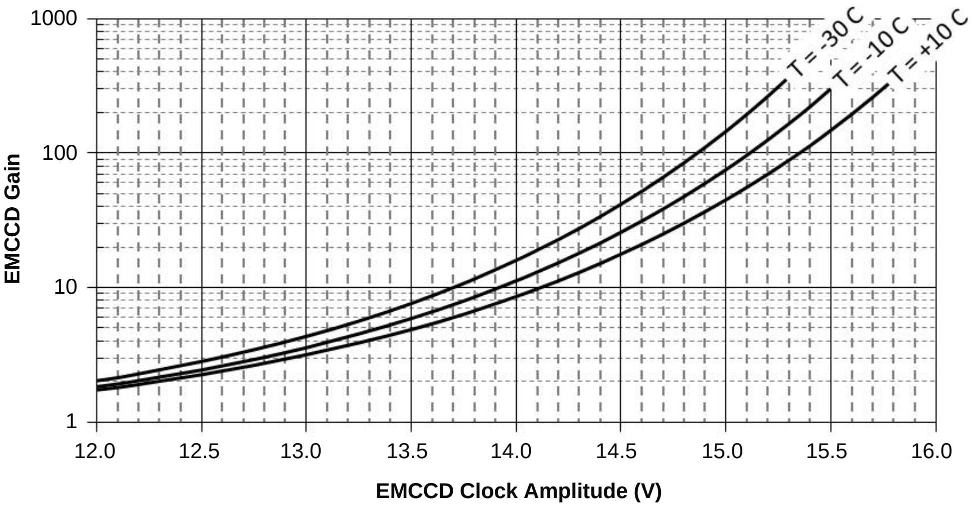


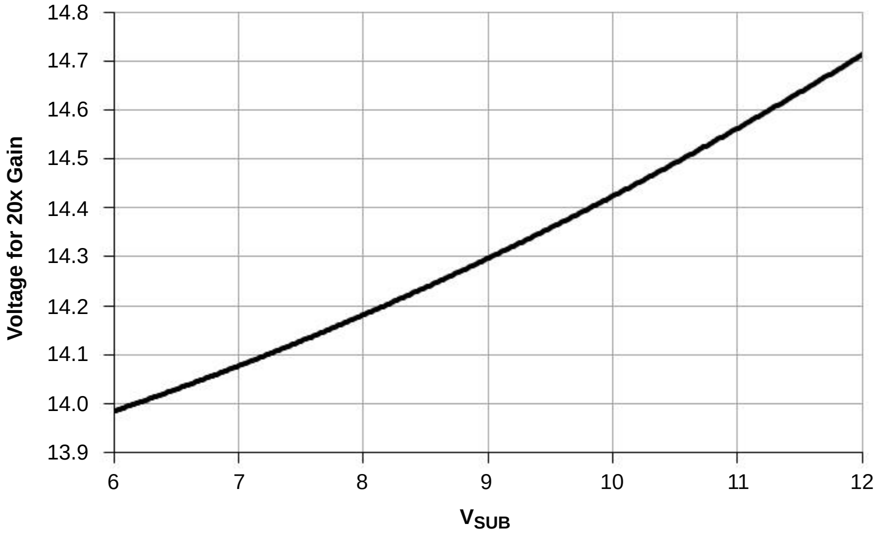
Figure 19. The Timing Diagram for Charge Multiplication

The amount of gain through the EMCCD will depend on temperature and H1SEM and H2SEM voltage as shown in Figure 20. Gain also depends on substrate voltage, as shown in Figure 21, and on the input signal, as shown in Figure 22.



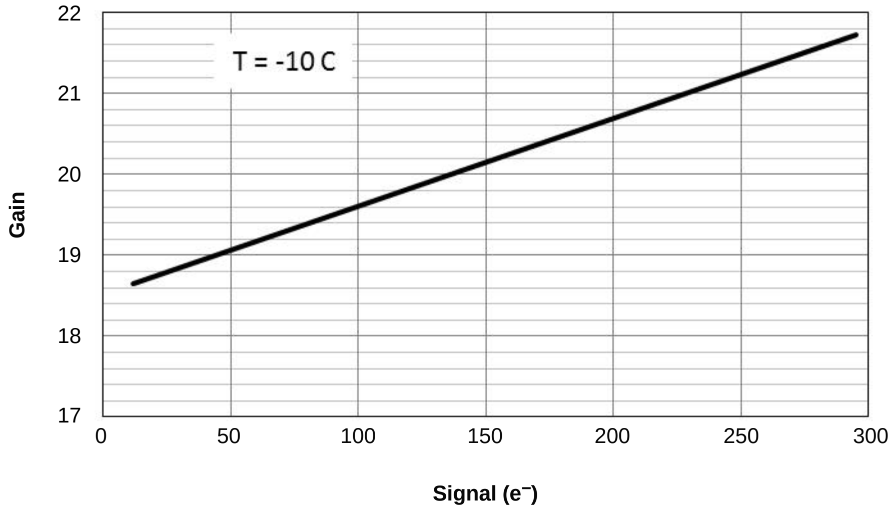
NOTE: This figure represents data from only one example image sensor, other image sensors will vary.

Figure 20. The Variation of Gain vs. EMCCD High Voltage and Temperature



NOTE: EMCCD gain is not constant with substrate voltage.

Figure 21. The Requirement EMCCD Voltage for Gain of 20x vs. Substrate Voltage



NOTE: The EMCCD voltage was set to provide 20x gain with an input of 180 electrons.

Figure 22. EMCCD Gain vs. Input Signal

If more than one output is used, then the EMCCD high level voltage must be independently adjusted for each quadrant. This is because each quadrant will require a slightly different voltage to obtain the same gain. In addition, the voltage required for a given gain differs unpredictably from one image sensor to the next, as in Figure 23. Because of this, the gain vs. voltage relationship must be calibrated for each image sensor, although within each quadrant, the H1SEM and H2SEM high level voltage should be equal.

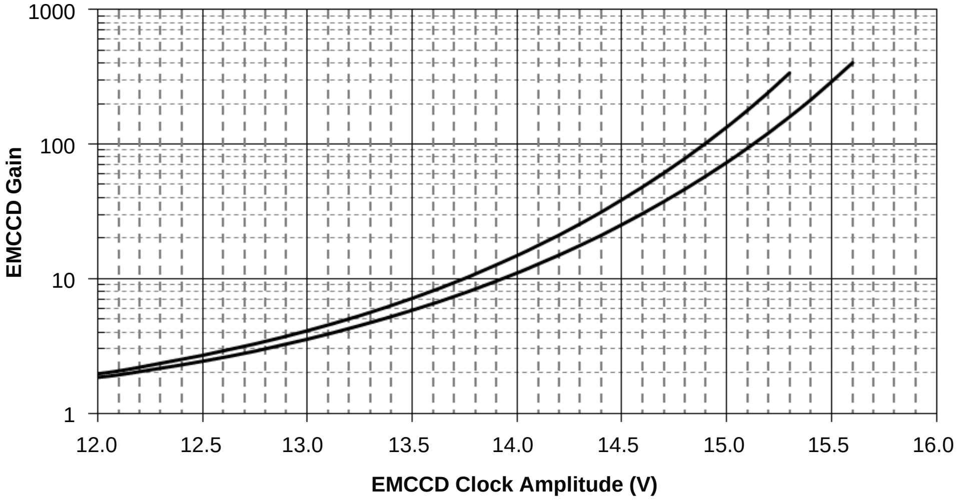
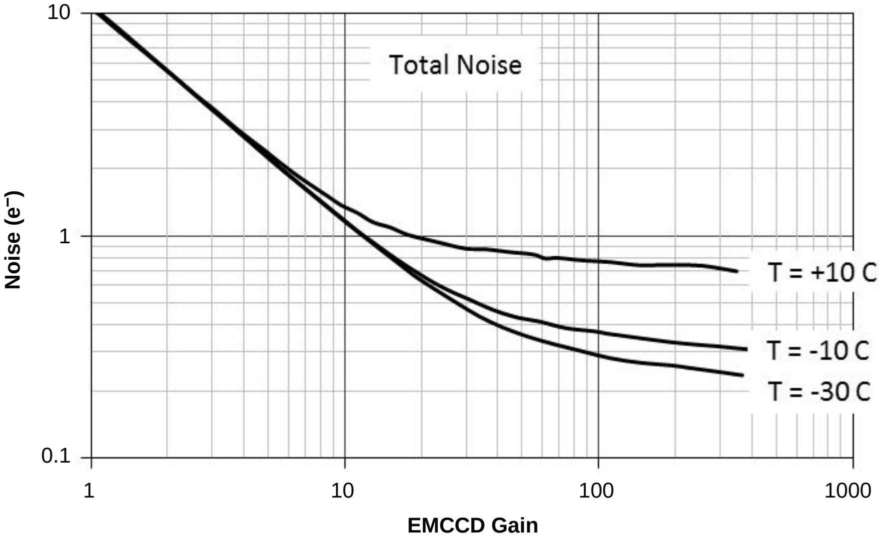


Figure 23. An Example Showing How Two Image Sensors Can Have Different Gain vs. Voltage Curves

The effective output noise of the image sensor is defined as the noise of the output signal divided by the gain. This is measured with zero input signal to the EMCCD. Figure 24 shows the EMCCD by itself has a very low noise that goes as the noise at gain = 1 divided by the gain. The EMCCD has very little clock-induced charge and does not require elaborate sinusoidal waveform clock drivers. Simple square wave clock drivers with a resistor between the driver and sensor for a small RC time constant are all that is needed. However, the pixel array may acquire spurious charge as a function of VCCD clock driver characteristics.



NOTE: The data represented by this chart includes noise from dark current and spurious charge generation.

Figure 24. EMCCD Output Noise vs. EMCCD Gain in Single Output Mode from −30°C to +10°C

Because of these pixel array noise sources, it is recommended that the maximum gain used be 100x, which typically gives a noise floor between 0.4e and 0.6e at −10°C. Using higher gains will provide limited benefit and will degrade the signal to noise ratio due to the EMCCD excess noise factor and spurious charge in the VCCD. Furthermore, the image sensor is not limited by dark current noise sources when the temperature is below −10°C. Therefore, cooling below −10°C will not provide a significant improvement to the noise floor, with the negative consequence that lower temperatures increase the probability of poor charge transfer.

CAUTION: The EMCCD should not be operated near saturation for an extended period, as this may result in gain aging and permanently reduce the gain. It should be noted that device degradation associated with gain aging is not covered under the device warranty.

Operating Temperature

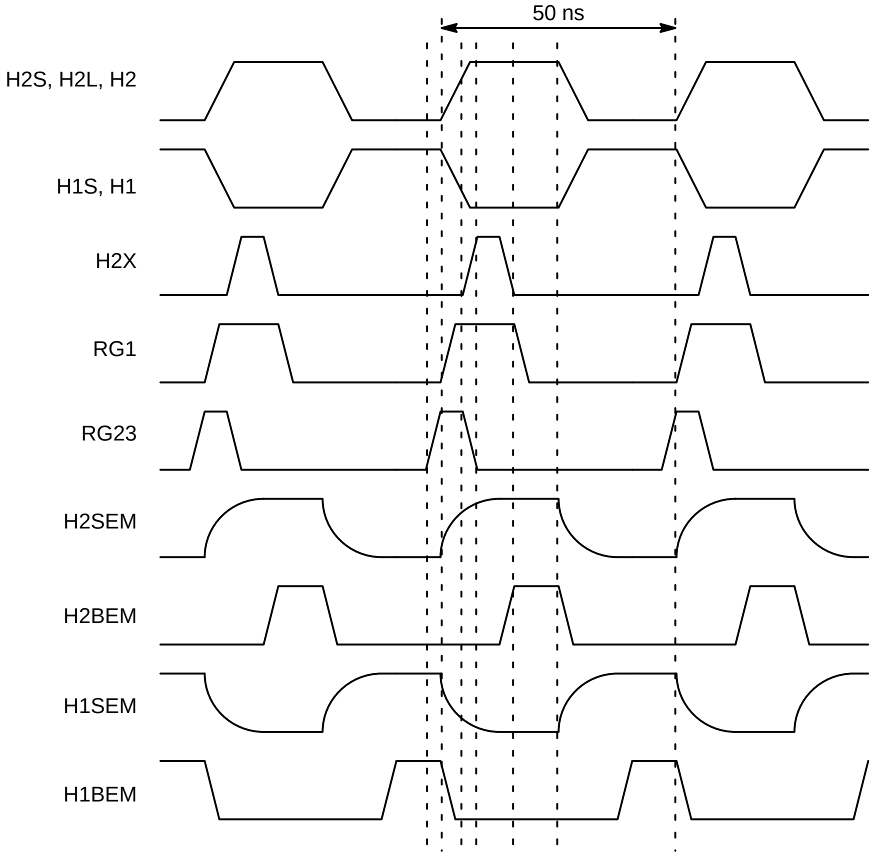
The reasons for lowering the operating temperature are to reduce dark current noise and to reduce image defects. The average dark signal from the VCCD and photodiodes must be less than 1e⁻ in order to have a total system noise less than 1e⁻ when using the EMCCD. The recommended operating temperature is −10°C. This represents the best compromise of low noise performance vs. complexity of cooling the image sensor. Operation below −30°C is not recommended, and temperatures below −30°C may result in poor charge transfer in the HCCD. Operation above 0°C may result in excessive dark current noise.

Charge Switch Threshold

The floating gate output amplifier (VOUT1) is used to select the routing of a pixel charge packet at the charge switch. Pixels with large signals should be routed to the normal floating diffusion amplifier at VOUT2. Pixels with small signals should be routed to the EMCCD and VOUT3. The routing of pixels is controlled by the timing on H2SW2 and H2SW3. The optimum signal threshold for that transition between VOUT2 and VOUT3 is approximately 3 times the floating gate amplifier noise, or 126 e⁻. Sending signals larger than 126 e⁻ into the EMCCD will produce images with lower signal to noise ratio than if they were read out of the normal floating diffusion output of VOUT2.

TIMING DIAGRAMS

Pixel Timing



NOTE: The minimum time for one pixel is 50 ns.

Figure 25. Pixel Timing Pattern P1

Black, Clamp, VOUT1, VOUT2, and VOUT3 Alignment at Line Start

The black level clamping operation of the analog front end (AFE) should take place within the first 28 clock cycles of every row. This applies to all modes of operation.

VCCD Timing

Vertical Transfer Times and Pulse Widths

Table 14. TIMING DEFINITIONS

Symbol	Definition	Min	Nominal	Max	Unit
T_{VA}	VCCD Transfer Time A	1.2	1.2	2.0	μs
T_{VB}	VCCD Transfer Time B	1.2	1.2	4.0	μs
T_{SUB}	Electronic Shutter Pulse	2.0	2.5	10.0	μs
T_3	Photodiode to VCCD Transfer Time	3.0	3.0	5.0	μs

Clock Edge Alignments for V1, V2, V3, V4

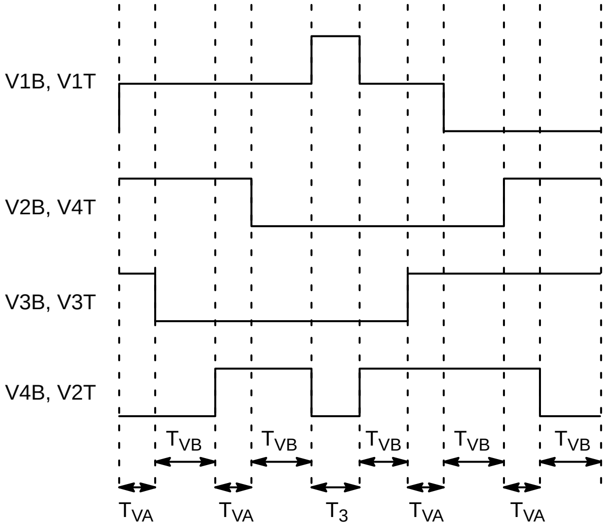


Figure 26. Timing Pattern F1. VCCD Frame Timing to Transfer Charge from Photodiodes to the VCCD when Using the Bottom HCCD Outputs A or B

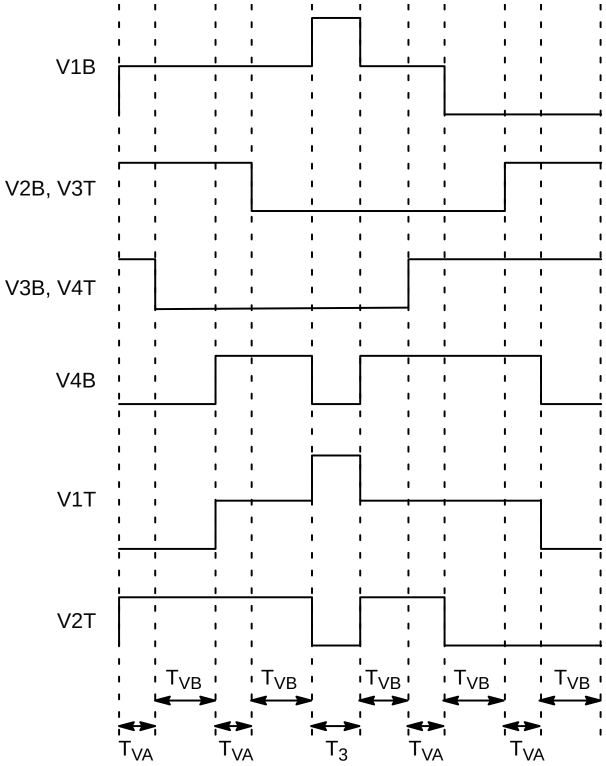


Figure 27. Timing Pattern F2. VCCD Frame Timing to Transfer Charge from Photodiodes to the VCCD when Using All Four Outputs in Quad Output Mode

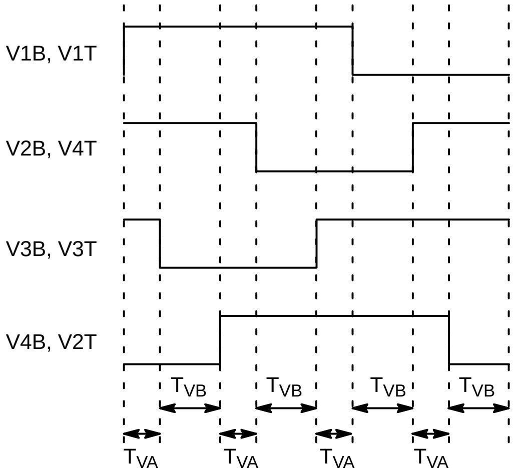


Figure 28. Line Timing L1. VCCD Line Timing to Transfer One Line of Charge from VCCD to the HCCD when Using the Bottom HCCD Outputs A or B in Single or Dual Output Modes

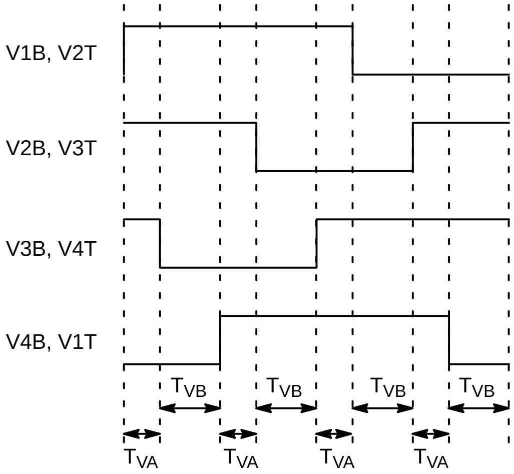


Figure 29. Line Timing L2. VCCD Line Timing to Transfer One Line of Charge from the VCCD to the HCCD when Using All Four Outputs in Quad Output Mode

Electronic Shutter

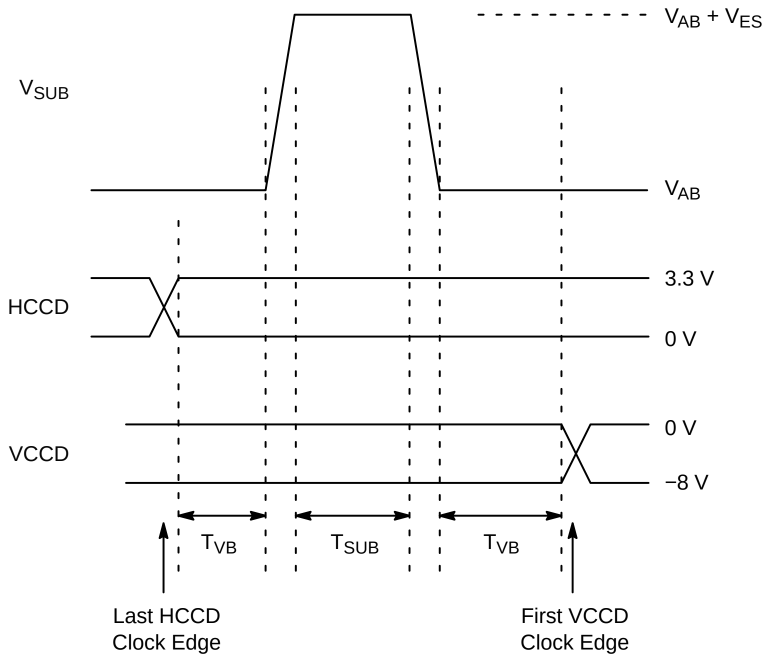


Figure 30. Electronic Shutter Timing Pattern S1

CAUTION: The EMCCD register must not be clocked while the electronic shutter pulse is high.

HCCD and EMCCD Clocks for Electronics Shutter

The HCCD and EMCCD clocks must be static during the frame, line, and electronic shutter timing sequences.

Table 15. HCCD AND EMCCD CLOCKS FOR ELECTRONICS SHUTTER

Clocks	State
H1S, H1, H1SEM, H1BEM	High
H2S, H2, H2SW, H2L, H2X, H2SEM, H2BEM	Low

HCCD Timing

To reverse the direction of charge transfer in a Horizontal CCD, the timing patterns of the H1B and H2B inputs of that HCCD are exchanged. If a HCCD is not used, all of its gates are to be held at the high level.

Table 16. HCCD TIMING

Mode	HCCD a, b Timing	HCCD c, d Timing
Single	H1Ba = H2Bb = H1Sa = H1Sb H2Ba = H1Bb = H2Sa = H2Sb	3.3 V
Dual	H1Ba = H1Bb = H1Sa = H1Sb H2Ba = H2Bb = H2Sa = H2Sb	3.3 V
Quad	H1Ba = H1Bb = H1Sa = H1Sb H2Ba = H2Bb = H2Sa = H2Sb	H1Bc = H1Bd = H1Sc = H1Sd H2Bc = H2Bd = H2Sc = H2Sd

Table 17. FRAME RATES

Single	Dual (Left/Right)	Dual (Top/Bottom)	Quad	Unit
3.7	6.9	7.4	13.8	fps

Image Exposure and Readout

The flowchart for image exposure and readout is shown in the figure below. The electronic shutter timing may be omitted to obtain an exposure time equal to the image read out time. NEXP is the number of lines exposure time and NV is the number of VCCD clock cycles (row transfers).

Table 18. IMAGE READOUT TIMING

Mode	NH	NV	Line Timing	Frame Timing
Single	2316	2144	L1	F1
Dual (Left/Right)	1158	2144	L1	F1
Dual (Top/Bottom)	2316	1072	L2	F2
Quad	1158	1072	L2	F2

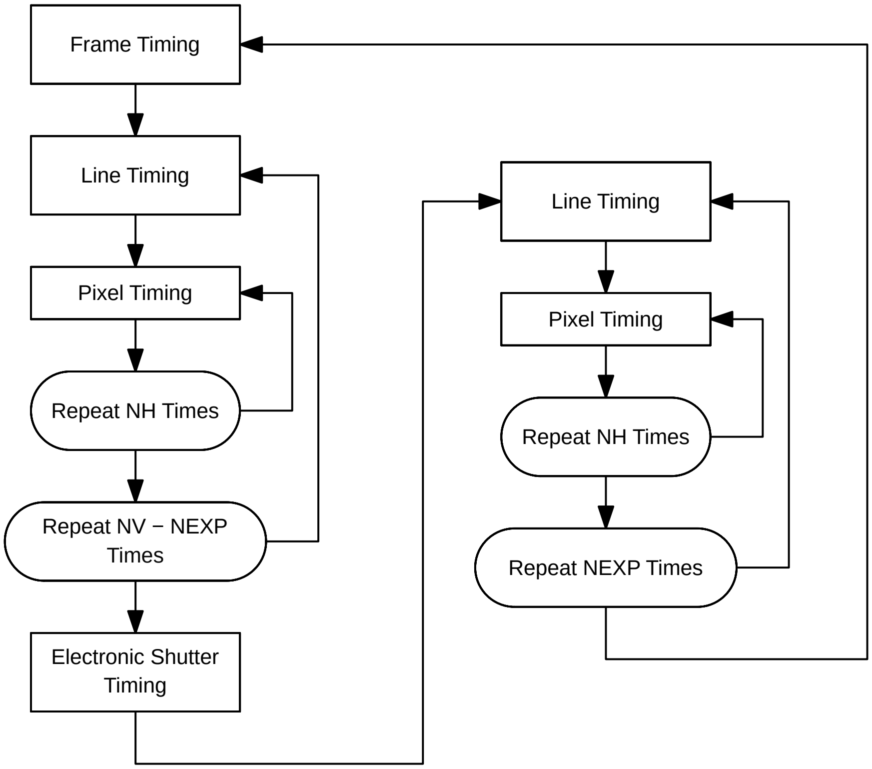


Figure 31. The Image Readout Timing Flow Chart

Long Integrations and Readout

For extended integrations the output amplifiers need to be powered down. When powered up, the output amplifiers emit near infrared light that is sensed by the photodiodes. It will begin to be visible in images of 30 second integrations or longer.

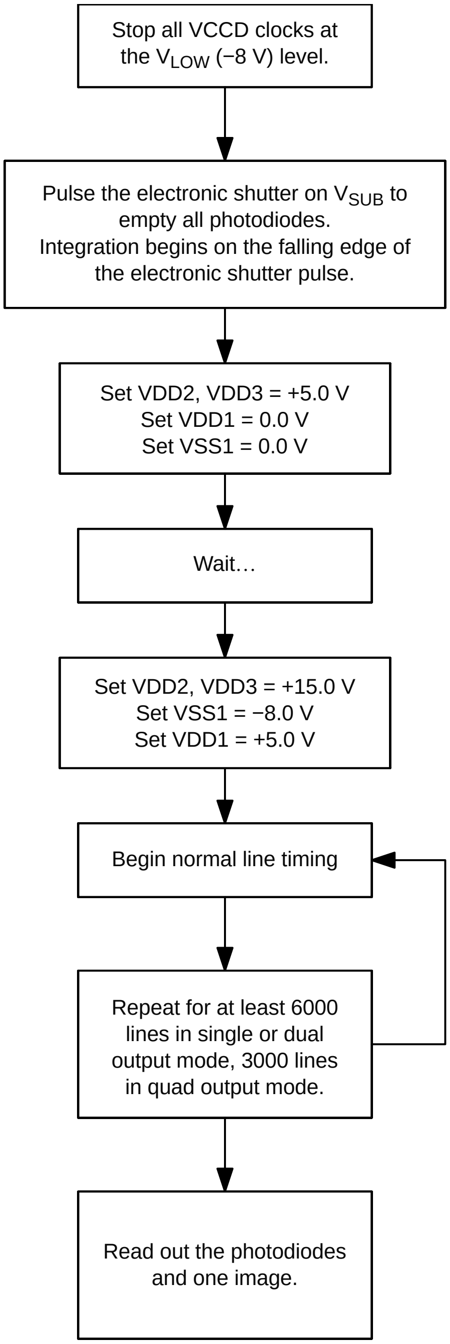


Figure 32. Timing Flow Chart for Long Integration Time

To power down the output amplifiers set VDD1 and VSS1 to 0 V, and VDD2(a,b,c,d) and VDD3(a,b,c,d) to +5 V. VDD2 or VDD3 must not be set to 0 V during the integration of an image. During the time the VDD2 and VDD3 supplies are reduced to +5 V the VDD15 pin is to be kept at +15 V. The substrate voltage reference output SUBV will be valid as long as VDD15 is powered. The HCCD and EMCCD may be continue to clock during integration. If they are stopped during integration then the EMCCD should be re-started at +7 V amplitude to flush out any undesired signal before increasing the voltage to charge multiplying levels.

STORAGE AND HANDLING

Table 19. STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Unit
Temperature (Note 26)	T_{ST}	−55	80	°C
Humidity (Note 27)	RH	5	90	%

26. Long-term exposure toward the maximum temperature will accelerate color filter degradation.
27. T = 25°C. Excessive humidity will degrade Mean Time to Failure (MTTF.)

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL INFORMATION

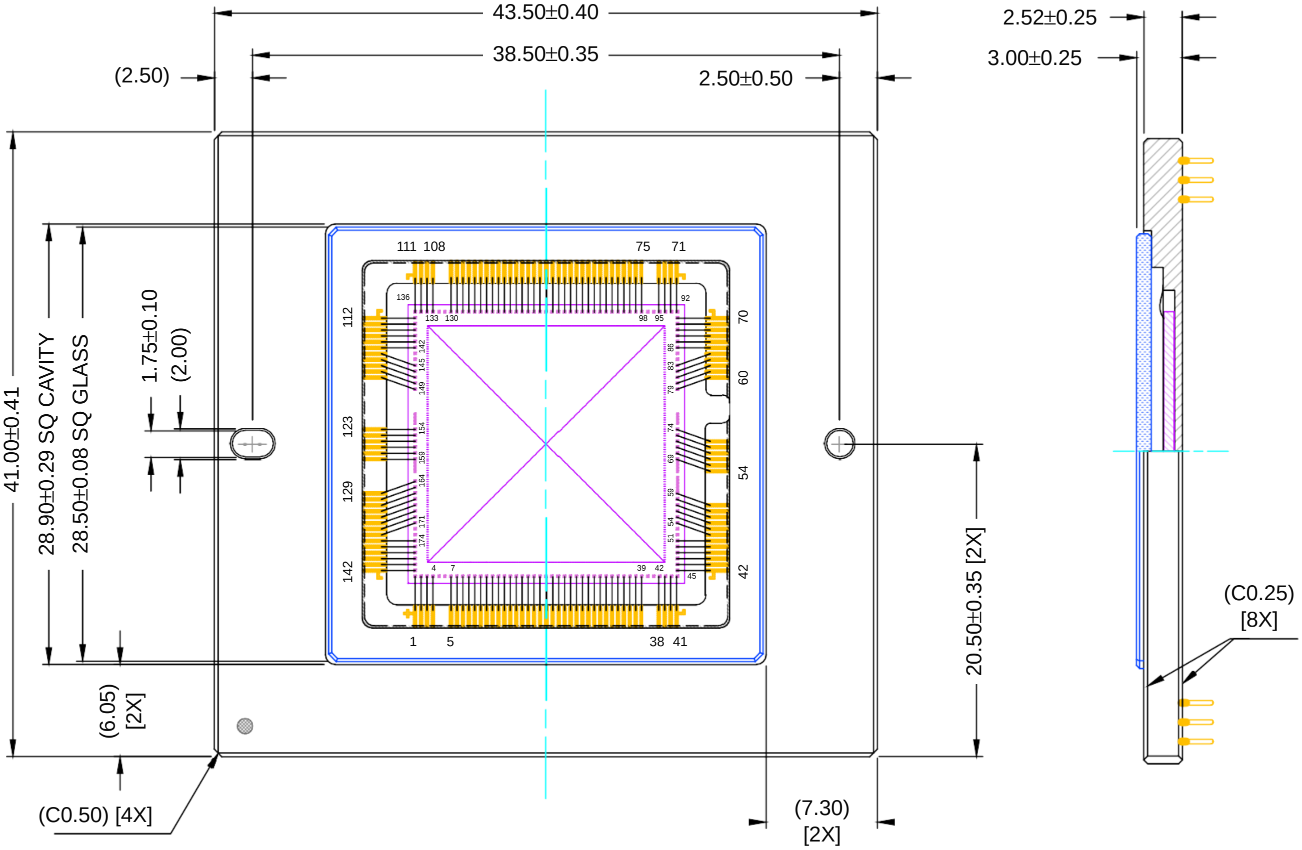


Figure 33. Completed Assembly 1

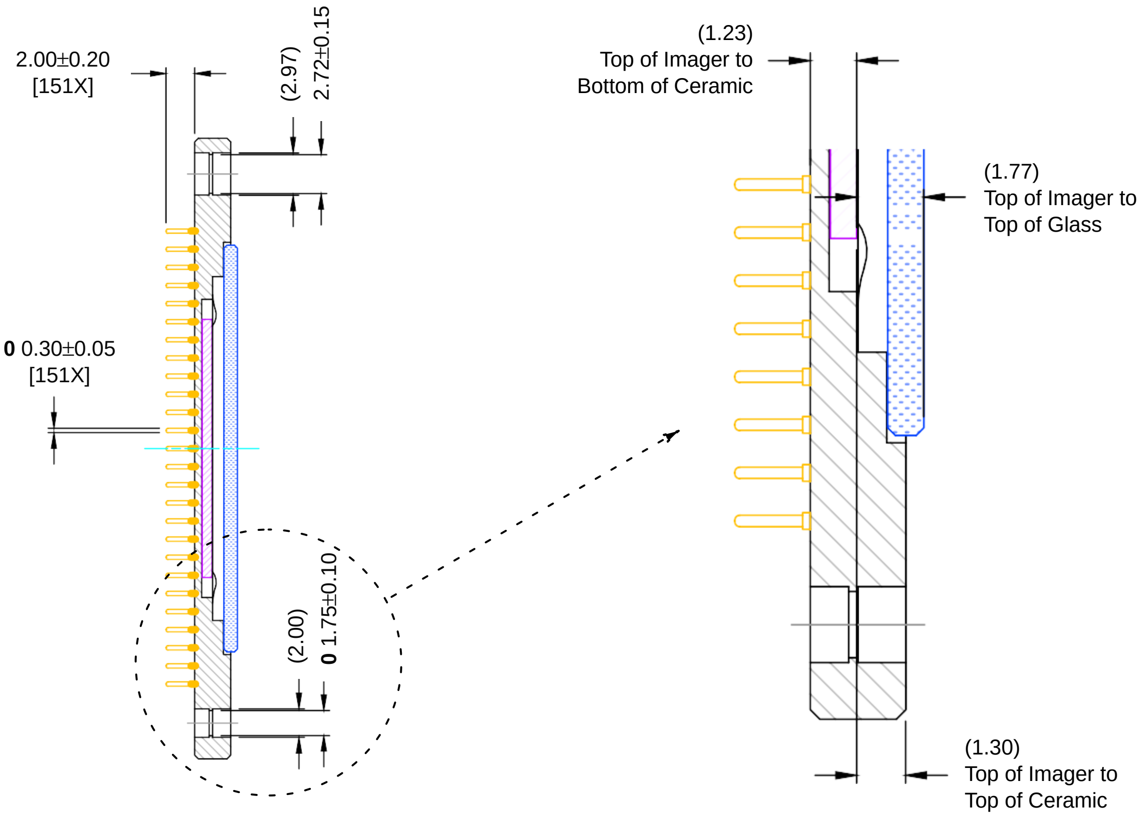
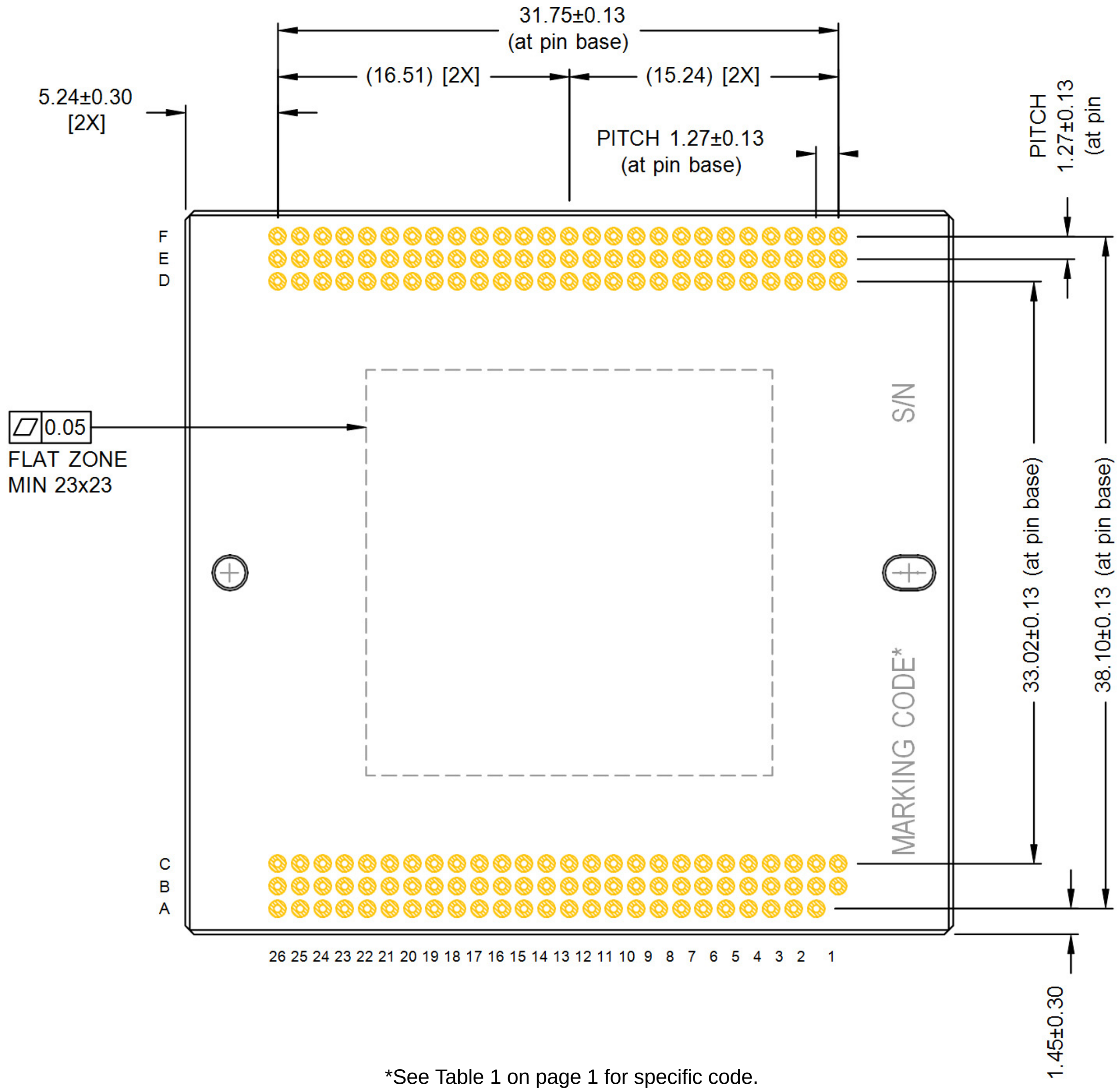


Figure 34. Completed Assembly 2



*See Table 1 on page 1 for specific code.

Figure 35. Completed Assembly 3

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