AS0142AT

Advance Information

1/4-Inch 1.0 Mp Color CMOS Digital Image Sensor and Signal Processor Stack Chip

ON Semiconductor®

www.onsemi.com

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Features

- Latest 3.0 μm pixel with ON Semiconductor DR−Pix™ technology
- Superior Low−light Performance
- 45 fps at 1.0 MP, 60 fps at 720p
- Linear or High Dynamic Range Video
- Color Processing Optimized for HDR Video Operation
- Color and Gamma Correction
- Auto Exposure, Auto White Balance, 50/60 Hz Auto Flicker Detection and Avoidance
- Adaptive Local Tone Mapping (ALTM)
- Programmable Spatial Transform Engine (STE)
- Pre−rendered Graphical Overlay
  - Line and Arc support
  - 191 characters from UTF−8/Unicode
  - 64 user−defined characters
- Two−wire Serial Programming Interface (CCIS)
- Parallel output, OpenLDI to directly drive displays
- Supports 1−clock or 2−clocks per pixel output modes
- Interface to low−cost Flash or EEPROM through SPI bus (to configure and load patches, etc.)
- High−level host command interface
- Standalone operation supported
- Up to 7 GPIO
- Fail−safe IO
- Multi−Camera synchronization support

Applications

- Automotive ADAS
- Automotive surround and rear−view
- ADAS + Viewing Fusion
- High dynamic range imaging
- Mirror Replacement (CMS)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Table 1. KEY PARAMETERS

Parameter	Feature
Optical Format	1/4−inch
Maximum Resolution	1280 x 800 (1.0 Mp)
Shutter Type	Electronic Rolling Shutter (ERS)
Pixel Size	3 μm x 3 μm
Output Interface	Up to 24−bit parallel (Note 1)
Output Formats	RGB888, RGB565, YUV422 8−/10−bit
Control Interface	Two−Wire, Serial Control 100 kHz/1 MHz
Input clock Range	10 − 29 MHz
Maximum Frame Rate	45 fps at 1.0Mp 60 fps at 720p
Output Pixel Clock Maximum Rate	125 MHz (Note 2)
Max Dynamic Range	93 dB
Packaging Option	8.5 mm x 8.5 mm 143 Pins iBGA
Operating Temperature Range [Ambient]	−40°C to 105°C
Supply Voltage (Nominal)	VDDIO (Host) 1.8 or 2.8 V VDDIO (Sensor) 1.8 V VDD (Regulator) 1.8 V VAA/ Analog 2.8 V OTPM 2.8 V
Power Consumption	530 mW target [Full−Res 30fps HDR mode] (Note 3)

1. Maximum frame rates depend on output interface and data format configuration used.
2. Maximum pixel clock rates depend on IO voltage. Please see table 25/ 26 for details.
3. Excluding VDDIO (Host) and VDDIO (Sensor)

Table 2. ORDERING INFORMATION

Part Number	Product Description	Orderable Product Attribute Description
AS0142ATSC00XUSM0−DRBR−E	Rev1, Engineering Sample, iBGA Package	Dry−pack without Protective Film; Double Side ARC Glass
AS0142ATSC00XUSM0−DPBR−E	Rev1, Engineering Sample, iBGA Package	Dry−pack with Protective Film; Double Side ARC Glass
AS0142ATSC00XUSM0−TRBR−E	Rev1, Engineering Sample, iBGA Package	Tape & Reel without Protective Film; Double Side ARC Glass
AS0142ATSC00XUSM0−TPBR−E	Rev1, Engineering Sample, iBGA Package	Tape & Reel with Protective Film; Double Side ARC Glass
AS0142ATSC00XUSM0H3−GEVB	AS0142 Rev 1 iBGA Sample housed in DEMO3 Headboard	N/A

GENERAL DESCRIPTION

The ON Semiconductor AS0142AT is a 1.0 MP CMOS digital image sensor and signal processor for automotive viewing applications. The device includes full auto−functions support (AWB and AE) and ALTM (Adaptive Local Tone Mapping) to enhance HDR image/video. The AS0142AT implements a high−sensitivity 3.0 μm pixel with DR−Pix technology and advanced noise reduction, to enable excellent low−light performance. It can be operated in either linear or high dynamic range modes. The AS0142AT may be operated in video (master) mode or in single frame trigger mode, providing flexibility for multi−camera systems.

FUNCTIONAL OVERVIEW

Figure 1 shows the typical configuration of the AS0142AT in a camera system. On the host side, a two−wire serial or SPI interface is used to configure the operation of the AS0142AT, and image data is transferred using the parallel interface between the AS0142AT and the host. Image data from 1200x800 Active Color Array is communicated with AS0142AT embedded image co−processor via internal parallel or HiSPi interface.

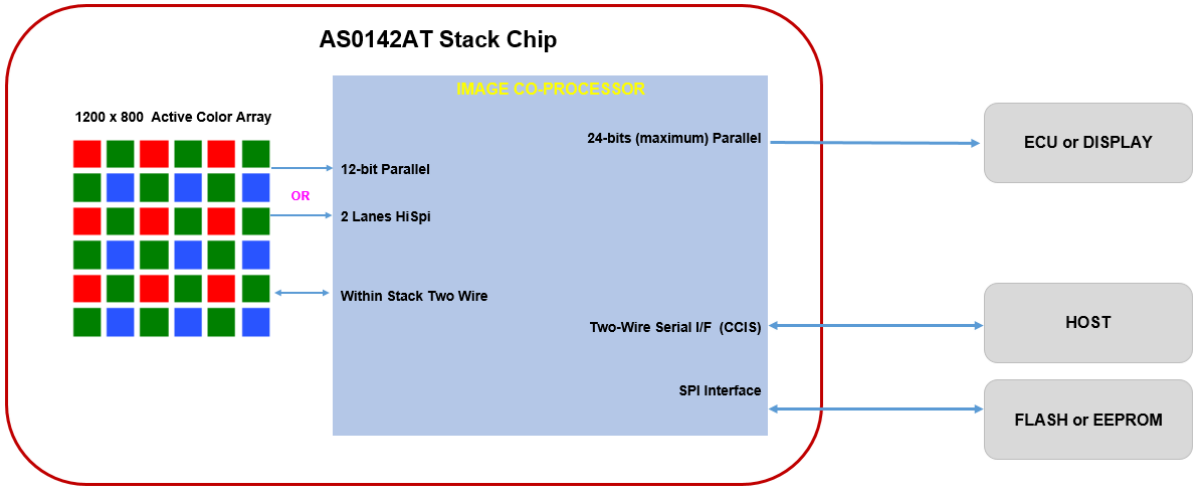


Figure 1. AS0142AT Connectivity

Figure 2. Example AS0142AT Connectivity

SYSTEM INTERFACES

Figure 3: “Typical Parallel Configuration (Legacy Mode) @ AS0142AT Internal Regulator” shows typical AS0142AT device connections.

All power supply rails must be decoupled from ground using capacitors as close as possible to the package.

The AS0142AT signals to the sensor and host interfaces can be at different supply voltage levels to optimize power consumption and maximize flexibility. Table 3 provides the signal descriptions for the AS0142AT.

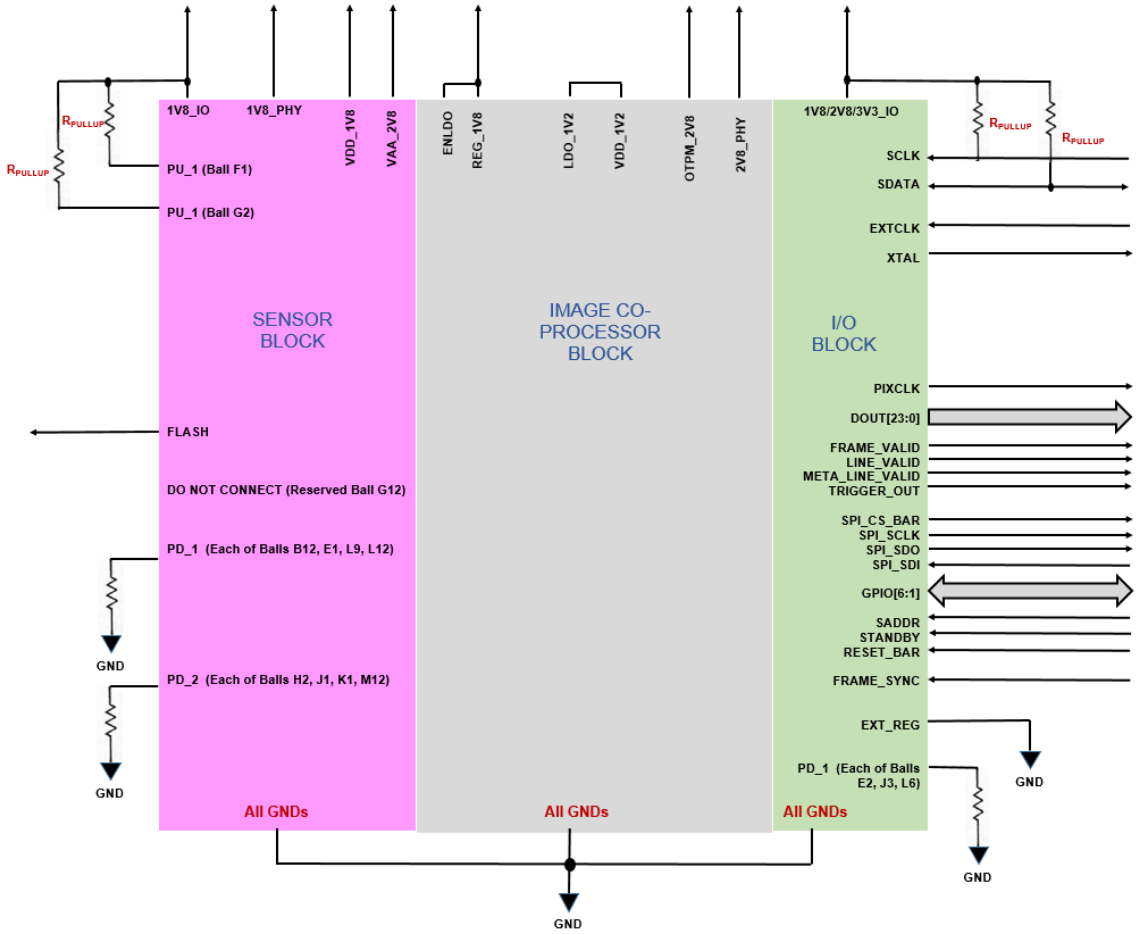


Figure 3. Typical Parallel Configuration (Legacy Mode) @ AS0142AT Internal Regulator

1. Minimum “Bypass Capacitor Set” recommendation

Block	Supply	Bypass Capacitor Set			Number of Sets Minimum
		10 µF	1 µF	0.1 uF	
I/O	1V8/2V8/3V3_IO	X	X	X	1
Image Co−Processor	2V8_PHY		X	X	1
	OTPM_2V8		X	X	1
	VDD_1V2		X	X	1
	LDO_1V2		X	X	1
	REG_1V8		X	X	1
Sensor	1V8_IO	X	X	X	2
	1V8_PHY	X	X	X	2
	VAA_2V8	X	X	X	3
	VDD_1V8	X	X	X	1

2. ON Semiconductor recommends a 1.5 kΩ resistor value for the two−wire serial interface RPULL-UP. However, greater values may be used for slower two−wire serial transmission speed.
3. RESET_BAR has an internal pull−up resistor and can be left floating if not used.
4. The decoupling capacitors for the regulator input and output should have a value of 1.0 µF and 0.1 uF each. The capacitors should be ceramic and need to have X5R or X7R dielectric.
5. PU_1 & PD_1 connection are mandatory; PD_2 are strongly recommended.
6. Decoupling capacitors for each power supply should be mounted as close as possible to the supply pin(s). Actual values and numbers may vary, depending on layout and design consideration.
7. The diagram is showing typical parallel configuration. If Crossbar mode is used, the 27 parallel outputs can be assigned to any output pad. Refer to crossbar section for more details.
8. Contact ON Semiconductor for case of “VDD_1V2” being supplied by external voltage source.

SENSOR PIXEL ARRAY OUTPUT – HISPI/ PARALLEL CONFIGURATION

Sensor Pixel Array Output can be fed either in HiSPi or Parallel configuration, to the embedded AS0142AT Image Co−Processor, via stream settings command.

More information will be provided in future Datasheet update.

CRYSTAL USAGE

As an alternative to using an external oscillator, a crystal may be connected between EXTCLK and XTAL. Two small loading capacitors and a feedback resistor should be added, as shown in Figure 4.

For applications above 85°C, ON Semiconductor does not recommend using crystal option. An external oscillator with temperature compensation is instead recommended for higher temperature applications.

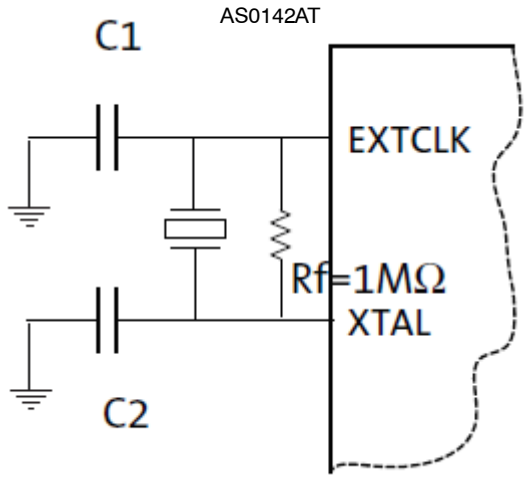


Figure 4. Using a Crystal Instead of an External Oscillator

Rf represents the feedback resistor, and a Rf value of 1 MΩ is sufficient for AS0142AT. C1 and C2 are decided according to the crystal (or resonator) CL specification. In the steady state of oscillation, CL is defined as (C1 * C2)/(C1 + C2). In fact, the I/O ports, the bond pad, package pin and PCB traces all contribute the parasitic capacitance to C1 and C2. Therefore, CL can be rewritten to be (C1' * C2')/(C1' + C2'), where C1' = (C1+CIN, STRAY1) and C2' = (C2+COUT, STRAY2). The stray capacitance for the I/O ports, bond pad, and package pins are known, so the formulas can be rewritten as Cl' = (Cl + CIN + PCB_EXTCLK) and C2' = (C2 + COUT + PCB_XTAL).

PIN DESCRIPTIONS

Table 3. PINOUT DESCRIPTION

Pinout Category	Pinout Name(s)	Pinout Direction	Correspondent Ball(s)	Ball(s) Total	Note(s)
Power	1V8/2V8/3V3_IO	Supply	D12, E12, F12	3	• Host Interface Supply, 1.8V/ 2.8V/ 3.3V capable
	1V8_IO	Supply	D3, E3	2	• Sensor Interface Supply, 1.8V nominal
	2V8_PHY	Supply	C6	1	• Host HiSPi Supply, 2.8V nominal
	1V8_PHY	Supply	C1	1	• Sensor HiSPi Supply, 1.8V nominal
	OTPM_2V8	Supply	L5	1	• Host OTPM Supply, 2.8V nominal
	VAA_2V8	Supply	A2, A3, A4	3	• Sensor Array Supply, 2.8V nominal
	REG_1V8	Supply	B4, B5, C5	3	• Host Regulator Supply, 1.8V nominal
	VDD_1V8	Supply	A1, B1, B2	3	• Sensor Digital Core Supply, 1.8V nominal
	LDO_1V2	Supply	A5, A6, B6	3	• Host Regulator Output, 1.2V nominal • Sense Line embedded
	VDD_1V2	Supply	A11, A12, B11	3	• Host Digital Core Supply, 1.2V nominal
	AGND	Supply – GND	H11, H12, J11, J12, K11, K12	6	• Analog related Stack Chip Ground
	DGND	Supply – GND	D4 to D9, E4 to E9, F4 to F9, G4 to G9, H4 to H9, J4 to J9	36	• Digital related Stack Chip Ground
Host Regulator Control	ENLDO	Input	B9	1	• Host Regulator enable (REG_1V8 domain)
	EXT_REG	Input	A8	1	• External Supply enable (VDD_1V2 domain)
Master Clock	EXTCLK	Input	C8	1	• This can either be a square−wave generated from an oscillator (in which case the XTAL input must be left unconnected), or direct connection to a crystal
	XTAL	Output	B7	1	• If EXTCLK is connected to one pin of a crystal, the other pin of the crystal is connected to XTAL pin; otherwise this signal must be left unconnected.

Table 3. PINOUT DESCRIPTION

Pinout Category	Pinout Name(s)	Pinout Direction	Correspondent Ball(s)	Ball(s) Total	Note(s)
SPI Interface	SPI_CS_BAR	Output	F3	1	• Chip select out to SPI flash or EEPROM memory
	SPI_SCLK	Output	G3	1	• Clock output for interfacing to an external SPI flash or EEPROM memory
	SPI_SDI	Input	L4	1	• Data in from SPI flash or EEPROM memory • Pin with Internal Pull Up Resistor • When no SPI device detected, the logic state of this pin decides whether AS0142AT should perform Auto−Configure ♦ 0: Do not Auto−Configure; Two−wire interface will be used to configure the device (i.e. Host−Configure mode) ♦ 1: Auto−Configure
	SPI_SDO	Output	L3	1	• Data out to SPI flash or EEPROM memory
Two Wired	SCLK	Input	G1	1	• Host two−wire serial clock • Recommended 1.5 kΩ to 1V8/2V8/3V3_IO
	SDATA	I/O	K2	1	• Host two−wire serial data • Recommended 1.5 kΩ to 1V8/2V8/3V3_IO
General Purpose I/O	GPIO[6:1]	I/O	L2, J2, K6, L7, K4, K5	6	• Configurable Host I/O interface
Inactive Control	RESET_BAR	Input	F2	1	• Hard Reset Control, Active Low • No Hardware State Retention • Pin with Internal Pull Up Resistor
	STANDBY	Input	H3	1	• Hard Standby Control, Active High • Hardware State Retention possible
Two Wire Address Definition	SADDR	Input	K3	1	• Selects device address for the two−wire slave serial interface ♦ When connected to GND the device ID is 0x90 ♦ When wired to 1V8/2V8/3V3_IO, the device ID is 0xBA

Table 3. PINOUT DESCRIPTION

Pinout Category	Pinout Name(s)	Pinout Direction	Correspondent Ball(s)	Ball(s) Total	Note(s)
Host Output	PIXCLK	Output	M10	1	• Host pixel clock output
	FRAME_VALID	Output	L8	1	• Host frame valid output (synchronous to PIXCLK)
	LINE_VALID	Output	M8	1	• Host line valid output (synchronous to PIXCLK)
	META_LINE_VALID	Output	L10	1	• Line valid signal to indicate when Metadata is valid • There is an option to allow META_LINE_VALID to be reflected in LINE_VALID
	DOUT[23:0]	Output	K9, M9, K10, H10, K7, J10, G11, G10, F11, F10, E11, E10, D10, C10, B10, D11, B8, C12, C9, C7, C11, A10, A7, A9	24	• Host pixel data output (synchronous to PIXCLK)
	FRAME_SYNC	Input	K8	1	• Pass through to TRIGGER_OUT • This signal should be connected to GND if not used
	TRIGGER_OUT	Output	L11	1	• Host Trigger signal to embedded image sensor
	FLASH	Output	H1	1	• External Flash Light Control Output
Special Pins	NC	DO NOT CONNECT	B3, C2, C4, D1, D2, L1, M1 to M7, M11	14	• ON Internal Monitor Function Only
	Reserved	DO NOT CONNECT	G12	1	• ON Internal Debug Only
	PU_1	I/O	F1, G2	2	• Embedded Image Sensor Two−Wires Pins (for Stack Chip internal communication) • Recommended 1.5 KΩ to 1V8_IO
	PD_1	I/O	B12, E1, E2, J3, L6, L9, L12	7	• Must be at Logic Low for proper Stack Chip Operation • Recommended 10 KΩ to GND
	PD_2	I/O	H2, J1, K1, M12	4	• Pull down to GND for proper Stack Chip Operation • Recommended 1 KΩ to GND

Table 4. PACKAGE PINOUT

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VDD_1V8	VAA_2V8	VAA_2V8	VAA_2V8	LDO_1V2	LDO_1V2	DOUT1	EXT_REG	DOUT0	DOUT2	VDD_1V2	VDD_1V2	A
B	VDD_1V8	VDD_1V8	NC	REG_1V8	REG_1V8	LDO_1V2	XTAL	DOUT7	ENLDO	DOUT9	VDD_1V2	PD_1	B
C	1V8_PHY	NC	NO BALL	NC	REG_1V8	2V8_PHY	DOUT4	EXTCLK	DOUT5	DOUT10	DOUT3	DOUT6	C
D	NC	NC	1V8_IO	DGND	DGND	DGND	DGND	DGND	DGND	DOUT11	DOUT8	1V8/2V8/3V3_IO	D
E	PD_1	PD_1	1V8_IO	DGND	DGND	DGND	DGND	DGND	DGND	DOUT12	DOUT13	1V8/2V8/3V3_IO	E
F	PU_1	RESET_BAR	SPI_CS_BAR	DGND	DGND	DGND	DGND	DGND	DGND	DOUT14	DOUT15	1V8/2V8/3V3_IO	F
G	SCLK	PU_1	SPI_SCLK	DGND	DGND	DGND	DGND	DGND	DGND	DOUT16	DOUT17	RESERVED	G
H	FLASH	PD_2	STANDBY	DGND	DGND	DGND	DGND	DGND	DGND	DOUT20	AGND	AGND	H
J	PD_2	GPIO_5	PD_1	DGND	DGND	DGND	DGND	DGND	DGND	DOUT18	AGND	AGND	J
K	PD_2	SDATA	SADDR	GPIO_2	GPIO_1	GPIO_4	DOUT19	FRAME_SYNC	DOUT23	DOUT21	AGND	AGND	K
L	NC	GPIO_6	SPI_SDO	SPI_SDI	OTPM_2V8	PD_1	GPIO_3	FRAME_VALID	PD_1	META_LINE_VALID	TRIGGER_OUT	PD_1	L
M	NC	NC	NC	NC	NC	NC	NC	LINE_VALID	DOUT22	PIXCLK	NC	PD_2	M
	1	2	3	4	5	6	7	8	9	10	11	12	

ON−CHIP REGULATOR

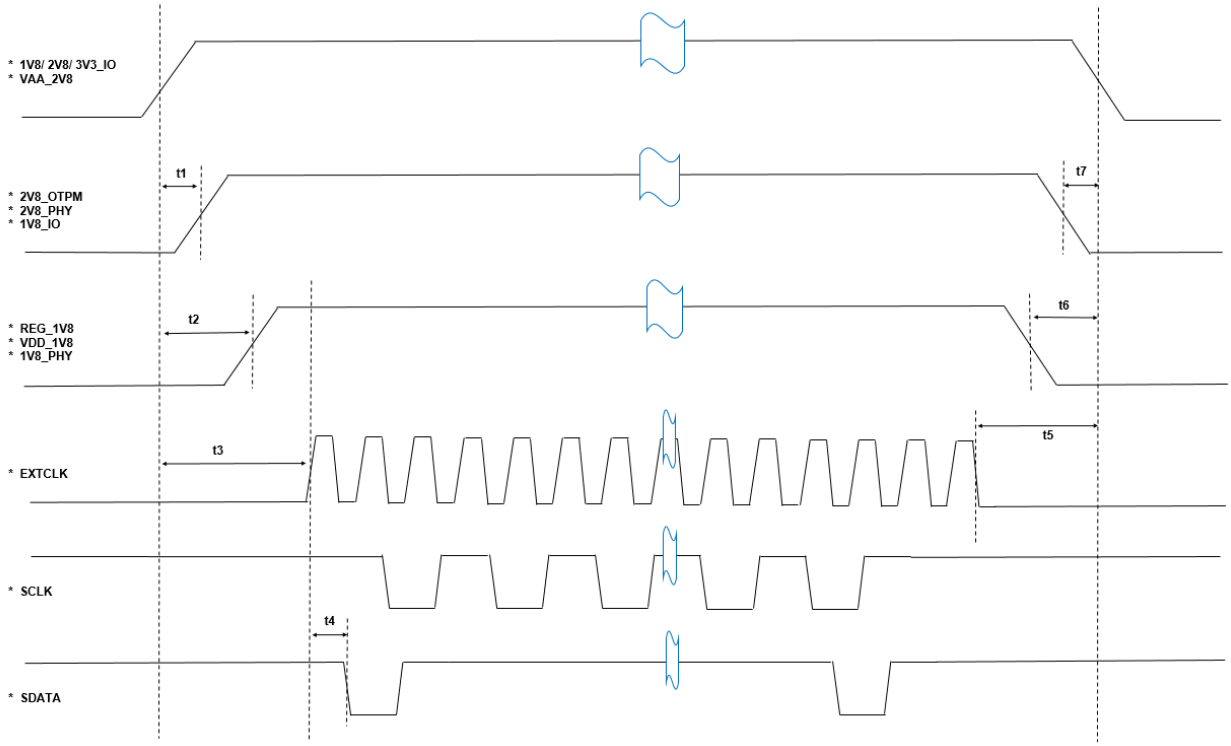
The AS0142AT has an on−chip regulator that outputs 1.2 V target voltage. The regulator should only be used to power AS0142AT internal core. It is also possible to bypass the regulator and provide power to relevant AS0142AT internal core that needs 1.2 V. The following table summarizes the configuration of using or bypassing AS0142AT internal regulator.

Table 5. AS0142AT REGULATOR MODE CONFIGURATION

Pinout Name	Internal Regulator	External Regulator
REG_1V8	1.8 V Nominal	Tied to 1V8/2V8/3V3_IO
ENLDO	Tied to REG_1V8	Tied to GND
EXT_REG	GND	Tied to 1V8/2V8/3V3_IO
LDO_1V2	1.2 V nominal (Output)	Floating (No Connection)
VDD_1V2	Tied with LDO_1V2	External 1.2 V Nominal Supply

POWER−UP SEQUENCE

Powering up the AS0142AT requires voltages to be applied in a particular order, as seen in Figure 5. The timing requirements are shown in Table 6. The AS0142AT includes a power−on reset feature that initiates a reset upon power up.



1. When using XTAL the setting should be taken into account.
2. RESET_BAR can be either @ 1V8/2V8/3V3_IO or GND at power−up.

Figure 5. Power−Up and Power−Down Sequence (AS0142AT Internal Regulator Mode)

Table 6. POWER−UP AND POWER−DOWN SIGNAL TIMING (AS0142AT INTERNAL REGULATOR MODE)

Symbol	Parameter	MIN	TYP	MAX	Unit
t1	Delay from 1V8/2V8/3V3_IO and VAA_2V8 to 2V8_OTPM, 2V8_PHY, and 1V8_IO	0	0.1	50	mS
t2	Delay from 1V8/2V8/3V3_IO and VAA_2V8 to REG_1V8, VDD_1V8, and 1V8_PHY	0	0.1	50	mS
t3	EXTCLK activation	t2 + 1	–	–	mS
t4	First serial command[1]	100	–	–	EXTCLK CYCLES
t5	EXTCLK cutoff	t6	–	–	mS
t6	Delay from REG_1V8, VDD_1V8, and 1V8_PHY to 1V8/2V8/3V3_IO and VAA_2V8	0	–	50	mS
t7	Delay from 2V8_OTPM, 2V8_PHY, and 1V8_PHY to 1V8/2V8/3V3_IO and VAA_2V8	0	–	50	mS
dv/dt	Power supply ramp up time (slew rate), from GND to full rail voltage	–	–	0.1	V/ uS

NOTE: When using XTAL the settling time should be taken into account

RESET AND STANDBY MODES

RESET

The AS0142AT has three types of reset available:

- A hard reset is issued by toggling the RESET_BAR signal
- A soft reset is issued by writing commands through the two−wire serial interface
- An internal power−on reset

Table 7 shows the output states when the part is in various states.

Table 7. OUTPUT STATES

Name	Hardware States		Firmware States				Notes
	Reset State	Default State	Hard Standby	Soft Standby	Streaming	Idle	
EXTCLK	(clock running or stopped)	(clock running)	(clock running or stopped)	(clock running)	(clock running)	(clock running)	Input
XTAL	n/a	n/a	n/a	n/a	n/a	n/a	Input
RESET_BAR	(asserted)	(negated) Internal pull− up enabled	(negated)	(negated)	(negated)	(negated)	Input. Internal pull up permanently enabled on die pad.
SCLK	n/a	n/a	(clock running or stopped)	(clock running or stopped)	(clock running or stopped)	(clock running or stopped)	Input. Must always be driven to a valid logic level; external pull−up for two−wire protocol standard I/O connection.
SDATA	High− impedance	High− impedance	High− impedance	High− impedance	High− impedance	High− impedance	Input/Output. A valid logic level should be established by pull−up.
SADDR	n/a	n/a	n/a	n/a	n/a	n/a	Input. Must always be driven to a valid logic level.
FRAME_SYNC	n/a	n/a	n/a	n/a	n/a	n/a	Input. Must always be driven to a valid logic level.
STANDBY	n/a	(negated)	(asserted)	(negated)	(negated)	(negated)	Input. Must always be driven to a valid logic level.
EXT_REG	n/a	n/a	n/a	n/a	n/a	n/a	Input. Must always be driven to a valid logic level that is compliment to ENLDO logic level.
ENLDO	n/a	n/a	n/a	n/a	n/a	n/a	Input. Must be tied to VDD_REG or GND.
SPI_SCLK	High− impedance	driven, logic 0	driven, logic 0	driven, logic 0			Output
SPI_SDI	Internal pull− up enabled	Internal pull− up enabled	Internal pull−up enabled	internal pull−up enabled			Input. Internal pull up permanently enabled on die pad.
SPI_SDO	High− impedance	driven, logic 0	driven, logic 0	driven, logic 0			Output
SPI_CS_BAR	High− impedance	driven, logic 1	driven, logic 1	driven, logic 1			Output
FRAME_VALID, LINE_VALID, META_LINE_VALID, PIXCLK, DOUT[23:0]	High− impedance	Varied	Driven if used	Driven if used	Driven if used	Driven if used	Output. Default state dependent on configuration.
GPIO[6:1]	High− impedance	Input, then high− impedance	Driven if used	Driven if used	Driven if used	Driven if used	Input/ Output.
TRIGGER_OUT	High− impedance	High− impedance	Driven if used	Driven if used	Driven if used	Driven if used	Output
FLASH	High− impedance	driven, logic 0	driven, logic 0	driven, logic 0	Driven if used	Driven if used	Output

HARD RESET

The AS0142AT enters the reset state when the external RESET_BAR signal is asserted LOW (voltage level), as shown in Figure 6. All output signals will be in a High−Z state. AS0142AT settings will not be preserved.

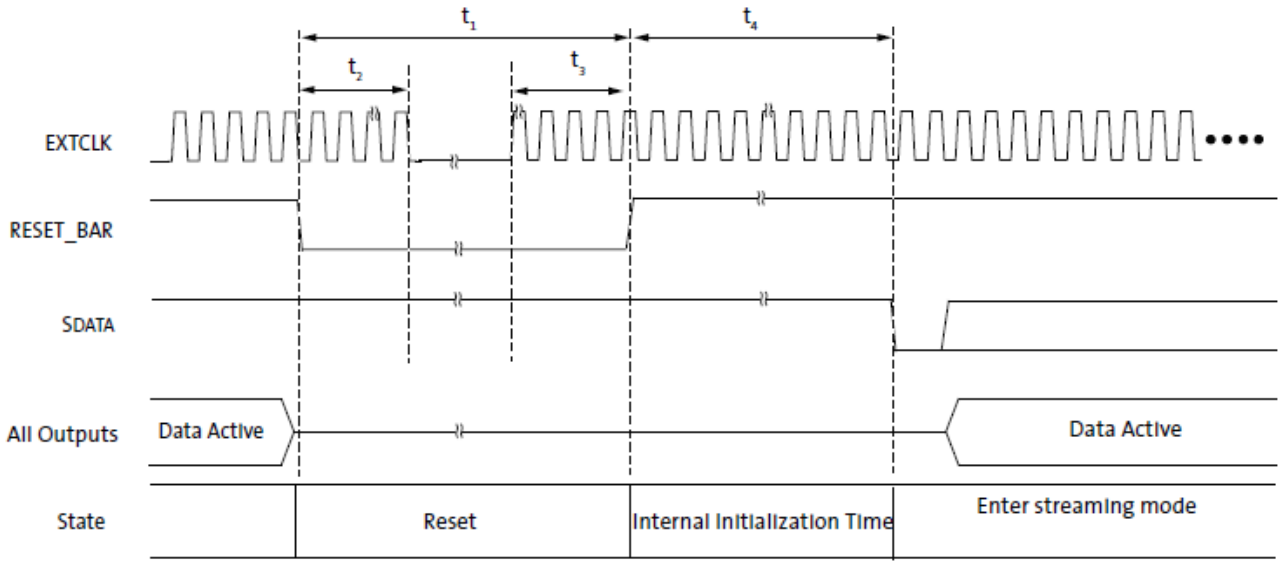


Figure 6. Hard Reset Operation

Table 8. HARD RESET

Symbol	Definition	Min	Typ	Max	Unit
t_1	RESET_BAR pulse width	50	–	–	EXTCLK CYCLES
t_2	Active EXTCLK required after RESET_BAR asserted	10	–	–	
t_3	Active EXTCLK required before RESET_BAR de− asserted	10	–	–	
t_4	First two−wire serial interface communication after RESET is HIGH	100	–	–	

SOFT RESET

A soft reset sequence to AS0142AT can be activated by writing to a register through the two−wire serial interface.

AS0142AT settings will not be preserved.

HARD STANDBY

The AS0142AT enters hard standby mode by using external STANDBY signal, as shown in Figure 7. In hard standby mode, the total power consumption is reduced. In this mode, the AS0142AT is switched off. Further power reduction can be achieved by turning off the EXTCLK, but this must be restored before de−asserting the STANDBY pin to LOW (voltage) state to restart the device. AS0142AT settings could be preserved.

Entering Standby Mode

Assert STANDBY signal HIGH (voltage level)

Exiting Standby Mode

De−assert STANDBY signal LOW (voltage level)

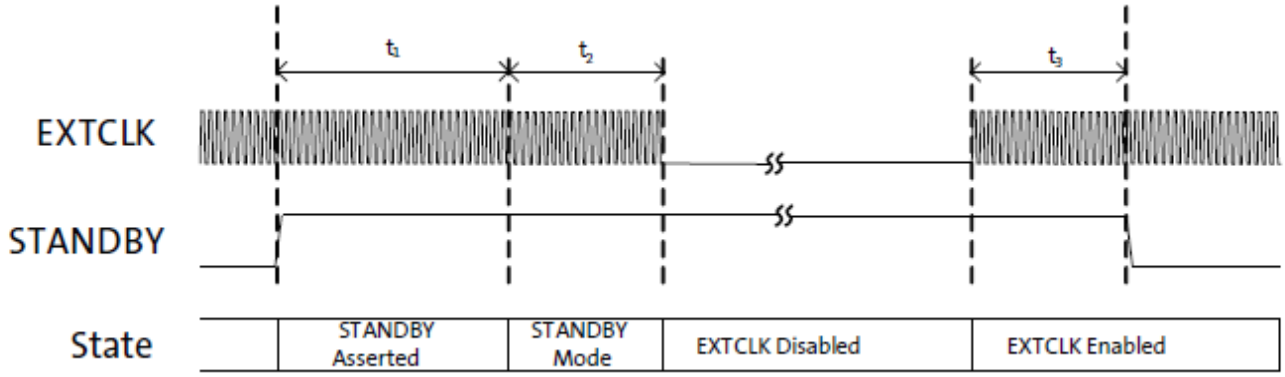


Figure 7. Hard Standby Operation

Table 9. HARD STANDBY SIGNAL TIMING

Symbol	Parameter	Min	Typ	Max	Unit
t1	Standby entry complete	–	–	2 Frames	Lines
t2	Active EXTCLK required after going into STANDBY mode	10	–	–	EXTCLKs
t3	Active EXTCLK required before STANDBY de−asserted	10	–	–	EXTCLKs

SOFT STANDBY

A soft standby sequence to AS0142AT can be activated by writing to a register through the two−wire serial interface.

AS0142AT settings could be preserved.

DEVICE CONFIGURATION

After power is applied and the device is out of reset (either the power on reset, hard or soft reset), it will enter a boot sequence to configure its operating mode. There are essentially three configuration modes: Flash/EEPROM Config, Auto Config, and Host Config.

The AS0142AT firmware supports a System Configuration phase at start−up. This consists of two sub−groups of execution:

Flash detection, then one of the following:

a. Flash Config

b. Auto Config

c. Host Config

The System Configuration phase is entered immediately following power−up or reset. Firmware will then performs Flash Detection that attempts to detect the presence of an SPI Flash or EEPROM device:

- If a device is detected, the firmware switches to the Flash−Config mode.
- If no device is detected, the firmware then samples the SPI_SDI pin state to determine the next mode:
  - If SPI_SDI is low, then it enters the Host−Config mode.
  - If SPI_SDI is high, then it enters the Auto−Config mode.

In the Flash Config mode, the firmware interrogates the device to determine if it contains valid configuration records:

- If no records are detected, then the firmware enters the Host Config mode.
- If records are detected, the firmware processes them. By default, when all Flash records are processed the firmware switches to the Host−Config mode. However, the records encoded into the Flash can optionally be used to instruct the firmware to proceed to Auto Config, or to start streaming (via a Change−Config).

In the Host Config mode, the firmware performs no configuration, and remains idle waiting for configuration and commands from the host. The System Configuration phase is effectively complete and the AS0142AT will take no actions until the host issues commands.

USAGE MODES

How a camera based on the AS0142AT will be configured depends on what features are used. In the simplest case, an AS0142AT operating in Auto−Config mode with no customized settings might be sufficient.

A back−up camera with dynamic input from the steering system will require a μC with a system bus interface. Flash sizes supported up to 2 GB. The two−wire bus is adequate since only high−level commands are used.

In the simplest case no EEPROM or Flash memory or μC is required, as shown in Figure 8.

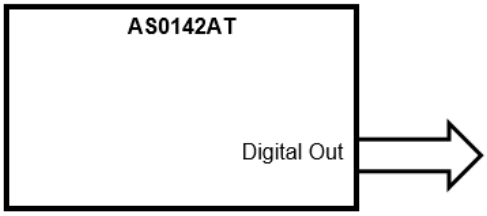


Figure 8. Auto Mode

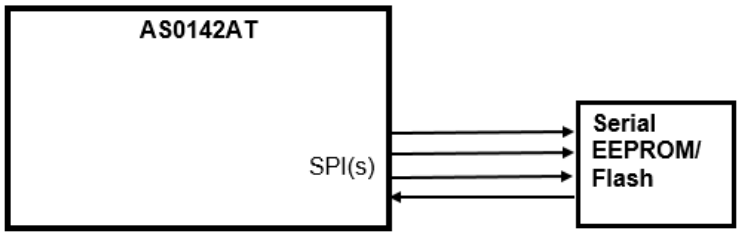


Figure 9. Flash Mode

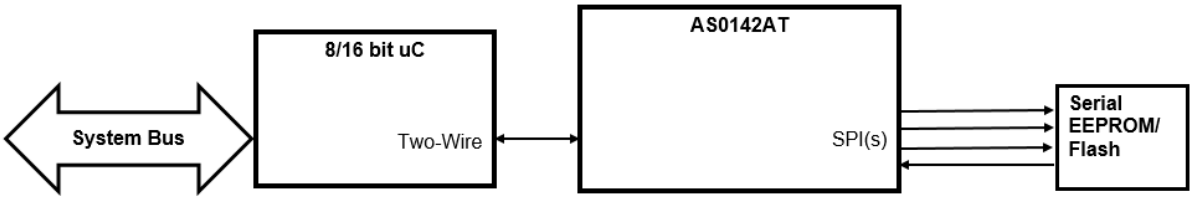


Figure 10. Host Mode with Flash

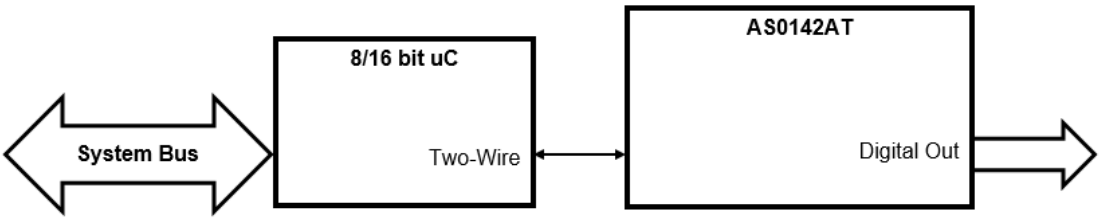


Figure 11. Host Mode

IMAGE FLOW PROCESSOR

Image and color processing in the AS0142AT is implemented as an image flow processor (IFP) coded in hardware logic. During normal operation, the embedded microcontroller will automatically adjust the operating parameters. For normal operation of the AS0142AT, streams of raw image data from the embedded image sensor are fed into the color pipeline. In addition, AS0142AT has the option to select from a number of build in test patterns to be input instead of sensor array data.

DEFECT CORRECTION

Image stream processing commences with the defect correction function immediately after data decompanding.

To obtain defect free images, the pixels marked defective during sensor readout and the pixels determined defective by the defect correction algorithms are replaced with values derived from the non−defective neighboring pixels.

ADACD (ADAPTIVE COLOR DIFFERENCE)

The next step in the image stream process is noise reduction. The AS0142AT uses a noise reduction filter called AdaCD which focuses on removing color noise while preserving edge details. Automotive applications require good performance in extremely low light, even at high temperature conditions. In these stringent conditions the image sensor is prone to higher noise levels. Efficient noise reduction techniques are required to circumvent this sensor limitation and deliver a high quality image.

BLACK LEVEL SUBTRACTION AND DIGITAL GAIN

After noise reduction, the pixel data goes through black level subtraction and multiplication by a programmable digital gain. This digital gain can be programmed independently per color channel registers. Black level subtraction (to compensate for sensor data pedestal) is a single value applied to all color channels. If the black level subtraction produces a negative result for a particular pixel, the value of this pixel is set to 0.

POSITIONAL GAIN ADJUSTMENTS (PGA)

Lens has tendency to produce images whose brightness is significantly attenuated near the edges. On top of other factors causing fixed pattern signal gradients in images captured by image sensors, image shading occurs. The AS0142AT has an embedded shading correction module that can be programmed to counter the shading effects on each individual R, Gb, Gr, and B color signal.

THE CORRECTION FUNCTION

The correction functions can then be applied to each pixel value to equalize the response across the image as per following relation:

$$P_{corrected}(row, col) = P_{sensor}(row, col) \times f(row, col) \quad \text{(eq. 1)}$$

where P is the pixel value and f is the color dependent correction functions for each color channel.

ADAPTIVE LOCAL TONE MAPPING (ALTM)

Real world scenes often have very high dynamic range (HDR) that far exceeds the electrical dynamic range of the imager. Dynamic range is defined as the luminance ratio between the brightest and the darkest object in a scene. In recent years many technologies have been developed to capture the full dynamic range of real world scenes. For example, the multiple exposure method is widely adopted for capturing high dynamic range images, which combines a series of low dynamic range images of the same scene taken under different exposure times into a single HDR image.

Even though the new digital imaging technology enables the capture of the full dynamic range, low dynamic range display devices can be the limiting factor. Typical LCD monitor nowaday has contrast ratio around 1,000:1 which is not enough for an HDR image (the contrast ratio for an HDR image is around 250,000:1). Therefore, in order to reproduce HDR images on a low dynamic range display device, the captured high dynamic range must be compressed to the available range of the display device. This is commonly called tone mapping.

Tone mapping methods can be classified into global tone mapping and local tone mapping. Global tone mapping methods apply the same mapping function to all pixels. While global tone mapping methods provide computationally simple and easy to use solutions, they often cause loss of contrast and detail. A local tone mapping is thus necessary in addition to global tone mapping, for the reproduction of visually higher appealing images that could reveal scene details which are important for automotive safety and surveillance applications. Local tone mapping methods use a spatially variable mapping function determined by the neighborhood of a pixel, which allows it to increase the local contrast and the visibility of some details of the image. Local methods usually yield more pleasing results because they exploit the fact that human vision is more sensitive to local contrast.

ON Semiconductor's ALTM solution significantly improves the performance over global tone mapping. ALTM is directly applied to the Bayer domain to compress the dynamic range from 20-bit to 12−bit. This allows the regular color pipeline to be used for HDR image rendering.

COLOR INTERPOLATION

In the raw data stream fed by the embedded sensor to the IFP, each pixel is represented by a 20− or 12−bit integer number, which can be considered proportional to the pixel's response to a one−color light stimulus, red, green, or blue, depending on the pixel's position under the color filter array. Initial data processing steps, up to and including ALTM, preserve the one−color−per−pixel nature of the data stream, but after ALTM it must be converted to a three−colors−per−pixel stream appropriate for standard color processing. The conversion is done by an edge sensitive color interpolation module. The module pads the incomplete color information available for each pixel with information extracted from an appropriate set of neighboring pixels. The algorithm used to select this set and extract the information seeks the best compromise between preserving edges and filtering out high frequency noise in flat field areas. The edge threshold can be set through register settings.

COLOR CORRECTION AND APERTURE CORRECTION

To achieve good color fidelity of the IFP output, interpolated RGB values of all pixels are subjected to color correction. The IFP multiplies each vector of three pixel colors by a 3 x 3 color correction matrix. The three components of the resulting color vector are all sums of three 10−bit numbers. The color correction matrix (CCM) can be either programmed by the user or automatically selected by the auto white balance (AWB) algorithm implemented in the IFP. Color correction should ideally produce output colors that are corrected for the spectral sensitivity and color

crosstalk characteristics of the image sensor. The optimal values of the color correction matrix elements depend on those sensor characteristics and on the spectrum of light incident on the sensor. The color correction variables can be adjusted through register settings.

The AS0142AT offers a three sets of CCM solution that will give the user improved color fidelity over a wide range of lighting conditions.

To increase image sharpness, a programmable 2D aperture correction (sharpening filter) is applied to color−corrected image data. The gain and threshold for 2D correction can be defined through register settings.

GAMMA CORRECTION

The gamma correction curve is implemented as a piecewise linear function with 33 knee points, taking 12-bit arguments and mapping them to 10-bit output. The abscissas of the knee points are fixed at 0, 8, 16, 24, 32, 40, 48, 56, 64, 80, 96, 112, 128, 160, 192, 224, 256, 320, 384, 448, 512, 640, 768, 896, 1024, 1280, 1536, 1792, 2048, 2560, 3072, 3584, and 4096. The 10−bit ordinates are programmable through variables.

AS0142AT has the ability to calculate the 33−point knee points based on the tuning of CAM_LL_GAMMA and CAM_LL_CONTRAST_GRADIENT_BRIGHT. The other method is for the host to program the 33 knee point curve.

Also included in this block is a Fade−to Black curve which sets all knee points to zero and causes the image to go black in extreme low light conditions.

COLOR KILL

To remove high−or low−light color artifacts, a color kill circuit is included. It affects only pixels whose luminance exceeds a certain preprogrammed threshold. The U and V values of those pixels are attenuated proportionally to the difference between their luminance and the threshold.

YUV COLOR FILTER

As an optional processing step, noise suppression by one-dimensional low−pass filtering of Y and/or UV signals is possible. A 3− or 5-tap filter can be selected for each signal.

CAMERA CONTROL AND AUTO FUNCTIONS

AUTO EXPOSURE

The auto exposure algorithm optimizes scene exposure to minimize clipping and saturation in critical areas of the image. This is achieved by controlling exposure time and analog gains of the external sensor as well as digital gains applied to the image.

Auto exposure is implemented by a firmware algorithm that is running on the embedded microcontroller that analyzes image statistics collected by the exposure measurement engine, makes a decision, and programs the sensor and color pipeline to achieve the desired exposure. The measurement engine subdivides the image into 25 windows organized as a 5 x 5 grid.

W 0,0	W 0,1	W 0,2	W 0,3	W 0,4
W 1,0	W 1,1	W 1,2	W 1,3	W 1,4
W 2,0	W 2,1	W 2,2	W 2,3	W 2,4
W 3,0	W 3,1	W 3,2	W 3,3	W 3,4
W 4,0	W 4,1	W 4,2	W 4,3	W 4,4

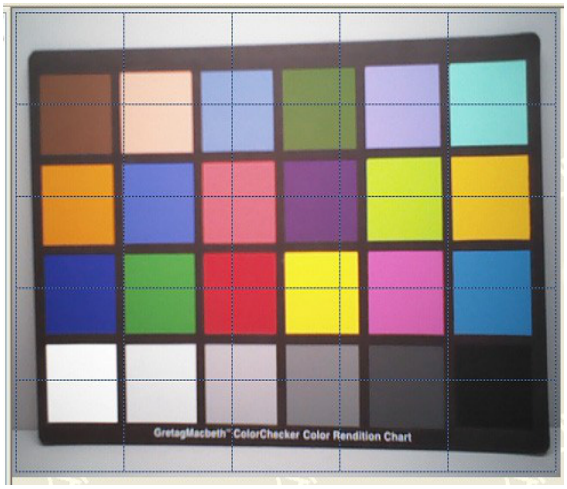


Figure 12. 5 x 5 Grid

AE TRACK

Other algorithm features include the rejection of fast fluctuations in illumination (time averaging), control of speed of response, and control of the sensitivity to small changes. While the default settings are adequate in most situations, the user can program target brightness, measurement window, and other parameters described above.

The AS0142AT changes AE parameters (integration time, gains, and so on) to drive scene brightness to the programmable target.

To avoid unwanted reaction of AE on small fluctuations of scene brightness or momentary scene changes, the AE uses a temporal filter for luma and a threshold around the AE luma target. The AE changes AE parameters only if the

filtered luma is larger than the AE target step and pushes the luma beyond the threshold.

AUTO WHITE BALANCE

The AS0142AT has a built−in AWB algorithm designed to compensate for the effects of changing spectra of the scene illumination on the quality of the color rendition. The algorithm consists of two major parts: a measurement engine performing statistical analysis of the image and a driver performing the selection of the optimal color correction matrix and IFP digital gain. While default settings of these algorithms are adequate in most situations, the user can reprogram base color correction matrices, place limits on color channel gains, and control the speed of both matrix and gain adjustments. The AS0142AT AWB displays the current AWB position in color temperature, the range of which will be defined when programming the CCM matrices.

The region of interest can be controlled through the combination of an inclusion window and an exclusion window.

DUAL BAND IRCF

For some applications a day/night filter would be switched in/out; this option adds cost to the camera system. The AS0142AT supports the use of dual band IRCF, which removes the need for switching day/night filter. Tuning support is provided for this usage case. Refer to the AS0142AT developer guide for details.

EXPOSURE AND WHITE BALANCE MODES

The AS0142AT supports auto and manual exposure and white balance modes. In addition, it will operate within synchronized multi-camera systems. In multi−camera use case, one camera within the system will be the ’master’, and the others ’slaves’. The master is used to calculate the appropriate exposure and white balance which are then applied to all slaves concurrently under host control.

Auto Mode

In Auto Exposure mode, the AE algorithm is responsible for calculating the appropriate exposure to keep the desired scene brightness, and for applying the exposure to the underlying hardware. In Auto White Balance mode, the AWB algorithm is responsible for calculating the color temperature of the scene and applying the appropriate red and blue gains to compensate.

Triggered Auto Mode

The Triggered Auto Exposure and Triggered Auto White Balance modes are intended for the multi−camera use cases, where a host is controlling the exposure and white balance of a number of cameras. The idea is that one camera is in triggered−auto mode (the master), and the others in host−controlled mode (slaves). The master camera must calculate the exposure and gains, the host then copies this to the slaves, and all changes are then applied at the same time.

Manual Mode

Manual mode is intended to allow simple manual exposure and white balance control by the host. The host needs to set the CAM_AET_EXPOSURE_TIME_MS, CAM_AET_EXPOSURE_GAIN and CAM_AWB_COLOR_TEMPERATURE controls and trigger an exposure; the camera will calculate the appropriate integration times and gains.

Host Controlled

The Host Controlled mode is intended to give the host full control over exposure and gains.

FLICKER AVOIDANCE

Flicker occurs when the integration time is not an integer multiple of the period of the light intensity. Flicker is caused by artificial light which is usually generated from incandescent or fluorescent light sources. The frequency of alternating current (AC) power sources in most countries is 50 Hz or 60 Hz, which emit light with alternating inverted positive and negative voltages. This results in a light source reflecting from an object to have a light intensity change frequency of 100 Hz and 120 Hz respectively. If the integration time is not an integer multiple of the period of AC powered light intensity, flicker can be visible. The AS0142AT can be programmed to avoid flicker for 50 or 60 Hz. For integration times below the light intensity period (10mS for 50 Hz environment, 8.33 ms in 60 Hz environments), flicker cannot be avoided. The AS0142AT supports an indoor AE mode that will ensure flicker-free operation.

FLICKER DETECTION

The AS0142AT supports flicker detection, the algorithm is designed only to detect a 50Hz or 60Hz flicker source.

OUTPUT FORMATTING

The pixel output data in AS0142AT will be transmitted as an 8− to 24−bit word over one or two clocks.

YCbCr DATA ORDERING

The AS0142AT supports swapping YCbCr mode, as illustrated in Table 10.

Table 10. YCbCr OUTPUT DATA ORDERING

Mode	Data Sequence			
Default (no swap)	Cbi	Yi	Cri	Yi+1
Swapped CrCb	Cri	Yi	Cbi	Yi+1
Swapped YC	Yi	Cbi	Yi+1	Cri
Swapped CrCb, YC	Yi	Cri	Yi+1	Cbi

The data ordering for the YCbCr output modes for AS0142AT are shown in Tables 11 and 12:

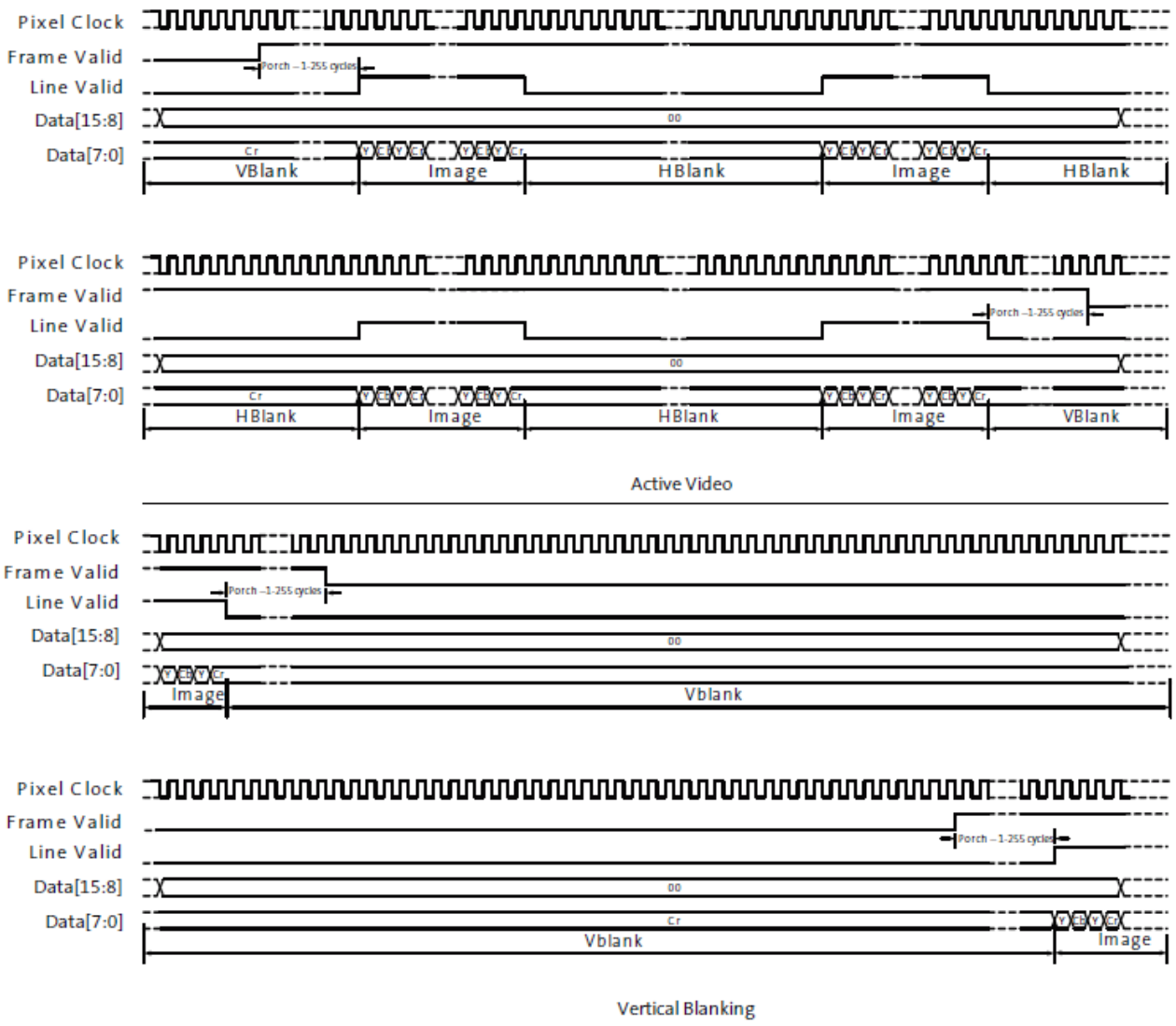
Table 11. YCbCr OUTPUT MODES (Default mode; CAM_PORT_PARALLEL_MSB_ALIGN = 0x1)

Mode	Byte	Pixel i	Pixel i+1	Notes
YCbCr_422_8_8	Odd (DOUT [23:16])	Cbi	Cri	Data range of 0-255 (Y=16-235 and C=16-240)
	Even (DOUT [23:16])	Yi	Yi+1	
YCbCr_422_10_10	Odd (DOUT [23:14])	Cbi	Cri	Data range of 0-1023 (Y=64−940 and C=64−960)
	Even (DOUT [23:14])	Yi	Yi+1	
YCbCr_422_16	Single (DOUT [23:8])	Cbi_Yi	Cri_Yi+1	Data range of 0-255 (Y=16-235 and C=16-240)
YCbCr_422_20	Single (DOUT [23:4])	Cbi_Yi	Cri_Yi+1	Data range of 0-1023 (Y=64−940 and C=64−960)

NOTE: Odd means first cycle; even means second cycle.

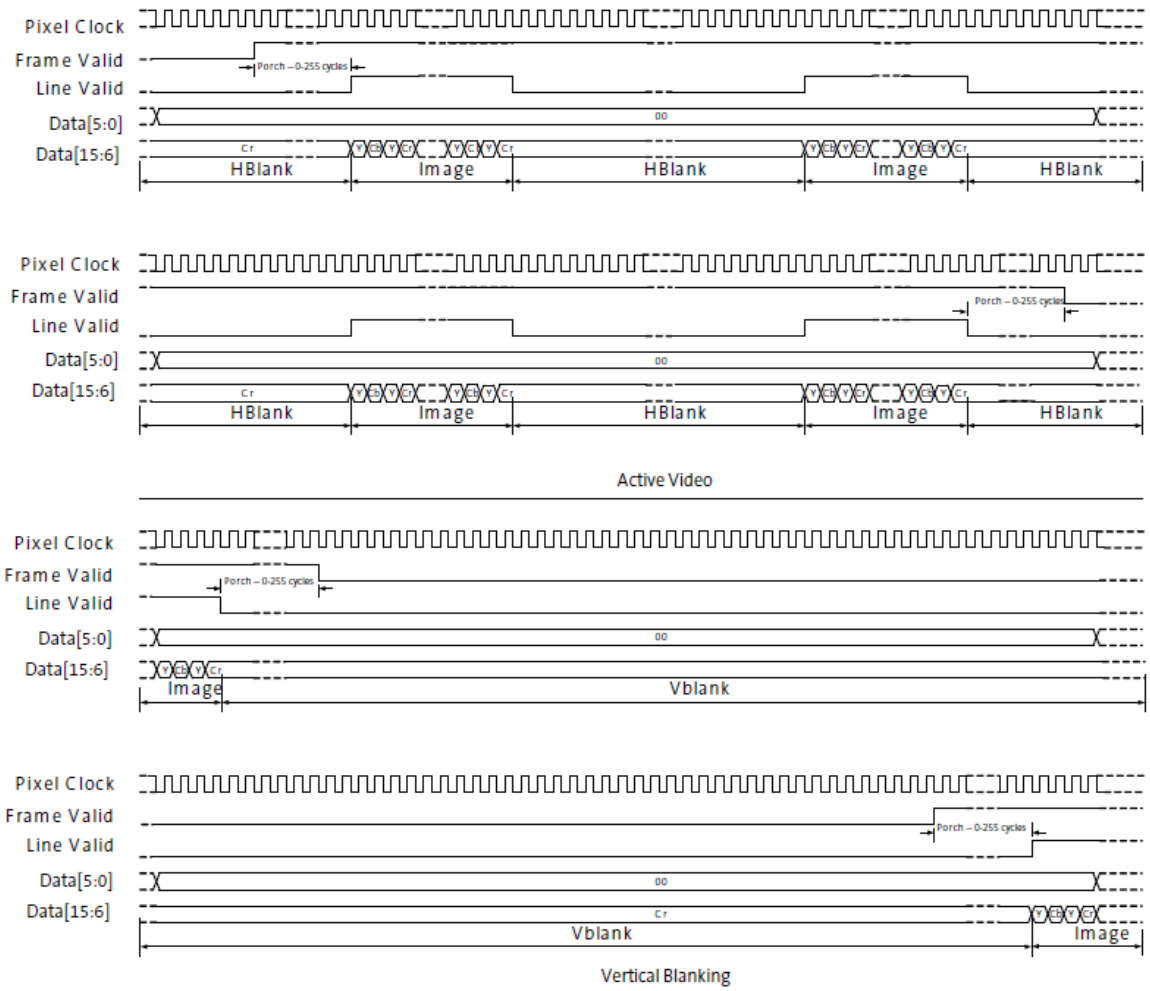
Table 12. YCbCr OUTPUT MODES (Default mode; CAM_PORT_PARALLEL_MSB_ALIGN = 0x0)

Mode	Byte	Pixel i	Pixel i+1	Notes
YCbCr_422_8_8	Odd (DOUT[7 :0])	Cbi	Cri	Data range of 0-255 (Y=16−235 and C=16-240)
	Even (DOUT [7:0]	Yi	Yi+1	
YCbCr_422_10_10	Odd (DOUT [9:0])	Cbi	Cri	Data range of 0-1023 (Y=64-940 and C=64-960)”
	Even (DOUT [9:0])	Yi	Yi+1	
YCbCr_422_16	Single (DOUT [15:0])	Cbi_Yi	Cri_Yi+1	Data range of 0-255 (Y=16−235 and C=16-240)
YCbCr_422_20	Single (DOUT [19:0])	Cbi_Yi	Cri_Yi+1	Data range of 0-1023 (Y=64-940 and C=64-960)



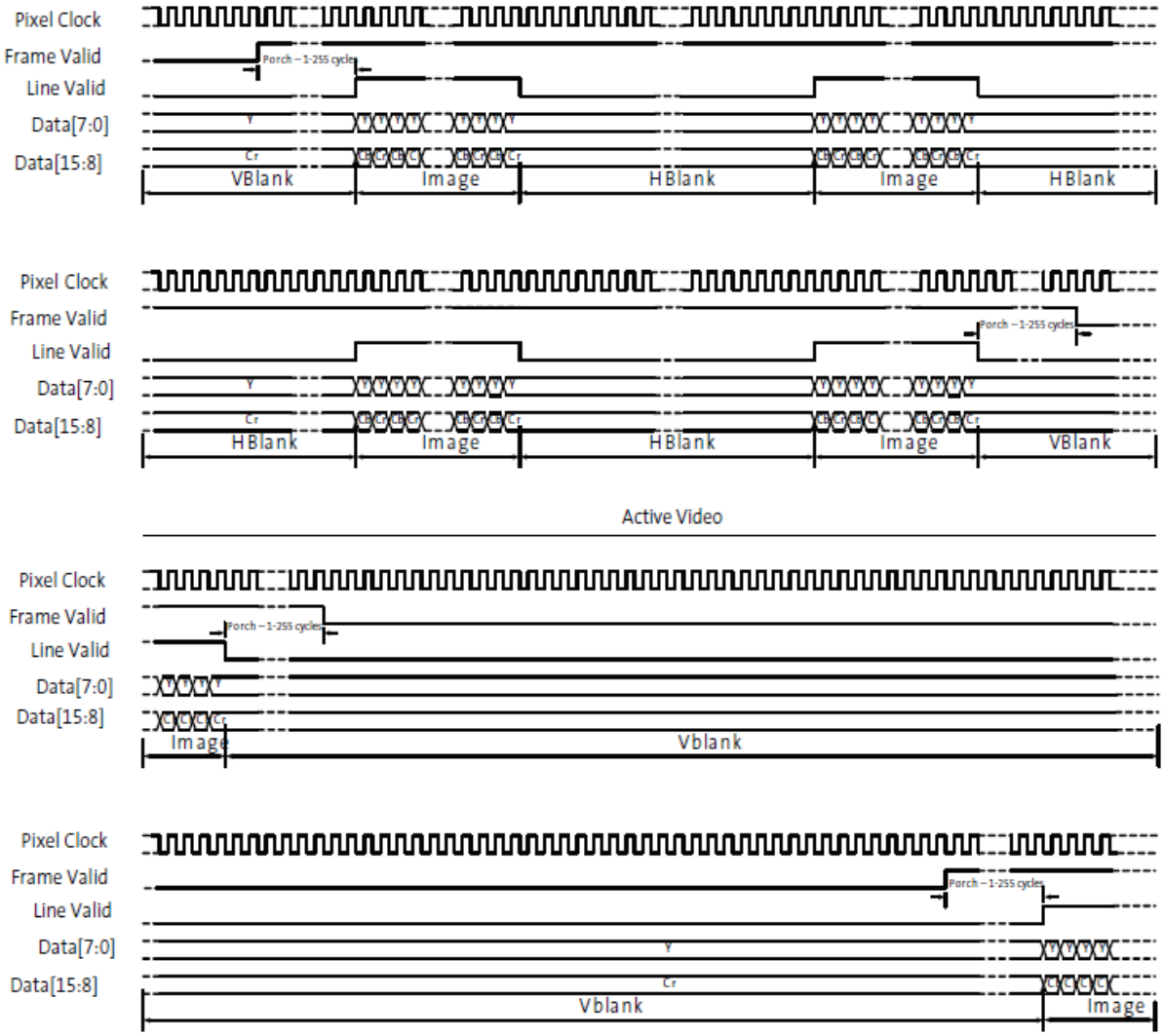
1. YC Swapped mode: YCbYCr
2. CAM_PORT_PARALLEL_MSB_ALIGN = 0x0

Figure 13. 8−bit YCbCr Output (YCbCr_422_8_8)



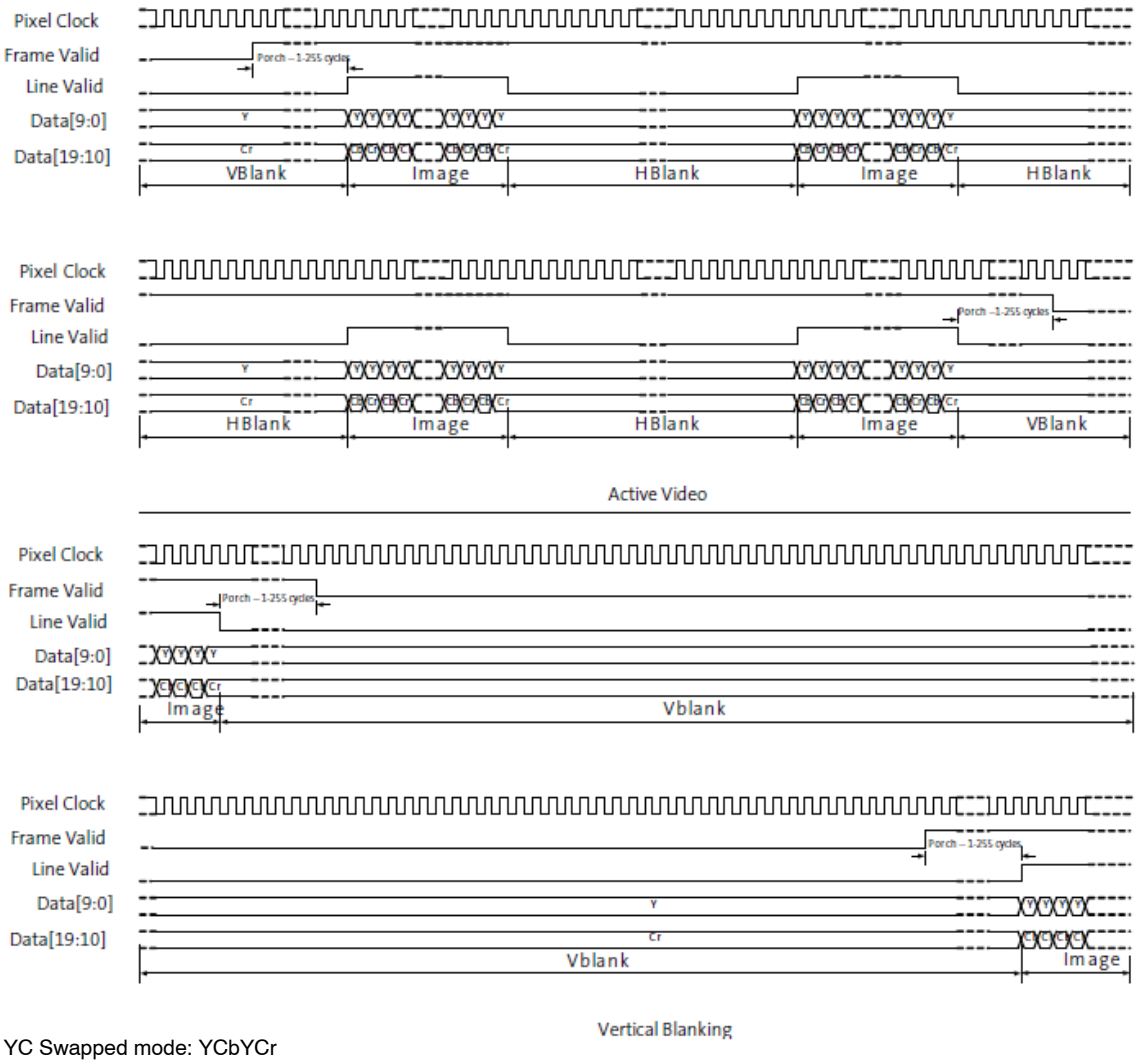
1. YC Swapped mode: YCbYCr
2. CAM_PORT_PARALLEL_MSB_ALIGN = 0x0

Figure 14. 10−bit YCbCr Output (YCbCr_422_10_10)



1. YC Swapped mode: YCbYCr
2. CAM_PORT_PARALLEL_MSB_ALIGN = 0x0

Figure 15. 16−bit YCbCr Output (YCbCr_422_16)



1. YC Swapped mode: YCbYCr
2. CAM_PORT_PARALLEL_MSB_ALIGN = 0x0

Figure 16. 20−bit YCbCr Output (YCbCr_422_20)

PROGRESSIVE CCIR656 (BT.656) DATA ORDERING

The AS0142AT supports progressive CCIR656 mode.

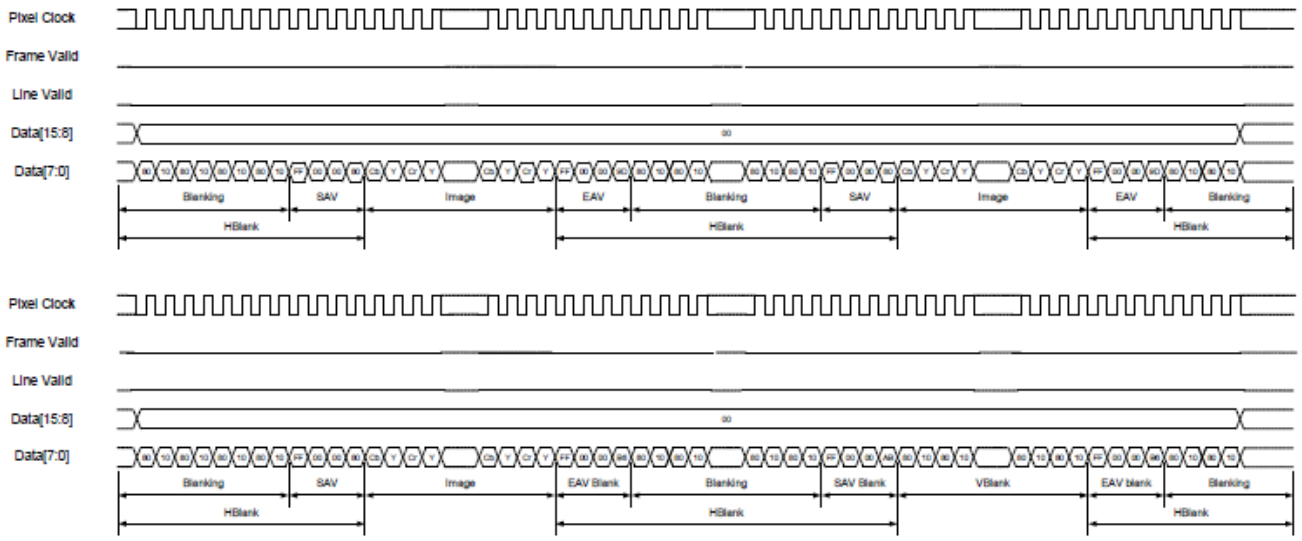


Figure 17. CCIR656 (Progressive) Output

RGB888 DATA ORDERING

The AS0142AT supports RGB888 output mode. The data ordering for this mode is shown in Tables 13 and 14:

Table 13. RGB888 OUTPUT MODES (CAM_PORT_PARALLEL_MSB_ALIGN = 0x01)

Mode	Byte	Pixel i	Pixel i+1	Notes
RGB888_12_12	Odd (DOUT [23:12])	Rm_Rl_Gm	Rm+1_Rl+1_Gm+1	
	Even (DOUT [23:12])	Gl_Bm_Bl	Gl+1_Bm+1_Bl+1	
RGB888_24	Single (DOUT [23:0])	R_G_B	R+1_G+1_B+1	

NOTE: Odd means first cycle; even means second cycle.

Table 14. RGB888 OUTPUT MODES (CAM_PORT_PARALLEL_MSB_ALIGN = 0x0)

Mode	Byte	Pixel i	Pixel i+1	Note
RGB888_12_12	Odd (DOUT[11:0])	Rm_Rl_Gm	Rm+1_Rl+1_Gm+1	
	Even (DOUT [11:0]	Gl_Bm_Bl	Gl+1_Bm+1_Bl+1	
RGB888_24	Single (DOUT [23:0])	R_G_B	R+1_G+1_B+1	

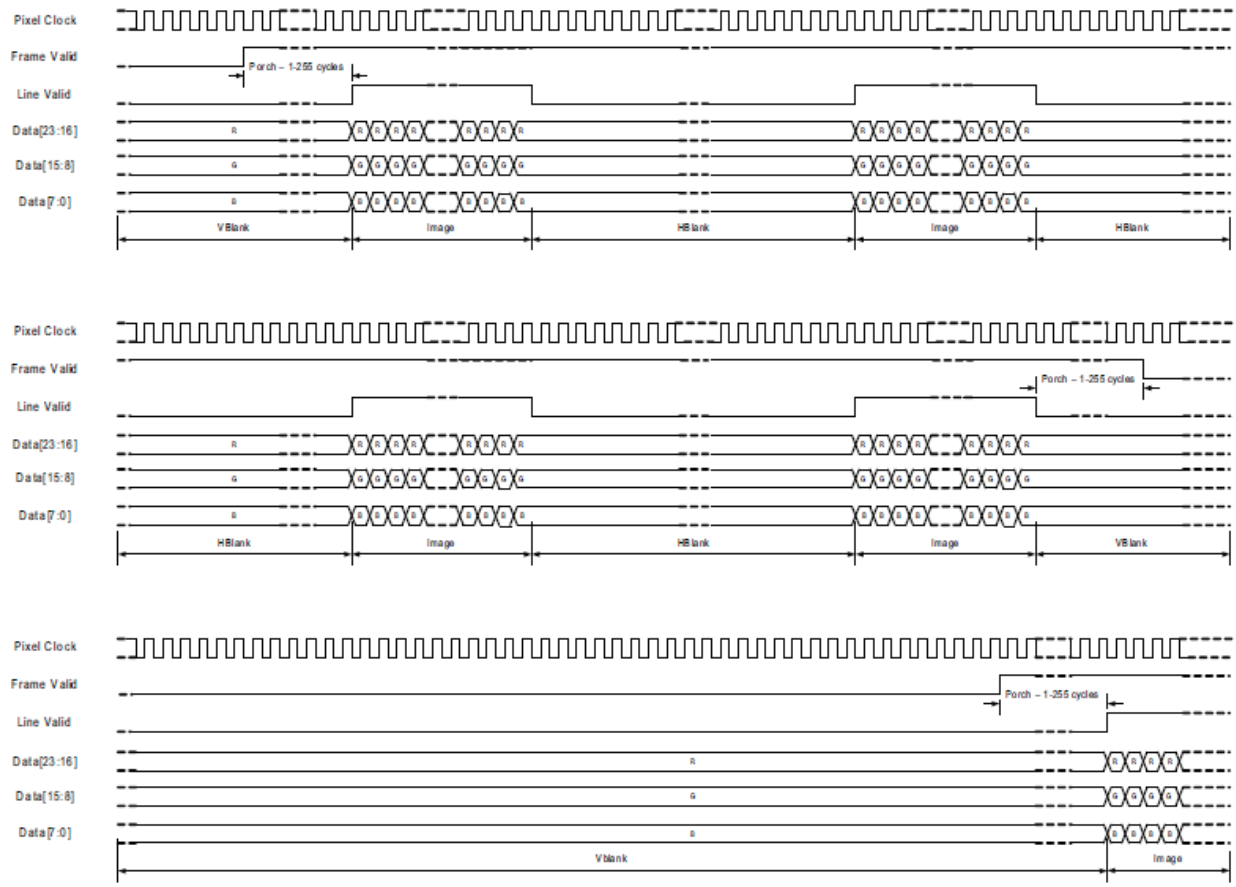


Figure 18. 24−bit RGB888 Output

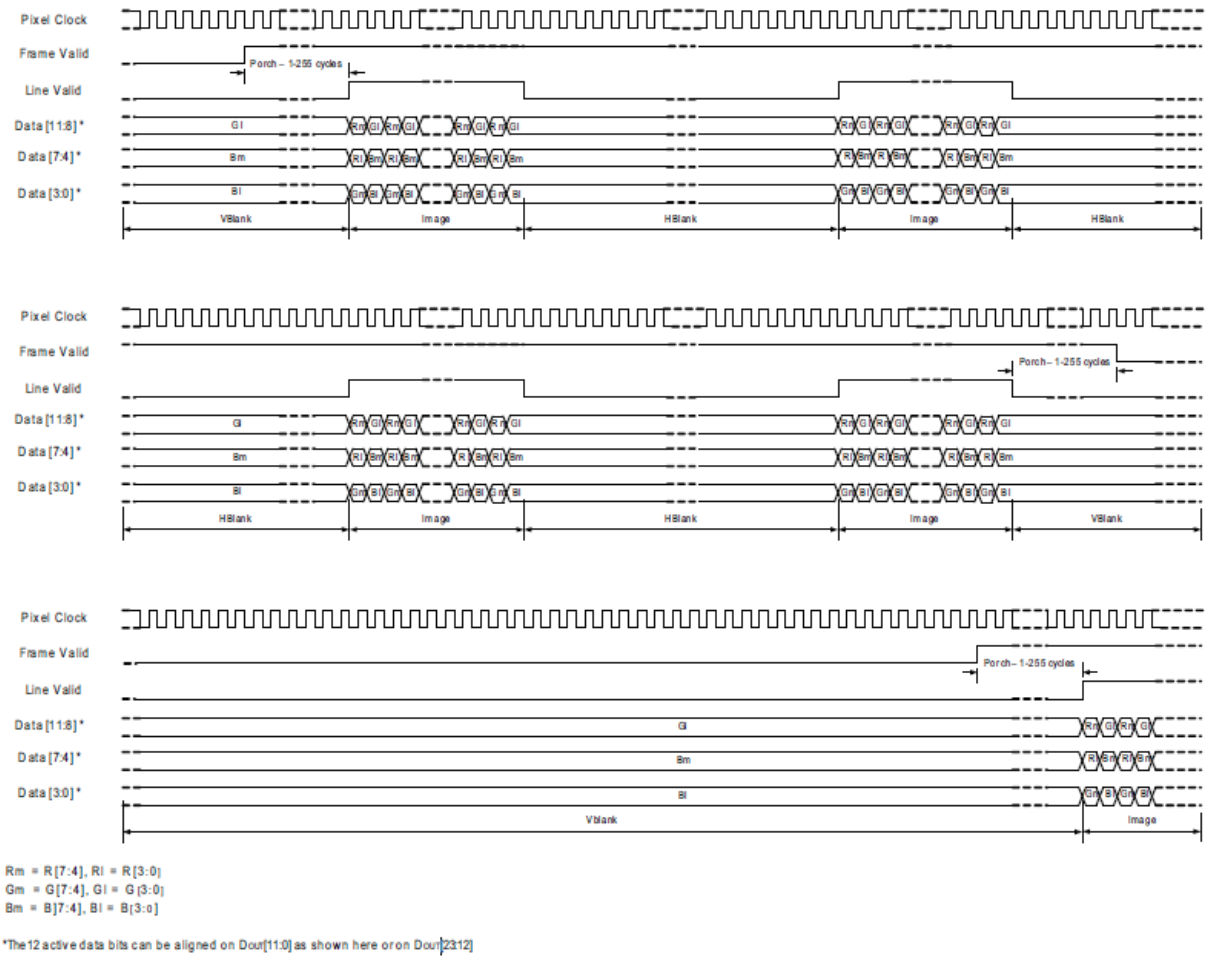


Figure 19. 12+12−bit RGB888 Output

RGB565 DATA ORDERING

The AS0142AT supports RGB565 output mode. The data ordering for this mode is shown in Tables 15 and 16:

Table 15. RGB565OUTPUT MODES (cam_port_parallel_msb_align=0x01)

Mode	Byte	Pixel i	Pixel i+1	Notes
RGB565_8_8	Odd (DOUT [23:16])	R_Gm	R+1_Gm+1	
	Even (DOUT [23:16])	Gl_B	Gl+1_B+1	
RGB565_16	Single (DOUT [23:8])	R_G_B	R+1_G+1_B+1	

NOTE: Odd means first cycle; even means second cycle.

Table 16. RGB565 OUTPUT MODES (cam_port_parallel_msb_align=0x0)

Mode	Byte	Pixel i	Pixel i+1	Note
RGB565_8_8	Odd (DOUT [7:0])	R_Gm	R+1_Gm+1	
	Even (DOUT [7:0])	Gl_B	Gl+1_B+1	
RGB565_16	Single (DOUT [15:0)	R_G_B	R+1_G+1_B+1	

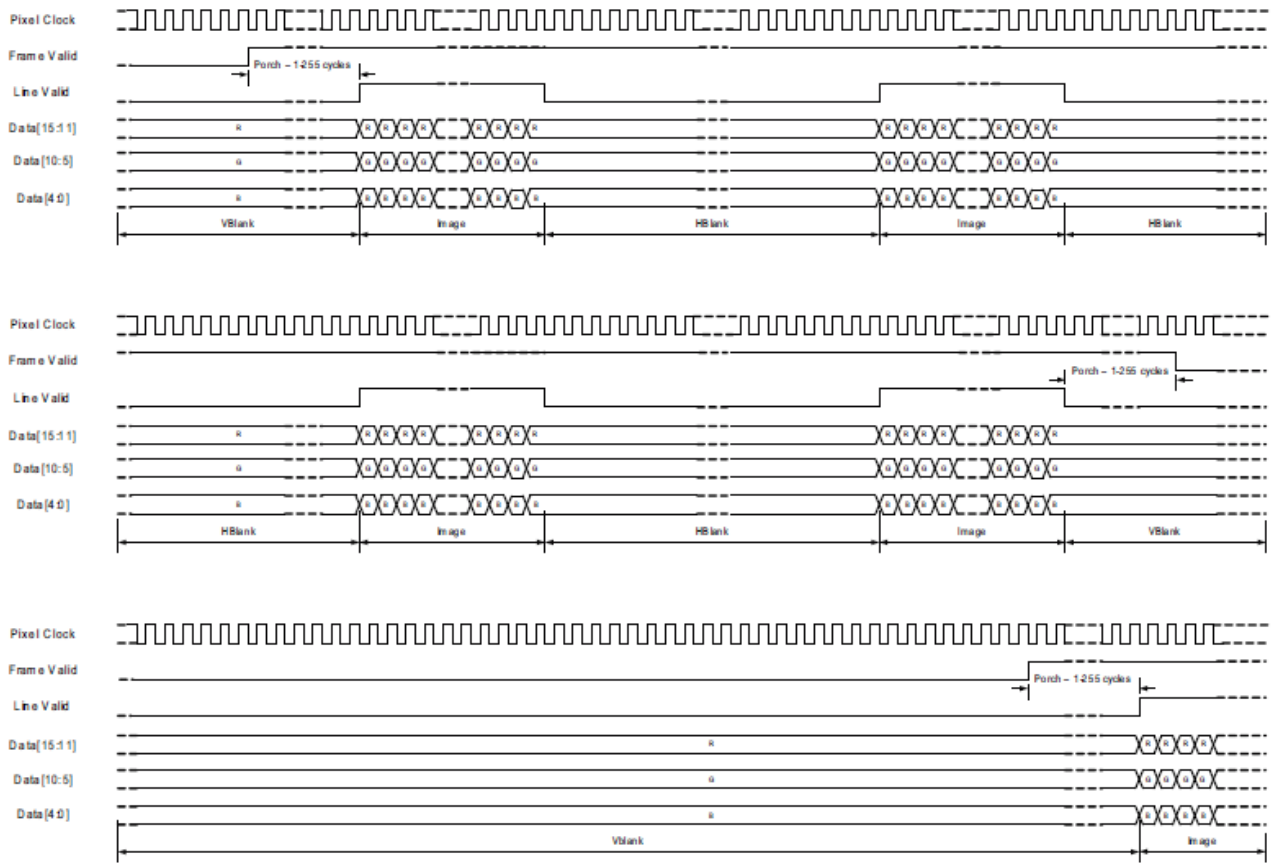


Figure 20. RGB565_16

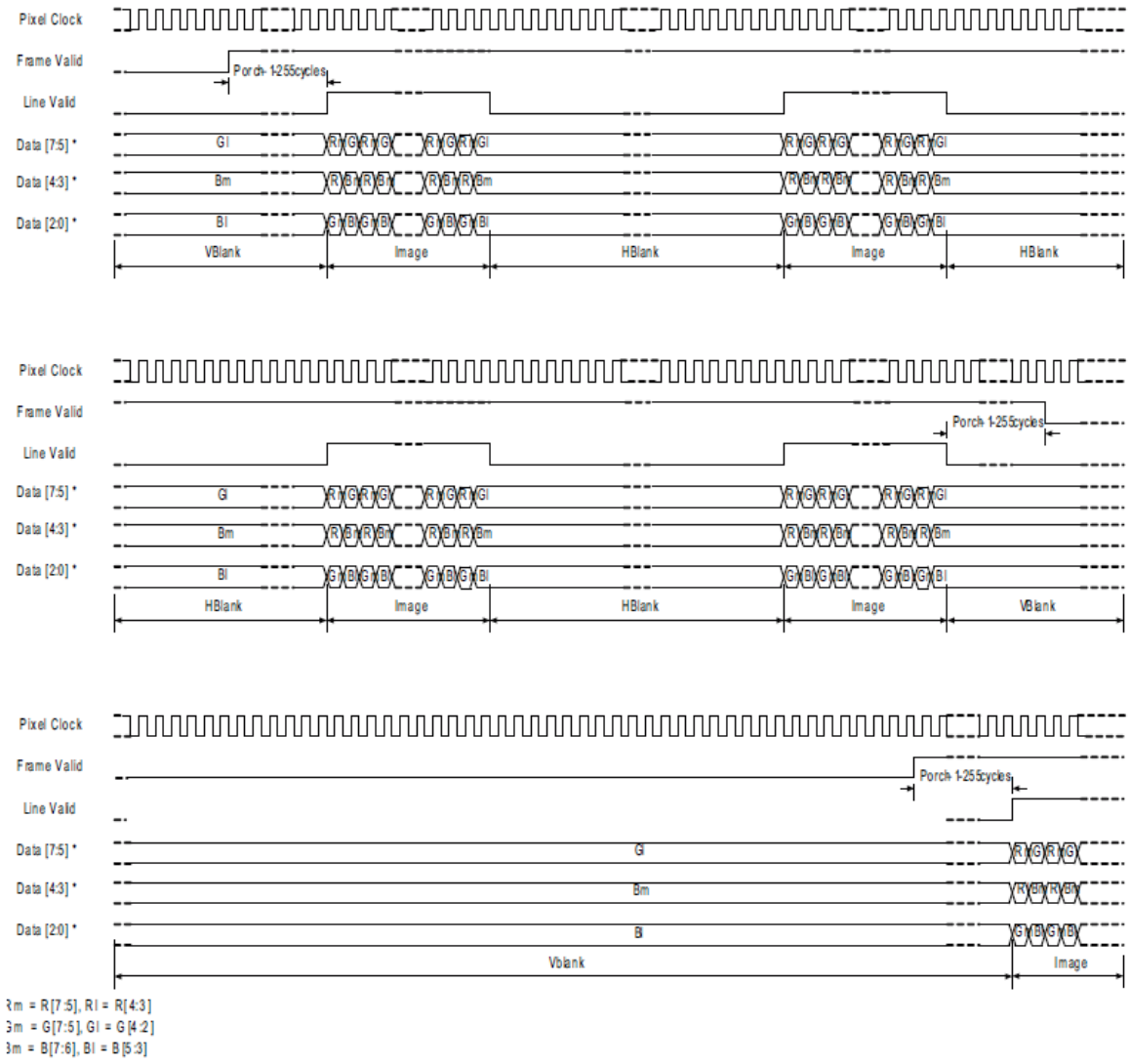


Figure 21. RGB565_8_8

BAYER MODES

The data ordering for the ALTM Bayer output modes for AS0142AT are shown in Table 17. Shown is LSB aligned data. It is possible using register settings to obtain MSB aligned data as well.

Table 17. ALTM BAYER OUTPUT MODES

Mode	Byte	D23– D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALTM_Bayer_10	Single	0	0	0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALTM_Bayer_12	Single	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

The data ordering for the 12/ 14/ 16/ 20bits Bayer output modes for AS0142AT are shown in shown in Tables 18, 19, 20, and 21. Shown is LSB-aligned data. It is possible using register setting to obtain MSB−aligned data as well.

Table 18. 12−bit BAYER OUTPUT MODE

Mode	Byte	D23– D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bayer_12	Single	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 19. 14−bit BAYER OUTPUT MODE

Mode	Byte	D23– D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bayer_14	Single	0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 20. 16−bit BAYER OUTPUT MODE

Mode	Byte	D23– D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bayer_16	Single	0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 21. 20−bit BAYER OUTPUT MODE

Mode	Byte	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bayer_20	Single	0	0	0	0	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bayer_16+4	Odd	0	0	0	0	0	0	0	0	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4
	Even	0	0	0	0	0	0	0	0	D3	D2	D1	D0	0	0	0	0	0	0	0	0	0	0	0	0

EMBEDDED DATA AND STATISTICS

AS0142AT embedded sensor supports a feature that, if enabled, inserts two extra lines at the beginning and end of each frame which contain information about that frame. The first two lines contain specific register values that were used to capture that frame. These values allow the host to know certain important things about how the sensor was configured for that frame, e.g. exposure, gain, image size, etc. The last two lines contain statistics about the image that was captured, e.g. mean values, intensity histograms, etc.

This feature is supported on output image sizes from full resolution to VGA.

CROSSBAR

The AS0142 Rev 2 has a crossbar functionality that allows the assignment of any Data, Vsync, Hsync, line valid, and frame valid signals to any of the 27 possible parallel output pins. Normally, as is the case for the legacy mode of the AS0142AT, the 27 output pins are named DOUT[23:0], LINE_VALID, FRAME_VALID and META_LINE_VALID.

These output pins can be considered as DOUT[26:0], with no special assignments as any data bit or control signal may be assigned to any output. If desired, each data bit or control signal may even be assigned to multiple outputs at once.

The crossbar has 27 registers that define how each input should be assigned to each of the 27 possible outputs. This feature affords a large amount of flexibility for the customer. For example, during PCB layout, the pins can be adjusted to minimize crossovers and optimize routing paths.

SPATIAL TRANSFORM ENGINE (STE)

A spatial transform is defined as a transform in which some pixels are in different positions within the input and output pictures. Examples include zoom, lens distortion correction, turn, rotate, roaming and projection. STE is a fully programmable engine which can perform spatial transforms.

LENS DISTORTION CORRECTION

Automotive backup cameras typically feature a wide FOV lens so that a single camera mounted above the center of the rear bumper can present the driver with a view of all potential obstacles immediately behind the full width of the vehicle. Lenses with a wide field of view typically exhibit at least a noticeable amount of barrel distortion.

Barrel distortion is caused by a reduction in object magnification the further away from the optical axis.

For the image to appear natural to the driver, the AS0142AT corrects this barrel distortion and reprocesses the image so that the resulting distortion is much smaller. This is called distortion correction. Distortion correction is the ability to digitally correct the lens barrel distortion and to provide a natural view of objects. In addition, with barrel distortion one can adjust the perspective view to enhance the visibility by virtually elevating the point of viewing objects.

PERSPECTIVE VIEW

A backup camera has to be able to virtually adjust the vertical perspective as if the camera were placed immediately behind the vehicle pointed directly down, as illustrated in Figure 22. The vertical perspective adjustment may be employed temporarily to assist with parking conditions, or it may be enabled permanently by loading new parameters.

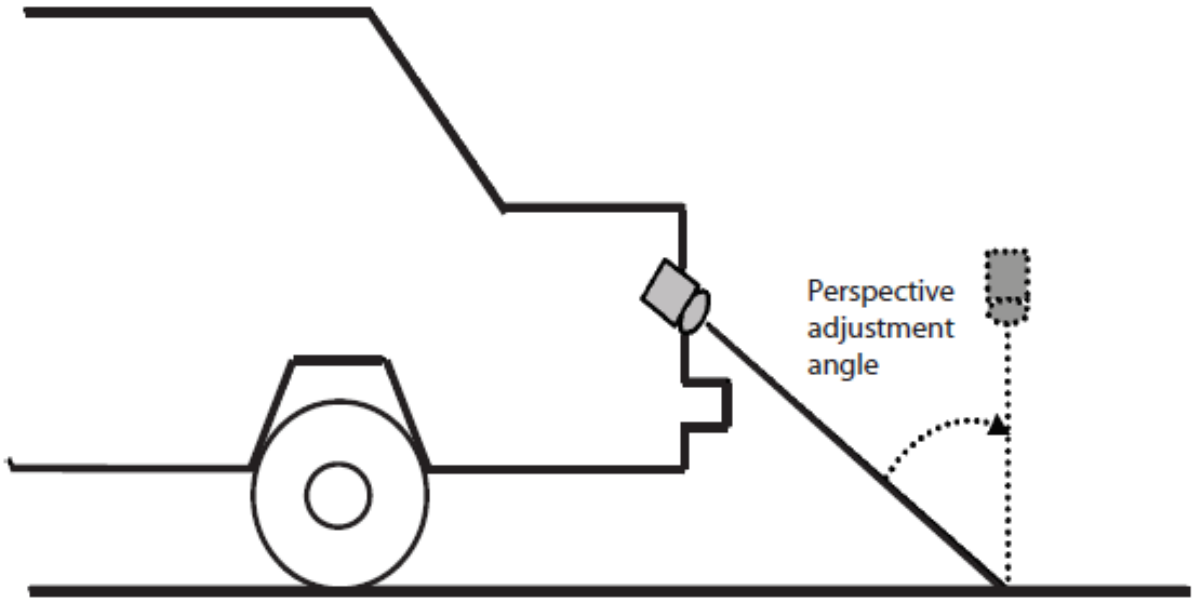


Figure 22. Vertical Perspective Adjustment

PAN, TILT, ZOOM, AND ROTATE

Using the STE it is possible to implement image transformations like Pan, Tilt, Zoom and Rotate.

Figure 23. Uncorrected Image

Figure 24. Zoomed

Figure 25. Zoom and Look Left

Figure 26. Zoom and Look Right

MULTI-PANEL

STE supports multi−panel views, these can be 2 or 3 panels. This feature is ideally suited for applications where viewing at a junction is required.

Figure 27. Multi−Panel

OVERLAY

The AS0142AT supports graphic overlays.

BITMAP RLE LAYER

Seven RLE layers containing “static” graphic data that does not change often. Essentially these are bit mapped graphic overlays.

Each RLE layer has 16K bytes of image space. 32 colors per layer. Each color has a YCbCr (8-8−8 bit) and 8 bits for the Alpha value (Opacity). The position, size and crop area can be defined for each layer.

The total number of layers is now 12 (7 RLE, 2 Line, 2 Arc, and 1 Character).

LINE LAYER

A layer that contains line data can also be overlaid. The Line Layer would be changed based on a host command and within that command would be a small number of parameters like line end points, line width, and color. It also supports anti−aliasing. Lines can be updated much faster and easier and are therefore more useful for dynamic overlays.

ARC LAYER

A layer that contains arc data can also be overlaid. The Arc Layer would be changed based on a host command and within that command would be a small number of parameters like arc center point, arc radius, arc start degrees, total arc degrees, and color. Arcs in this case are described as circle segments and can be linked to create general curves. Again these are useful for dynamic overlays.

CHARACTER GENERATOR LAYER

32 by 32 fixed font. Numbers and punctuation. In decimated mode 16 by 16 fixed font. Up to 40 32x32 characters on 4 separate lines, or up to 64 16x16 characters on 4 separate lines.

CHARACTER ROM/RAM

The ROM shall contain 191 characters from UTF−8/Unicode. It will also support the user inputting up to 64 user−defined characters.
These will be 32x32 in size.

SLAVE TWO−WIRE SERIAL INTERFACE (CCIS)

The two−wire slave serial interface bus enables read/write access to control and status registers within the AS0142AT.

The interface protocol uses a master/slave model in which a master controls one or more slave devices.

PROTOCOL

Data transfers on the two−wire serial interface bus are performed by a sequence of low-level protocol elements, as follows:

- A start or restart condition
- A slave address/data direction byte
- A 16−bit register address
- An acknowledge or a no−acknowledge bit
- Data bytes
- A stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

The SADDR pin is used to select between two different addresses in case of conflict with another device. If SADDR is LOW, the slave address is 0x90; if SADDR is HIGH, the slave address is 0xBA. See Table 22 below. The user can change the slave address by changing a register value.

Table 22. TWO−WIRE INTERFACE ID ADDRESS SWITCHING

SADDR	Two−Wire Interface Address ID
0	0x90
1	0xBA

START CONDITION

A start condition is defined as a HIGH−to−LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

DATA TRANSFER

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no−acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes. One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is low and must be stable while SCLK is HIGH.

SLAVE ADDRESS/DATA DIRECTION BYTE

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a write, and a “1” indicates a read. The default slave addresses used by the AS0142AT are 0x90 (write address) and 0x91 (read address). Alternate slave addresses of 0xBA (write address) and 0xBB (read address) can be selected by asserting the SADDR input signal.

MESSAGE BYTE

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data. The protocol used is outside the scope of the two−wire serial interface specification.

ACKNOWLEDGE BIT

Each 8−bit data transfer is followed by an acknowledge bit or a no−acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

NO−ACKNOWLEDGE BIT

The no−acknowledge bit is generated when the receiver does not drive SDATA low during the SCLK clock period following a data transfer. A no−acknowledge bit is used to terminate a read sequence.

STOP CONDITION

A stop condition is defined as a LOW−to−HIGH transition on SDATA while SCLK is HIGH.

TYPICAL OPERATION

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8−bit slave address/data direction byte. The last bit indicates whether the request is for a READ or a WRITE, where a “0” indicates a WRITE and a “1” indicates a READ. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16−bit register address to which a WRITE will take place. This transfer takes place as two 8−bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master will then transfer the 16−bit data, as two 8−bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master stops writing by generating a (re)start or stop condition. If the request was a READ, the master sends the 8−bit write slave address/data direction byte and 16−bit register address, just as in the write request. The master then generates a (re)start condition and the 8−bit read slave address/data direction byte, and clocks out the register data, 8 bits at a time. The master generates an acknowledge bit after each 8− bit transfer. The data transfer is stopped when the master sends a no−acknowledge bit.

SINGLE READ FROM RANDOM LOCATION

Figure 28 shows the typical READ cycle of the host to the AS0142AT. The first two bytes sent by the host are an internal 16−bit register address. The following 2−byte READ cycle sends the contents of the registers to host.

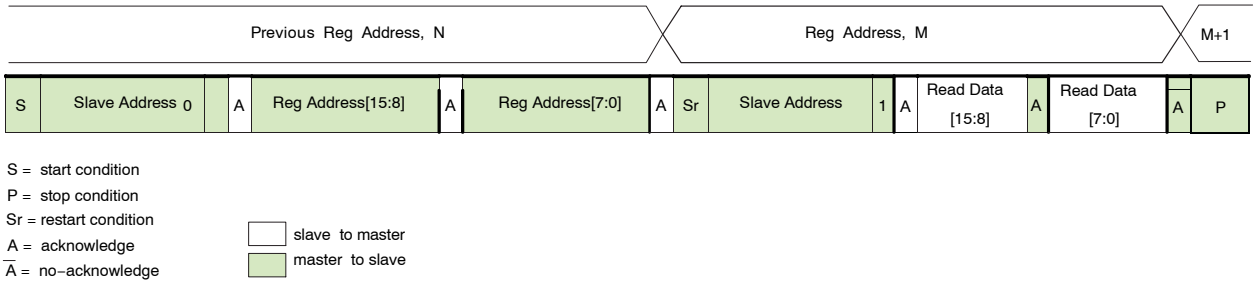


Figure 28. Single READ from Random Location

SINGLE READ FROM CURRENT LOCATION

Figure 29 shows the single READ cycle without writing the address. The internal address will use the previous address value written to the register.

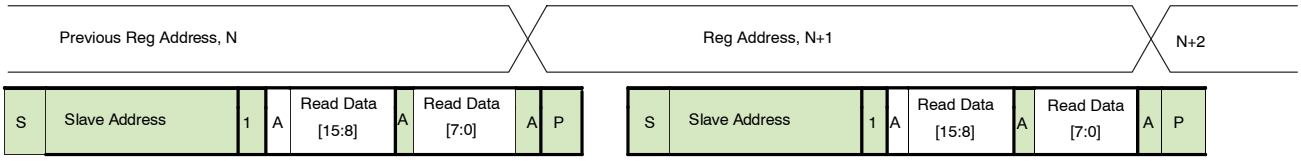


Figure 29. Single Read from Current Location

SEQUENTIAL READ, START FROM RANDOM LOCATION

This sequence (Figure 30) starts in the same way as the single READ from random location (Figure 28. Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

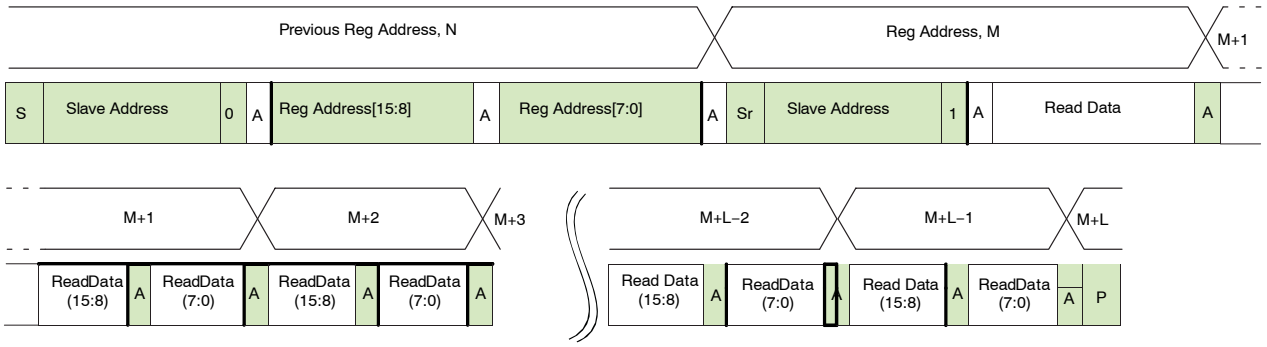


Figure 30. Sequential READ, Start from Random Location

SEQUENTIAL READ, START FROM CURRENT LOCATION

This sequence (Figure 31) starts in the same way as the single READ from current location (Figure 29). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte reads until “L” bytes have been read.

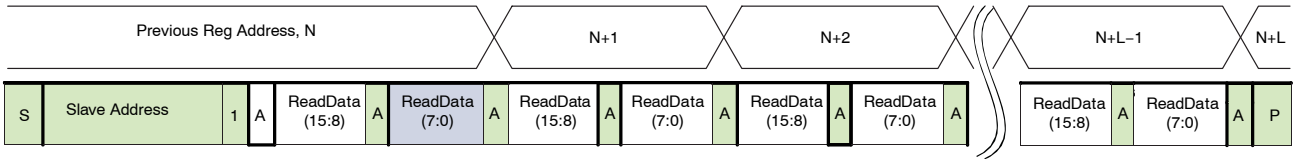


Figure 31. Sequential READ, Start from Current Location

SINGLE WRITE TO RANDOM LOCATION

Figure 32 shows the typical WRITE cycle from the host to the AS0142AT. The first 2 bytes indicate a 16−bit address of the internal registers with most−significant byte first. The following 2 bytes indicate the 16−bit data.

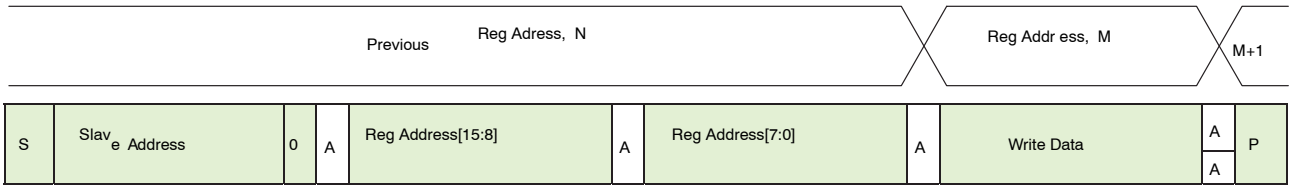


Figure 32. Single WRITE to Random Location

SEQUENTIAL WRITE, START AT RANDOM LOCATION

This sequence (Figure 33) starts in the same way as the single WRITE to random location (Figure 32). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte writes until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

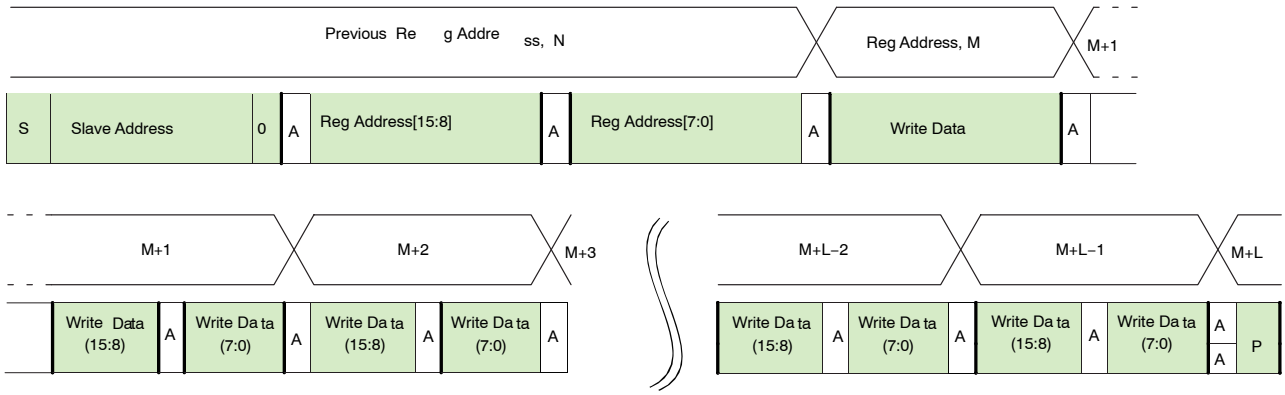


Figure 33. Sequential WRITE, Start at Random Location

SUPPORTED SPI DEVICES

The supported devices are those that conform to the JEDEC−compliant programming interface. Please contact ON Semiconductor for specific design criteria and requirements. The maximum supported device size is 2 Gb.

HOST COMMAND INTERFACE

The AS0142AT has a mechanism to write higher level commands thru the Host Command Interface (HCI). Once a command has been written through the HCI, it will be executed by on chip firmware and the results are reported back. EEPROM or Flash memory is also available to store commands for later execution.

Full details of the Host Command Interface can be found in the AS0142AT Host Command Interface (HCI) Specification document.

SPECIFICATIONS

Caution: Stresses greater than those listed in Table 23 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 23. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating		Unit
	Min	Max	
Host I/O Supply (1V8/2V8/3V3_IO)	−0.3	4	V
Host Serial Supply (2V8_PHY)	−0.3	4	V
Sensor I/O Supply (1V8_IO)	−0.3	2.4	V
Sensor Serial Supply (1V8_PHY)	−0.3	2.4	V
Sensor Analog Supply (VAA_2V8)	−0.3	4	V
On−Chip Regulator Supply (REG_1V8)	−0.3	2.4	V
Sensor Digital Core Supply (VDD_1V8)	−0.3	2.4	V
Co−Processor Digital Core Supply (VDD_1V2)	−0.3	1.8	V
OTPM Supply (OTPM_2V8)	−0.3	4	V
DC Input Voltage	−0.3	I/O Voltage + 0.3	V
DC Output Voltage	−0.3	I/O Voltage + 0.3	V
Storage Temperature	−50	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*REG_1V8 under Internal Regulator Mode

Table 24. ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS (Internal Regulator)

Parameter	Condition	Min	Typ	Max	Unit
Host IO Voltage (1V8/2V8/3V3_IO		1.71	1.8 / 2.8/3.3	3.46	V
Host Serial Voltage (2V8_PHY)		2.3	2.8	2.94	V
Sensor IO Voltage (1V8_IO)		1.71	1.8	1.89	V
Sensor Serial Voltage (1V8_PHY)		1.71	1.8	1.89	V
Sensor Analog Voltage (VAA_2V8)		2.5	2.8	2.94	V
Supply Voltage to On−Chip Regulator (REG_1V8)		1.71	1.8	1.89	V
Sensor Digital Core Voltage (VDD_1V8)		1.71	1.8	1.89	V
Co−Processor Digital Core Voltage (VDD_1V2)		1.14	1.2	1.26	V
OTPM Power Supply (OTPM_2V8)		2.38	2.8/3.3	3.46	V
Functional operating temperature	Ambient, T_A	−40		105	°C

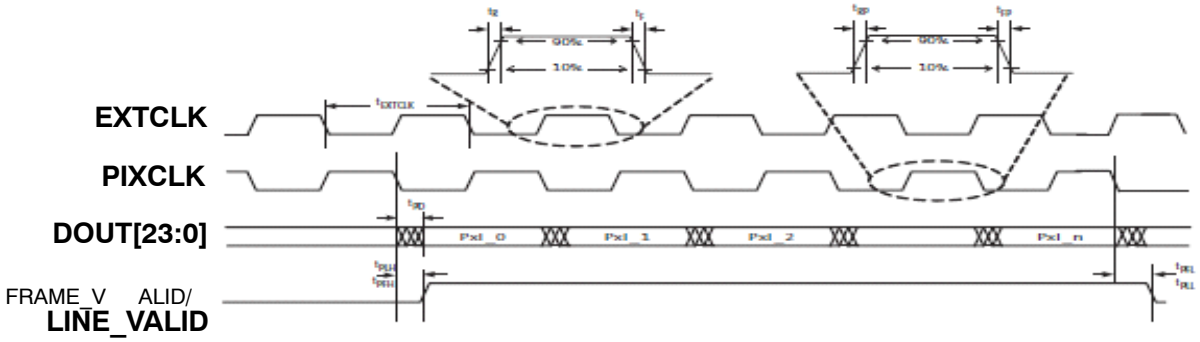


Figure 34. I/O Timing Diagram

Table 25. I/O TIMING CHARACTERISTICS − PARALLEL MODE (1V8/2V3/3V3 @ 2.8V) (Notes 4 and 5)

Symbol	Definition	Condition	Min	Typ	Max	Unit
fEXTCLK1	Input Clock Frequency	PLL Enabled	10	−	29	MHz
tR	Input Clock Rise Time	10%−90% 1V8/2V8/3V3_IO	−	2	TBD	nS
tF	Input Clock Fall Time	10%−90% 1V8/2V8/3V3_IO	−	2	TBD	nS
tJITTER	Input Clock Jitter		−	−	500	pS
tRP	PIXCLK Rise Time		−	3	TBD	nS
tFP	PIXCLK Fall Time		−	3	TBD	nS
	Duty Cycle		40	50	60	%
fPIXCLK	PIXCLK Frequency		18	74.25	125	MHz
tPD	PIXCLK to Data Valid		TBD	−	TBD	nS
tPFH	PIXCLK to FRAME_VALID HIGH		TBD	−	TBD	nS
tPLH	PIXCLK to LINE_VALID HIGH		TBD	−	TBD	nS
tPFL	PIXCLK to FRAME_VALID LOW		TBD	−	TBD	nS
tPLL	PIXCLK to LINE_VALID LOW		TBD	−	TBD	nS

4. Minimum and maximum values are taken at 105°C, 2.5 V and −40°C, 2.94 V. All values are taken at the 50% transition point. The loading used is 10 pF.
5. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.
6. Max PIXCLK frequency varies with IO voltage. Refer to Table 29, “Output Clocks,” for details.

Table 26. I/O TIMING CHARACTERISTICS − PARALLEL MODE (1V8/2V8/3V3 @ 1.8 V) (Notes 7 and 8)

Symbol	Definition	Condition	Min	Typ	Max	Unit
fEXTCLK1	Input Clock Frequency	PLL Enabled	10	−	29	MHz
tR	Input Clock Rise Time	10%−90% 1V8/2V8/3V3_IO	−	2	TBD	nS
tF	Input Clock Fall Time	10%−90% 1V8/2V8/3V3_IO	−	2	TBD	nS
tJITTER	Input Clock Jitter		−	−	500	pS
tRP	PIXCLK Rise Time		−	3	TBD	nS
tFP	PIXCLK Fall Time		−	3	TBD	nS
	Duty Cycle		40	50	60	%
fPIXCLK	PIXCLK Frequency		18	74.25	80	MHz
tPD	PIXCLK to Data Valid		TBD	−	TBD	nS
tPFH	PIXCLK to FRAME_VALID HIGH		TBD	−	TBD	nS
tPLH	PIXCLK to LINE_VALID HIGH		TBD	−	TBD	nS
tPFL	PIXCLK to FRAME_VALID LOW		TBD	−	TBD	nS
tPLL	PIXCLK to LINE_VALID LOW		TBD	−	TBD	nS

7. Minimum and maximum values are taken at 105°C, 1.71 V and −40°C, 1.89 V. All values are taken at the 50% transition point. The loading used is 10 pF.
8. Jitter from PIXCLK_OUT is already taken into account in the data for all of the output parameters.

Table 27. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition(s)	Min	Max	Unit	Notes
VIH	Input HIGH voltage		1V8/2V8/3V3_IO * 0.8	−	V	9
VIL	Input LOW voltage		−	1V8/2V8/3V8_IO * 0.2	V	9
IIN	Input Leakage Current	VIN = 0 V, VIN = 1V8/2V8/3V3_IO, VIN = 1V8_IO, or VIN = VDD_1V8	−1	1	μA	10
VOH	Output HIGH voltage		1V8/2V8/3V3_IO * 0.8	−	V	
VOL	Output LOW voltage		−	1V8/2V8/3V3_IO * 0.2	V	
IOZ	Output Leakage Current	I/O Pad @ Tri−State, and VOUT = 0 V to VOUT = 1V8/2V8/3V3_IO/ 1V8_IO	−1	1	μA	11

9. VIL and VIH have min/max limitations specified by absolute ratings.
10. Excludes pins that have internal PU resistors.
11. Excludes power pins and pins that cannot be Tri−State (e.g. XTAL pin).

INPUT CLOCKS

Table 28. INPUT CLOCKS

Clock	Min (MHz)	Typical (MHz)	Max (MHz)	Description
EXTCLK	10 (without XTAL) 20 (with XTAL)	27	29	Primary system clock. Drives PLLs. Crystal frequency range is 20-29 MHz, otherwise 10-29 MHz.

OUTPUT CLOCKS

Table 29. Output Clocks

Clock	MIN (MHz)	Typical (MHz)	Max (MHz)	Description
PIXCLK	18	74.25/25	80/125	Clock of parallel output bus. If pad voltage is 1.8 V nominal, then max frequency is 80 MHz. If pad voltage is 2.5 V, the hold time will decrease to 1.9 ns from 2.0 ns @ 125 MHz If pad voltage is 3.3V, then the max frequency is 125Mhz.
SPI_SCLK	1.2		20	SPI clock to nonvolatile external memory.

FRAME SYNC TIMING

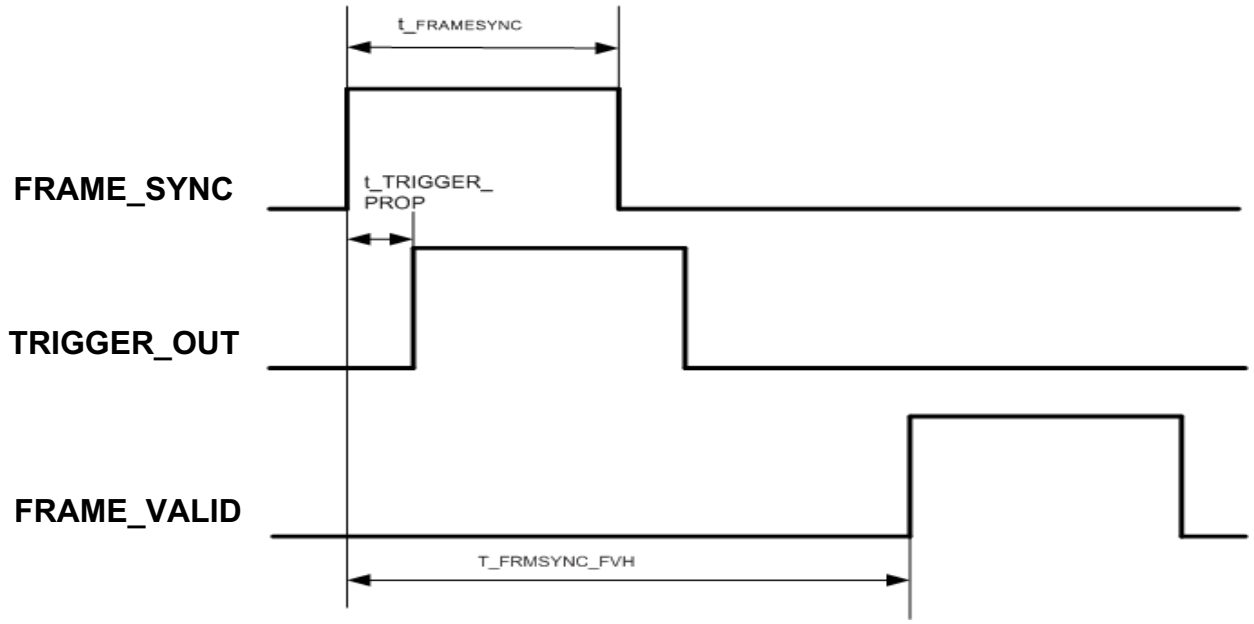


Figure 35. FRAME_SYNC (Operation) Diagram

Table 30. TRIGGER TIMING

Parameter	Name	Conditions	Min	Typ	Max	Unit
FRAME_SYNC to FRAME_VALID	tFRMSYNC_FVH		8 lines+ exposure time + sensor delay	–	–	Lines
FRAME_SYNC to TRIGGER_OUT	tTRIGGER_PROP		–	–	30	ns
tFRAME_SYNC	tFRAMESYNC		3	–	–	EXTCLK cycles

STANDBY AND INRUSH CURRENT (INTERNAL REGULATOR MODE)

Table 31. STANDBY CURRENT CONSUMPTION

Default Setup Conditions: fEXTCLK = 27 MHz, REG_1V8 = 1.8 V; VDD_1V8 = 1.8 V, OTPM_2V8 = 2.8 V, PHY_2V8 = 2.8 V, PHY_1V8 = 1.8 V, VAA_2V8 = 2.8 V, 1V8/2V8/3V3_IO = 2.8 V, 1V8_IO = 1.8 V, T_A = 105°C

Parameter/ Supply	Condition	Typ	Max	Unit
1V8/2V8/3V3_IO		TBD	TBD	mA
1V8_IO		TBD	TBD	mA
2V8_PHY		TBD	TBD	mA
1V8_PHY		TBD	TBD	mA
OTPM_2V8		TBD	TBD	mA
VAA_2V8		TBD	TBD	mA
REG_1V8		TBD	TBD	mA
VDD_1V8		TBD	TBD	mA
Total standby current when asserting the STANDBY signal		TBD	TBD	mA
		TBD	TBD	mW

Table 32. INRUSH CURRENT

Supply	Voltage	Max	Unit
1V8/2V8/3V3_IO	1.8/2.8/3.3	TBD	mA
1V8_IO	1.8	TBD	mA
2V8_PHY	2.8	TBD	mA
1V8_PHY	1.8	TBD	mA
OTPM_2V8	2.8	TBD	mA
VAA_2V8	2.8	TBD	mA
REG_1V8	1.8	TBD	mA
VDD_1V8	1.8	TBD	mA

OPERATING CURRENT (INTERNAL REGULATOR MODE)

Table 33. OPERATING CURRENT CONSUMPTION – STE AND OVERLAY BOTH ON

Default Setup Conditions: f_{EXTCLK} = 27 MHz, REG_1V8 = 1.8V, VDD_1V8=1.8V, VAA_2V8 = 2.8 V, OTPM_2V8 = 2.8V, 2V8_PHY = 2.8 V, 1V8_PHY = 1.8V, 1V8/2V8/3V3_IO and 1V8_IO not included in measurement; T_A = 105°C unless otherwise stated

Symbol	Input Data from Sensor	Min	Typ	Max	Unit
REG_1V8	Parallel	–	TBD	TBD	mA
VDD_1V8	Parallel	–	TBD	TBD	mA
VAA_2V8	Parallel	–	TBD	TBD	mA
OTPM_2V8	Parallel	–	TBD	TBD	mA
2V8_PHY	Parallel	–	TBD	TBD	mA
1V8_PHY	Parallel	–	TBD	TBD	mA
Total Power Consumption	Parallel	–	TBD	TBD	mW

Table 34. OPERATING CURRENT CONSUMPTION − STE ON AND OVERLAY OFF

Default Setup Conditions: f_{EXTCLK} = 27 MHz, REG_1V8 = 1.8V, VDD_1V8=1.8V, VAA_2V8 = 2.8V, OTPM_2V8 = 2.8V, 2V8_PHY = 2.8V, 1V8_PHY = 1.8V, 1V8/2V8/3V3_IO and 1V8_IO not included in measurement; T_A = 105°C unless otherwise stated

Symbol	Input Data from Sensor	Min	Typ	Max	Unit
REG_1V8	Parallel	−	TBD	TBD	mA
VDD_1V8	Parallel	−	TBD	TBD	mA
VAA_2V8	Parallel	−	TBD	TBD	mA
OTPM_2V8	Parallel	−	TBD	TBD	mA
2V8_PHY	Parallel	−	TBD	TBD	mA
1V8_PHY	Parallel	−	TBD	TBD	mA
Total Power Consumption	Parallel	−	TBD	TBD	mW

Table 35. OPERATING CURRENT CONSUMPTION − STE AND OVERLAY BOTH OFF

Default Setup Conditions: f_{EXTCLK} = 27 MHz, REG_1V8 = 1.8V, VDD_1V8=1.8V, VAA_2V8 = 2.8V, OTPM_2V8 = 2.8 V, 2V8_PHY = 2.8 V, 1V8_PHY = 1.8 V, 1V8/2V8/3V3_IO and 1V8_IO not included in measurement; T_A = 105°C unless otherwise stated

Symbol	Input Data from Sensor	Min	Typ	Max	Unit
REG_1V8	Parallel	−	TBD	TBD	mA
VDD_1V8	Parallel	−	TBD	TBD	mA
VAA_2V8	Parallel	−	TBD	TBD	mA
OTPM_2V8	Parallel	−	TBD	TBD	mA
2V8_PHY	Parallel	−	TBD	TBD	mA
1V8_PHY	Parallel	−	TBD	TBD	mA
Total Power Consumption	Parallel	−	TBD	TBD	mW

TWO−WIRE SERIAL REGISTER INTERFACE

The electrical characteristics of the two−wire serial register interface (SCLK, SDATA) are shown in Figure 36 and Table 36.

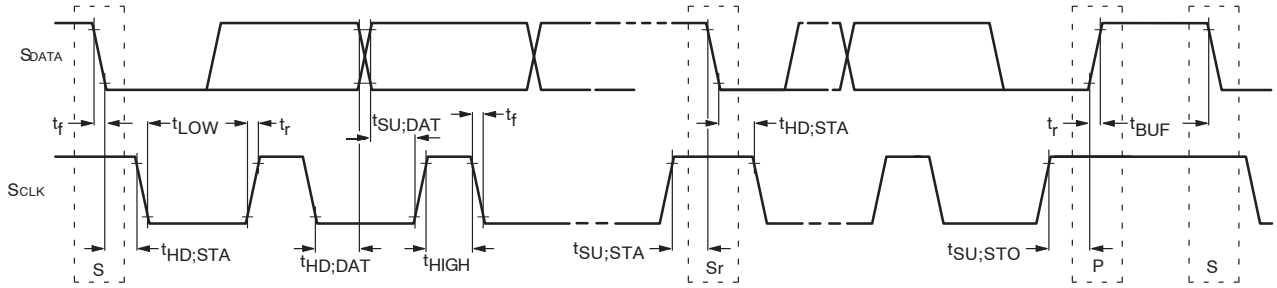


Figure 36. Slave Two Wire Serial Bus Timing Parameters (CCIS)

Table 36. SLAVE TWO−WIRE SERIAL BUS CHARACTERISTICS (CCIS)

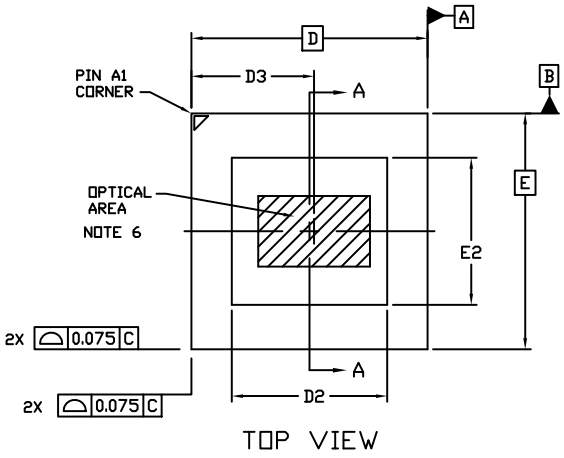
Default Setup Conditions: fEXTCLK = 27 MHz, REG_1V8 = 1.8 V; VDD_1V8 = 1.8 V, OTPM_2V8 = 2.8 V, PHY_2V8 = 2.8 V, PHY_1V8 = 1.8 V, VAA_2V8 = 2.8 V, 1V8/2V8/3V3_IO = 2.8 V, 1V8_IO = 1.8 V, T_J = 25°C unless otherwise states.

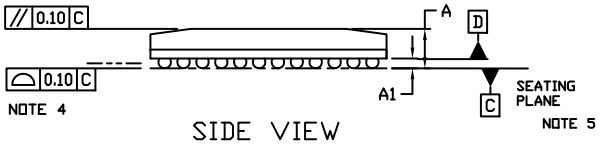
Parameter	Symbol	Standard−Mode		Fast−Mode Plus		Unit
		Min	Max	Min	Max	
SCLK Clock Frequency	fSCL	0	100	0	1000	kHz
Hold time (repeated) START condition: After this period, the first clock pulse is generated	tHD;STA	4.0	–	0.26	–	uS
LOW period of the SCLK clock	tLOW	4.7	–	0.5	–	uS
HIGH period of the SCLK clock	tHIGH	4.0	–	0.26	–	uS
Set−up time for a repeated START condition	tSU;STA	4.7	–	0.26	–	uS
Data hold time	tHD;DAT	0[2]	3.45 (Note 14)	0	–	uS
Data set-up time	tSU;DAT	250	–	50	–	nS
Rise time of both SDATA and SCLK signals (10-90%)	t_r	–	1000	20 + 0.1Cb (Note 15)	300	nS
Fall time of both SDATA and SCLK signals (10−90%)	t_f	–	300	20 + 0.1Cb (Note 15)	300	nS
Set−up time for STOP condition	tSU;STO	4.0	–	0.26	–	uS
Bus free time between a STOP and START condition	tBUF	4.7	–	0.5	–	uS
Capacitive load for each bus line	Cb	–	400	–	550	pF
Serial interface input pin capacitance (die pad)	CIN_SI	–	3.3	–	3.3	pF
SDATA max load capacitance	CLOAD_SD	–	30	–	30	pF
SDATA pull−up resistor	RSD	1.5	4.7	1.5	4.7	kΩ

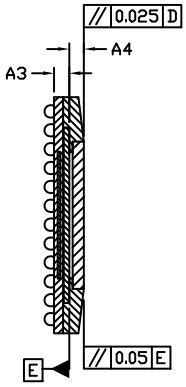
12. All values referred to VIHmin = 0.9 * 1V8/2V8/3V3_IO and VILmax = 0.1 * 1V8/2V8/3V3_IO levels.
13. A device must internally provide a hold time of at least 300 nS for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
14. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCLK signal.
15. Cb = total capacitance of one bus line in pF.

PACKAGE DIMENSIONS

IBGA143 8.5x8.5
CASE 503BH
ISSUE O



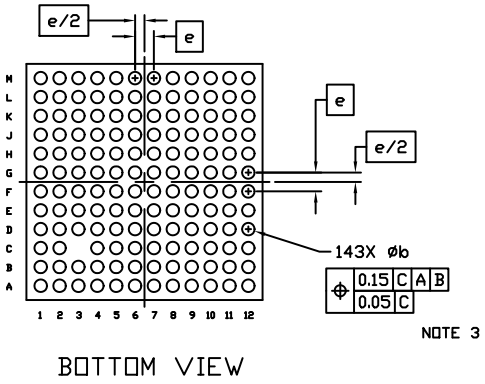


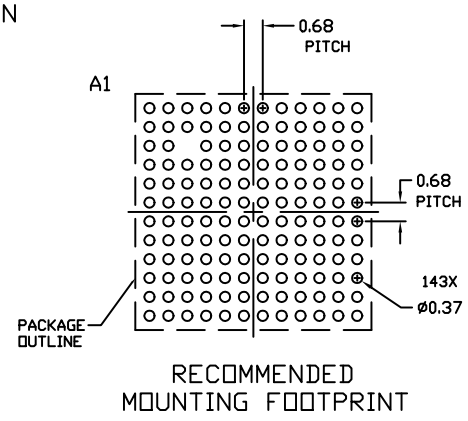


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. DIMENSION D3 LOCATES THE OPTICAL AREA CENTER. MAXIMUM ROTATION OF OPTICAL AREA RELATIVE D AND E WILL BE 1°. OPTICAL AREA IS DEFINED BY THE ACTIVE PIXEL ARRAY AND IS NOT DELINEATED BY THE LIGHT BLOCK BOUNDARY. REFER TO THE DEVICE DATA SHEET FOR TOTAL ARRAY AND FIRST ACTIVE PIXEL DEFINITIONS.

	MILLIMETERS	
DIM	MIN.	MAX.
A	---	1.57
A1	0.30	0.40
A3	0.495	0.595
A4	0.475	0.575
b	0.40	0.50
D	8.50 BSC	
D2	5.50	5.70
D3	4.34	4.49
E	8.50 BSC	
E2	5.20	5.40
e	0.68 BSC	





PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative