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FAIRCHILD SEMICONDUCTOR®

2013 年 11 月

FAN73932
半桥栅极驱动 IC

特性

- 浮动通道可实现高达 +600V 的自举运行
- 2.5A/2.5A 的典型源电流 / 灌电流驱动能力
- 扩展容许负 V_S 摆幅至 -9.8V，适合 V_{BS}=15V 的信号传播
- 高侧输出与 IN 输入信号同相
- 兼容 3.3V 和 5V 逻辑输入电平
- 适用于两个通道的匹配传播延迟
- 内置关断功能
- 两个通道均内置欠压闭锁 (UVLO) 功能
- 内置共模 dv/dt 噪声消除电路
- 内部最小 400ns 死区时间

应用

- 高速功率 MOSFET 和 IGBT 栅极驱动器
- 感应加热
- 大功率 DC-DC 转换器
- 同步降压转换器
- 电机驱动逆变器

说明

FAN73932 是一款半桥栅极驱动 IC，带关断和死区时间控制功能，可以驱动工作电压最高可达 +600V 的高速 MOSFET 和 IGBT。它具有缓冲输出级，且所有 NMOS 晶体管设计为具有高脉冲电流驱动能力和最低交叠导通。

飞兆的高压工艺和共模噪声消除技术 s 可使高侧驱动器在高 dv/dt 噪声环境下稳定运行。先进的电平转换电路，能使高侧栅极驱动器的工作电压在 V_{BS}=15V 时 V_S 达到 -9.8V （典型值）。

UVLO （欠压保护）电路在 V_{DD} 和 V_{BS} 低于额定阈值电压时启动保护防止故障发生。

大电流和低输出压降功能使得此器件适合所有类型的半桥和全桥逆变器，如电机驱动逆变器、开关电源、感应加热和大功率 DC-DC 转换器应用。

8-SOP

订购信息

器件编号	封装	工作温度范围	生态状况	包装方法
FAN73932M	8-SOP	-40°C 至 +125°C	RoHS	塑料管
FAN73932MX				卷带和卷盘

有关飞兆 Eco 状况的定义，请访问：*http://www.fairchildsemi.com/company/green/rohs_green.html*。

应用电路图

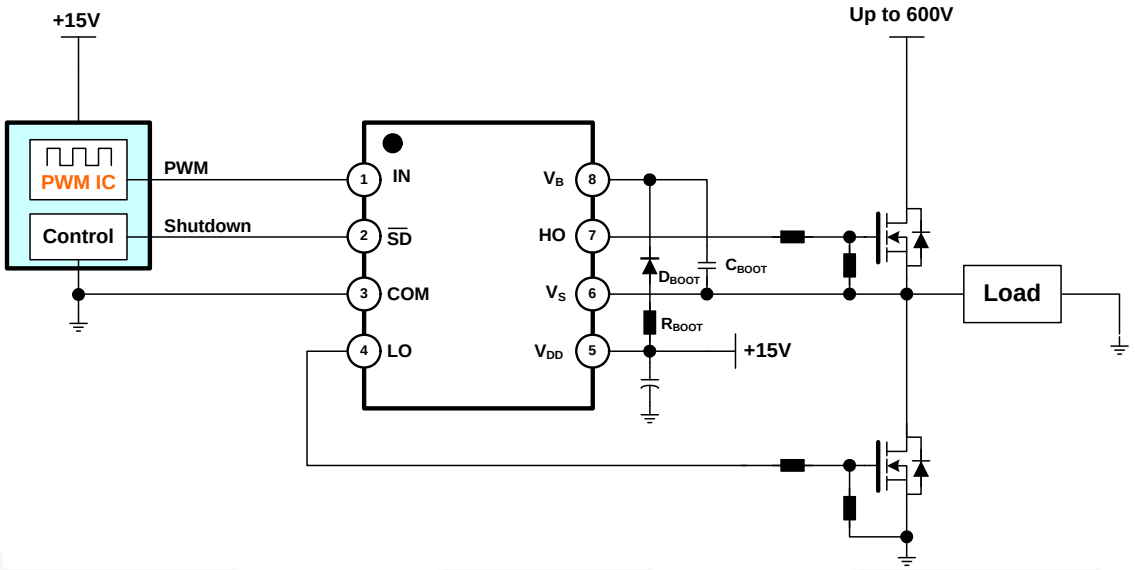


图 1. 典型应用电路

内部框图

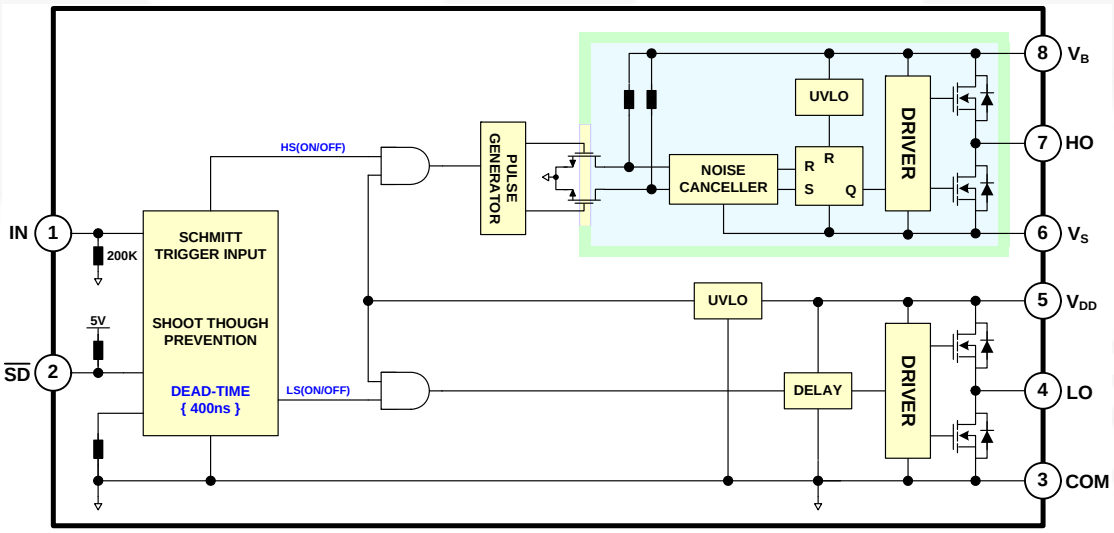


图 2. 功能框图

引脚布局

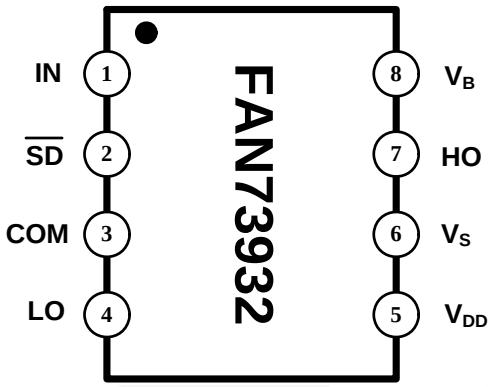


图 3. 引脚布局 （顶视图）

引脚定义

引脚号	名称	说明
1	IN	高侧和低侧栅极驱动器输出的逻辑输入，与 HO 同相
2	$\overline{SD}$	关断逻辑输入
3	COM	接地
4	LO	低侧驱动输出
5	V_{DD}	电源电压
6	V_S	高压浮地
7	HO	高侧驱动输出
8	V_B	高侧浮动供电

绝对最大额定值

应力超过绝对最大额定值，可能会损坏器件。在超出推荐的工作条件的情况下，该器件可能无法正常工作，所以不建议让器件在这些条件下长期工作。此外，在远高于推荐的工作条件下工作，会影响器件的可靠性。绝对最大额定值仅是应力规格值。 T_A=25°C，除非另有规定。

符号	参数	最小值	最大值	单位
V_B	高侧浮动电源电压	-0.3	625.0	V
V_S	高侧浮动偏置电压	V_B-25.0	V_B+0.3	V
V_{HO}	高侧浮动输出电压	V_S-0.3	V_B+0.3	V
V_{LO}	低侧输出电压	-0.3	V_{DD}+0.3	V
V_{DD}	低侧和逻辑电源电压	-0.3	25.0	V
V_{IN}	逻辑输入电压 (IN)	-0.3	V_{DD}+0.3	V
V_{SD}	逻辑输入电压 ($\overline{SD}$)	-0.3	5.5	V
COM	逻辑接地和低侧驱动器接地	V_{DD}-25.0	V_{DD}+0.3	V
dV_S/dt	允许偏置电压变化速率		± 50	V/ns
P_D	功耗 (1, 2, 3)		0.625	W
θ_{JA}	热阻		200	°C/W
T_J	结温		+150	°C
T_{STG}	存储温度	-55	+150	°C

注意：

1. 安装到 76.2 x 114.3 x 1.6mm PCB 板 (FR-4 环氧玻璃材料)。
2. 参考以下标准：
   JESD51-2: 集成电路热测试方法环境条件 - 自然对流；
   JESD51-3: 含铅表面贴装封装的低有效导热系数测试板。
3. 在任何情况下，都不要超过 P_D。

推荐工作条件

推荐的工作条件表明确了器件的真实工作条件。指定推荐的工作条件，以确保器件的最佳性能达到数据表中的规格。飞兆不建议超出额定或依照绝对最大额定值进行设计。

符号	参数	最小值	最大值	单位
V_B	高侧浮动电源电压	V_S+10	V_S+20	V
V_S	高侧浮动电源偏置电压	6-V_{DD}	600	V
V_{HO}	高侧输出电压	V_S	V_B	V
V_{DD}	低侧和逻辑电源电压	10	20	V
V_{LO}	低侧输出电压	COM	V_{DD}	V
V_{IN}	逻辑输入电压 (IN)	COM	V_{DD}	V
V_{SD}	逻辑输入电压 ($\overline{SD}$)(4)	COM	5	V
T_A	工作环境温度	-40	+125	°C

注：

4. 关断 ($\overline{SD}$) 输入在内部箝位至 5.2V。

电气特性

除非另有规定，否则 $V_{BIAS}(V_{DD}, V_{BS})$=15.0V，COM=0V，以及 T_A = 25°C。V_{IN} 和 I_{IN} 参数指的是以 COM 为参考点的值，同时适用于输入引脚：IN 和 $\overline{SD}$。 V_O 和 I_O 参数指的是以 COM 为参考点的值，同时适用于输出引脚：HO 和 LO。

符号	参数	测试条件	最小值	典型值	最大值	单位
电源部分						
I_{QDD}	静态 V_{DD} 电源电流	V_{IN}=0V， $\overline{SD}$=5V		320	700	μA
I_{QBS}	静态 V_{BS} 电源电流	V_{IN}=0V 或 5V， $\overline{SD}$=5V		50	120	μA
I_{PDD}	工作 V_{DD} 电源电流	f_{IN}=20KHz，无负载，$\overline{SD}$=5V		700	1300	μA
I_{PBS}	工作 V_{BS} 电源电流	C_L=1nF, f_{IN}=20KHz， rms，$\overline{SD}$=5V		420	800	μA
I_{SD}	关断模式电源电流	$\overline{SD}$=0V, $\overline{SD}$=5V		400	800	μA
I_{LK}	偏置漏电流	V_B=V_S=600V			10	μA
自举电源部分						
V_{DDUV+} V_{BSUV+}	V_{DD} 和 V_{BS} 电源欠压 正向 （电压从高到低）阈值电压	V_{DD} =V_{BS}=Sweep	8	9	10	V
V_{DDUV-} V_{BSUV-}	V_{DD} 和 V_{BS} 电源欠压 负向 （电压从低到高）阈值电压	V_{DD} =V_{BS}=Sweep	7.4	8.4	9.4	V
V_{DD}UVH V_{BSUVH}	V_{DD} 和 V_{BS} 电源欠压闭锁滞回电压回差	V_{DD}=V_{BS}=Sweep		0.6		V
输入逻辑部分						
V_{IH}	HO 的逻辑 “1” 输入电压和 LO 的逻辑 “0”		2.5			V
V_{IL}	HO 的逻辑 “0” 输入电压和 LO 的逻辑 “1”				0.8	V
I_{IN+}	逻辑输入高偏置电流	V_{IN}=5V, $\overline{SD}$=0V		25	60	μA
I_{IN-}	逻辑输入低偏置电流	V_{IN}=0V, $\overline{SD}$=5V			3	μA
R_{IN}	逻辑输入下拉电阻			200		KΩ
$V_{SDCLAMP}$	关断 ($\overline{SD}$) 输入箝位电压			5.0	5.5	V
$\overline{SD}$+	关断 ($\overline{SD}$) 输入正向阈值		2.5			V
$\overline{SD}$-	关断 ($\overline{SD}$) 输入负向阈值				0.8	V
R_{PSD}	关断 ($\overline{SD}$) 输入上拉电阻			200		KΩ
栅极驱动器输出部分						
V_{OH}	高电平输出电压 (V_{BIAS} - V_O)	无负载			1.5	V
V_{OL}	低电平输出电压	无负载			100	mV
I_{O+}	输出高电平、短路脉冲电流 (5)	V_{HO}=0V, V_{IN}=5V, PW ≤10μs	2.0	2.5		A
I_{O-}	输出低电平、短路脉冲电流 (5)	V_{HO}=15V, V_{IN}=0V, PW ≤10μs	2.0	2.5		A
V_S	IN 信号传播到 HO 时允许的 VS 引脚负电压			-9.8	-7.0	V

注：

5 这些参数由设计保证。

动态电气特性

除非另有规定，否则 $V_{BIAS}(V_{DD}$， $V_{BS})$=15.0V， COM=0V， C_L=1000pF，和 T_A=25°C。

符号	参数	工作条件	最小值	典型值	最大值	单位
t_{ON}	导通传播延迟时间 (6)	V_S=0V		600	850	ns
t_{OFF}	关断传播延迟时间	V_S=0V		200	350	ns
t_{SD}	关断传播延迟时间			140	220	ns
Mt_{ON}	延迟匹配， HO 和 LO 导通			0	50	ns
Mt_{OFF}	延迟匹配， HO 和 LO 关断			0	50	ns
t_R	开通上升时间	V_S=0V		25	50	ns
t_F	关断下降时间	V_S=0V		20	35	ns
DT	死区时间：LO 关断至 HO 导通和 HO 关断至 LO 导通		300	400	500	ns
MDT	死区时间匹配 =$\lvert DT_{LO-HO} - DT_{HO-LO} \rvert$			0	50	ns

注：

6. 导通传播延迟时间包括了死区时间。

典型特性

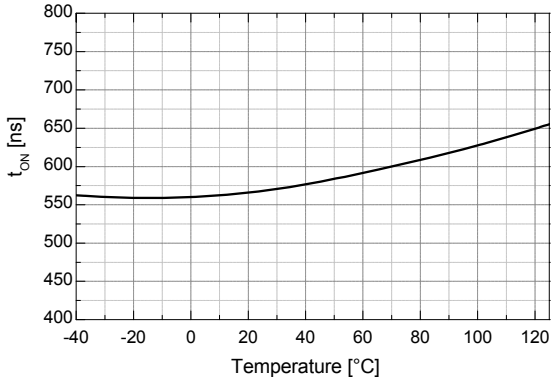


图 4. 导通传播延迟与温度的关系

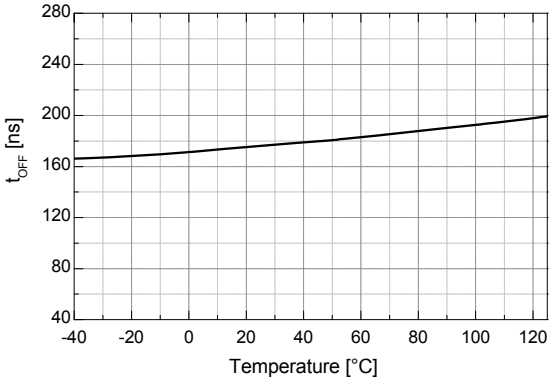


图 5. 关断传播延迟与温度的关系

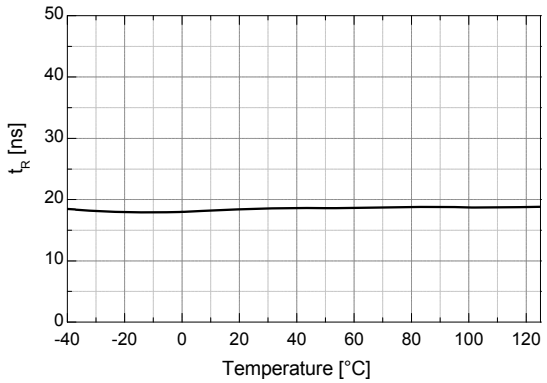


图 6. 导通上升时间与温度的关系

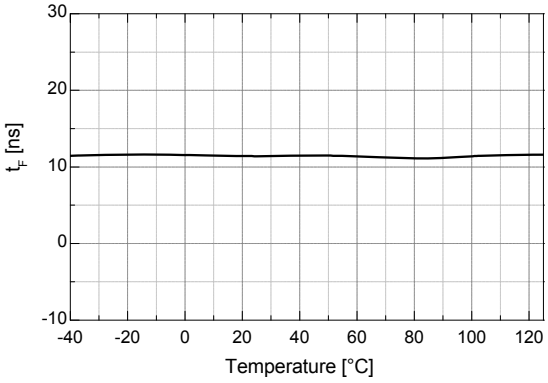


图 7. 关断下降时间与温度的关系

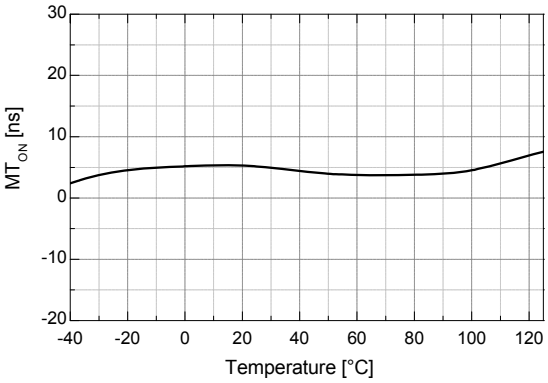


图 8. 导通延迟匹配与温度的关系

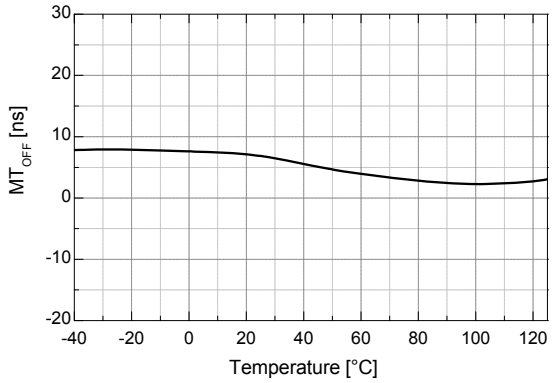


图 9. 关断延迟匹配与温度的关系

典型特性 （续）

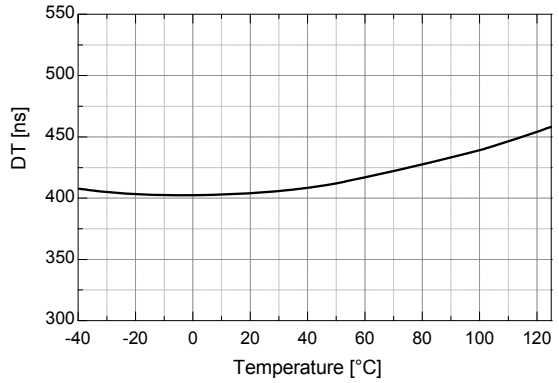


图 10. 死区时间与温度的关系

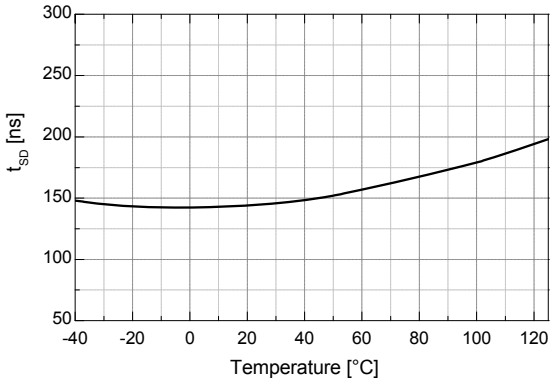


图 11. 关断传播延迟与温度的关系

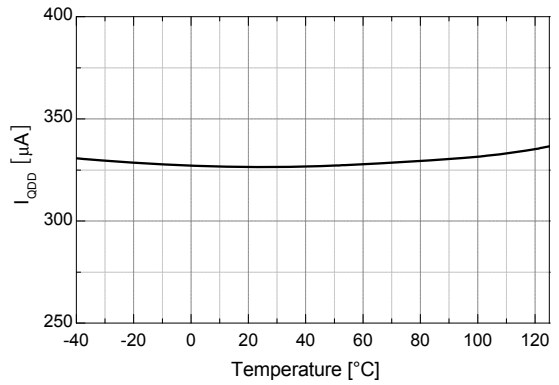


图 12. 静态 V_{DD} 电源电流与温度的关系

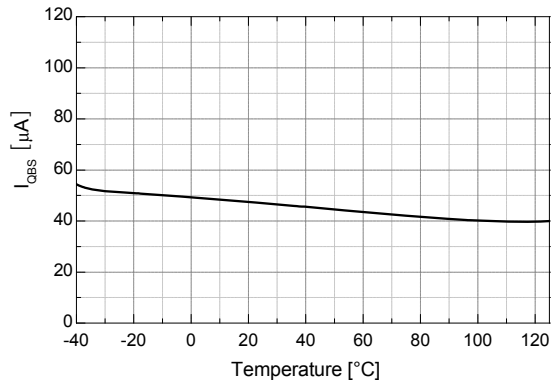


图 13. 静态 V_{BS} 电源电流与温度的关系

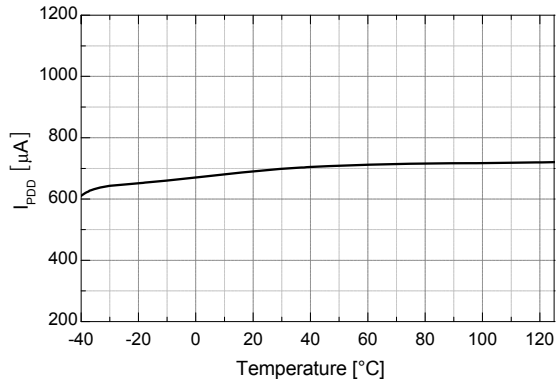


图 14. 工作时 V_{DD} 电源电流与温度的关系

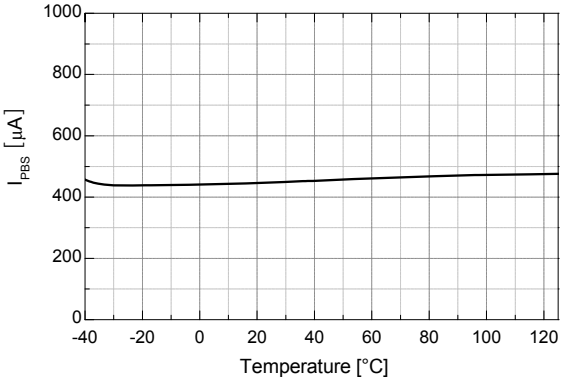


图 15. 工作 V_{BS} 电源电流与温度的关系

典型特性 （续）

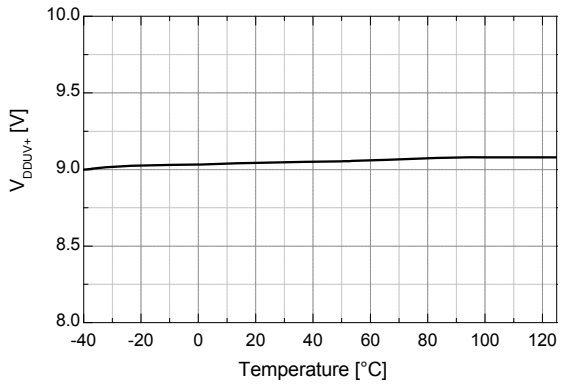


图 16.V_{DD} UVLO+ 与温度的关系

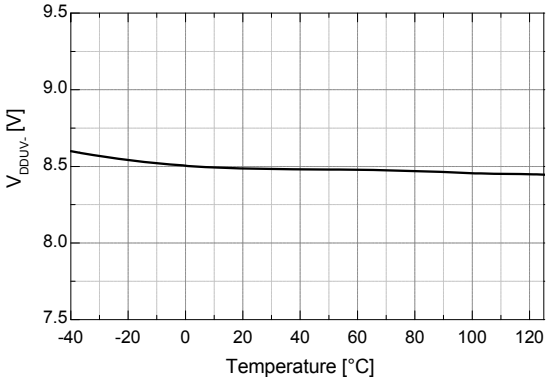


图 17.V_{DD} UVLO- 与温度的关系

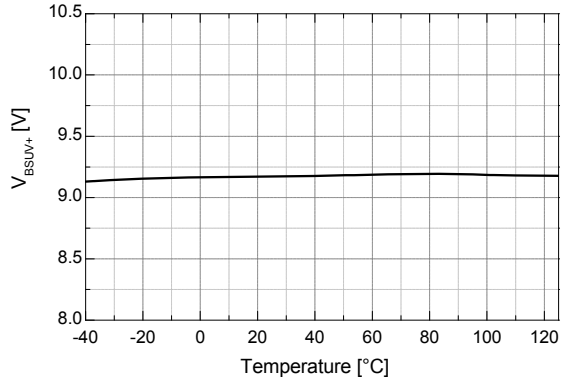


图 18.V_{BS} UVLO+ 与温度的关系

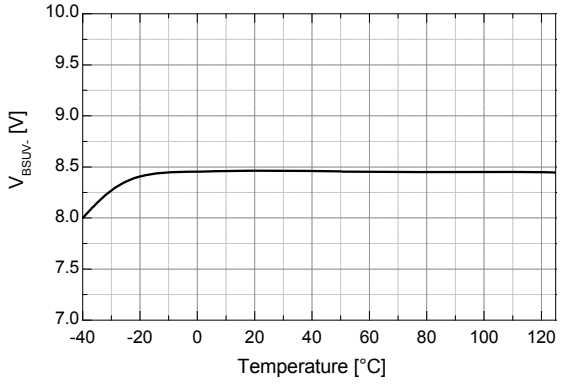


图 19.V_{BS} UVLO- 与温度的关系

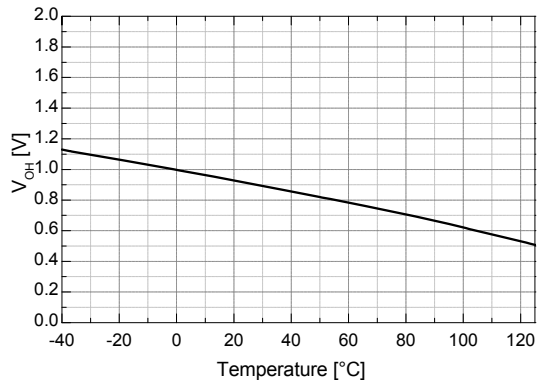


图 20. 高电平输出电压与温度的关系

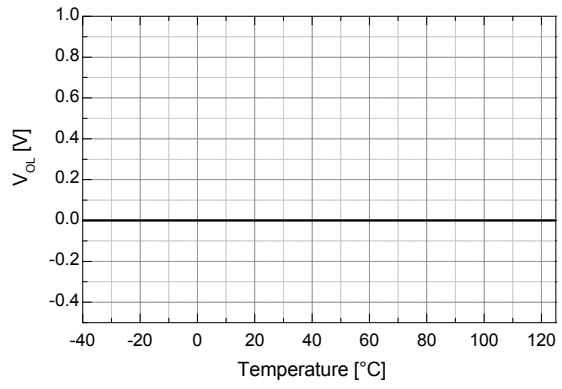


图 21. 低电平输出电压与温度的关系

典型特性 （续）

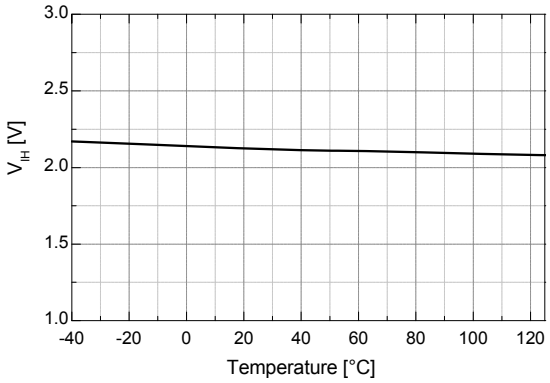


图 22. 逻辑高输入电压
与温度的关系

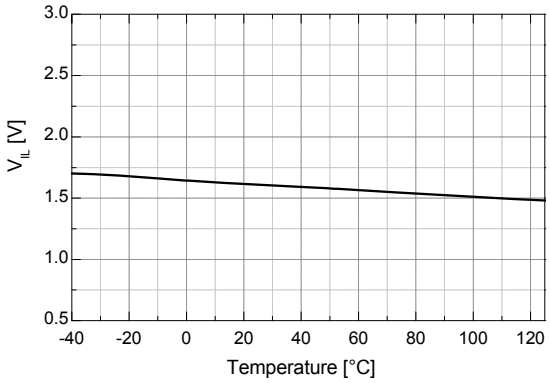


图 23. 逻辑低输入电压
与温度的关系

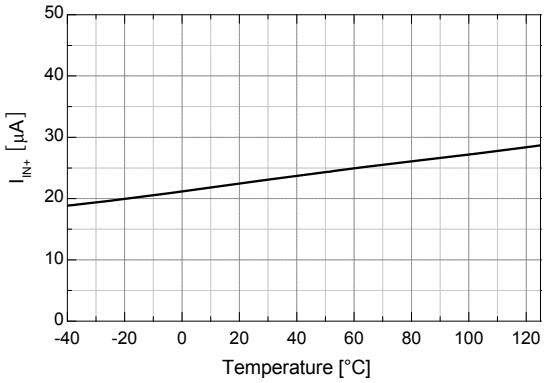


图 24. 逻辑输入高偏置电流
与温度的关系

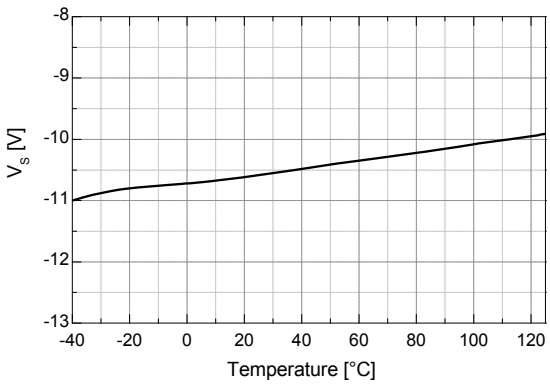


图 25. 容许负 V_S 电压
与温度的关系

开关时间定义

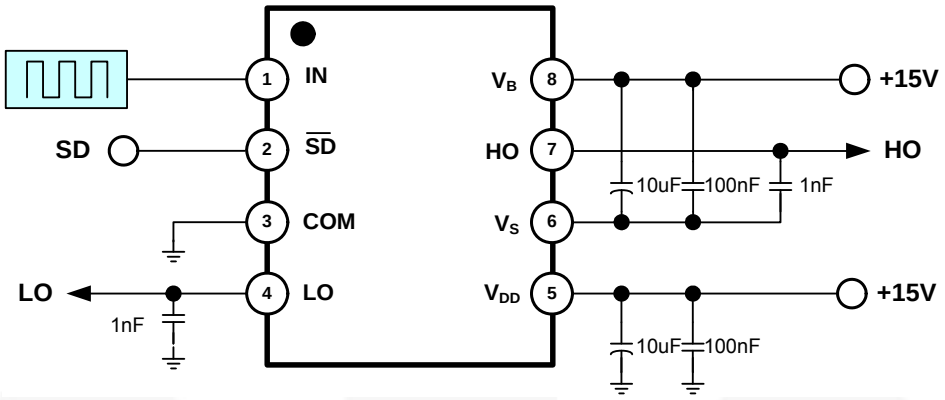


图 26. 开关时间测试电路

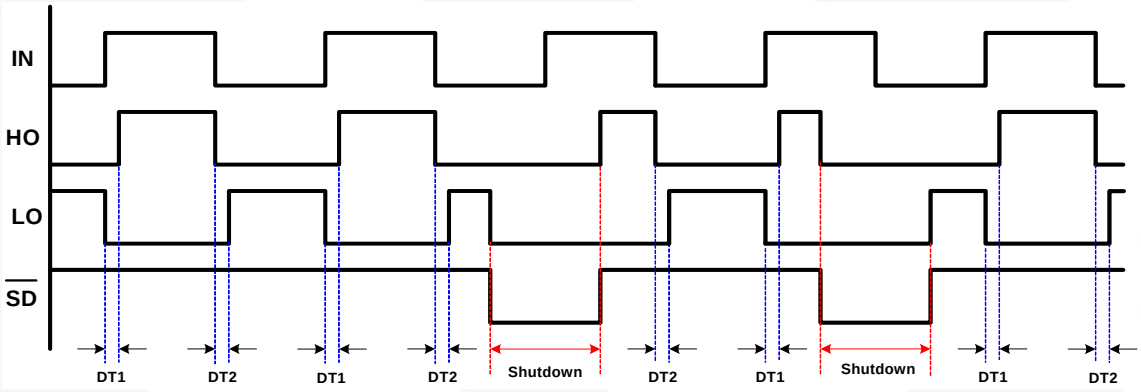


图 27. 输入 / 输出时序图

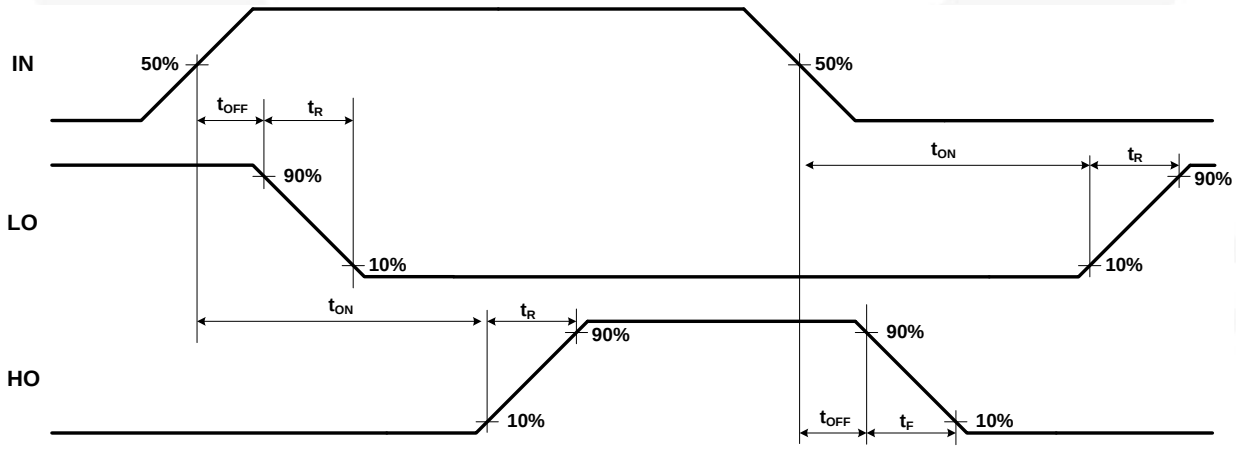


图 28. 开关时间波形定义

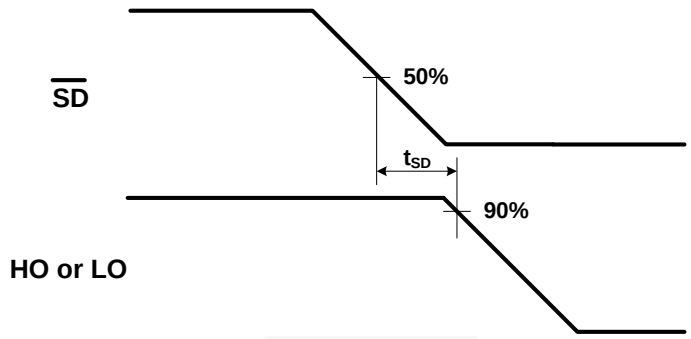
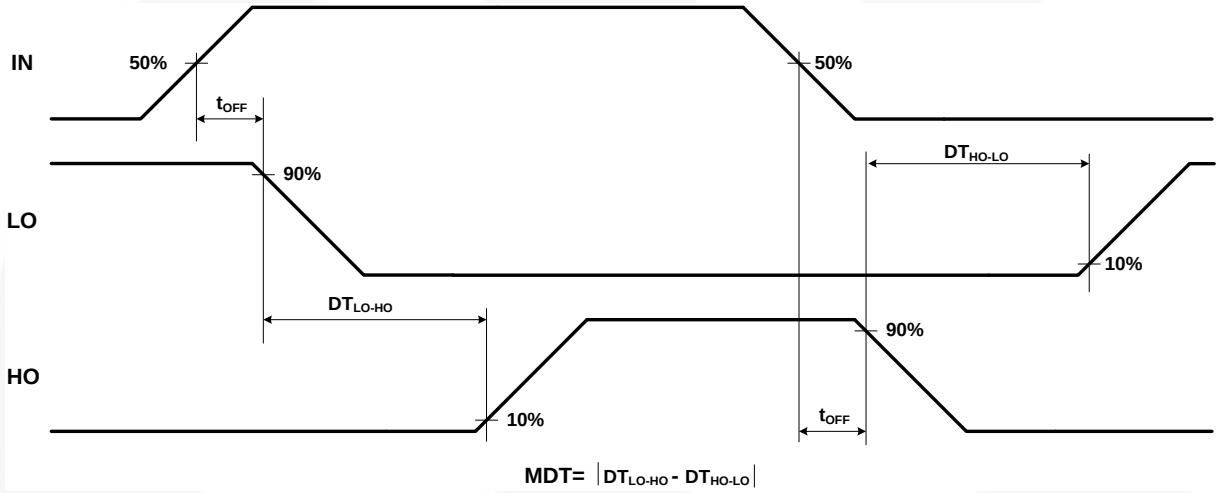


图 29. 关断波形定义



$$MDT = |DT_{LO-HO} - DT_{HO-LO}|$$

图 30. 死区时间波形定义

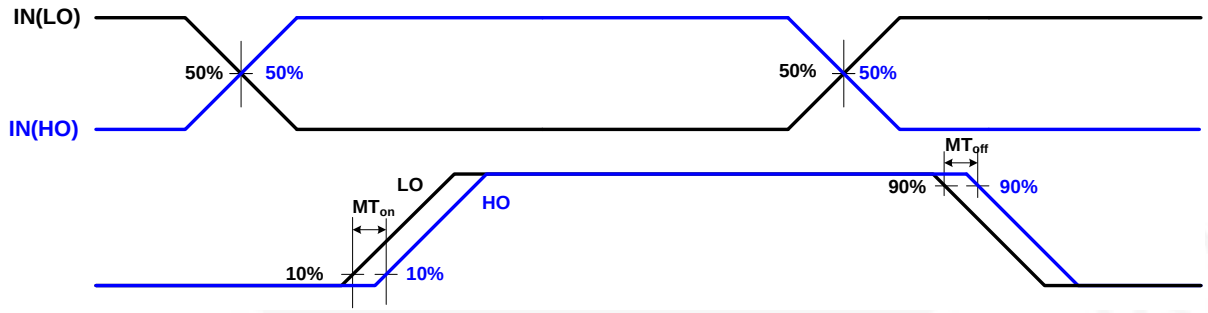


图 31. 延迟匹配波形定义

机械尺寸

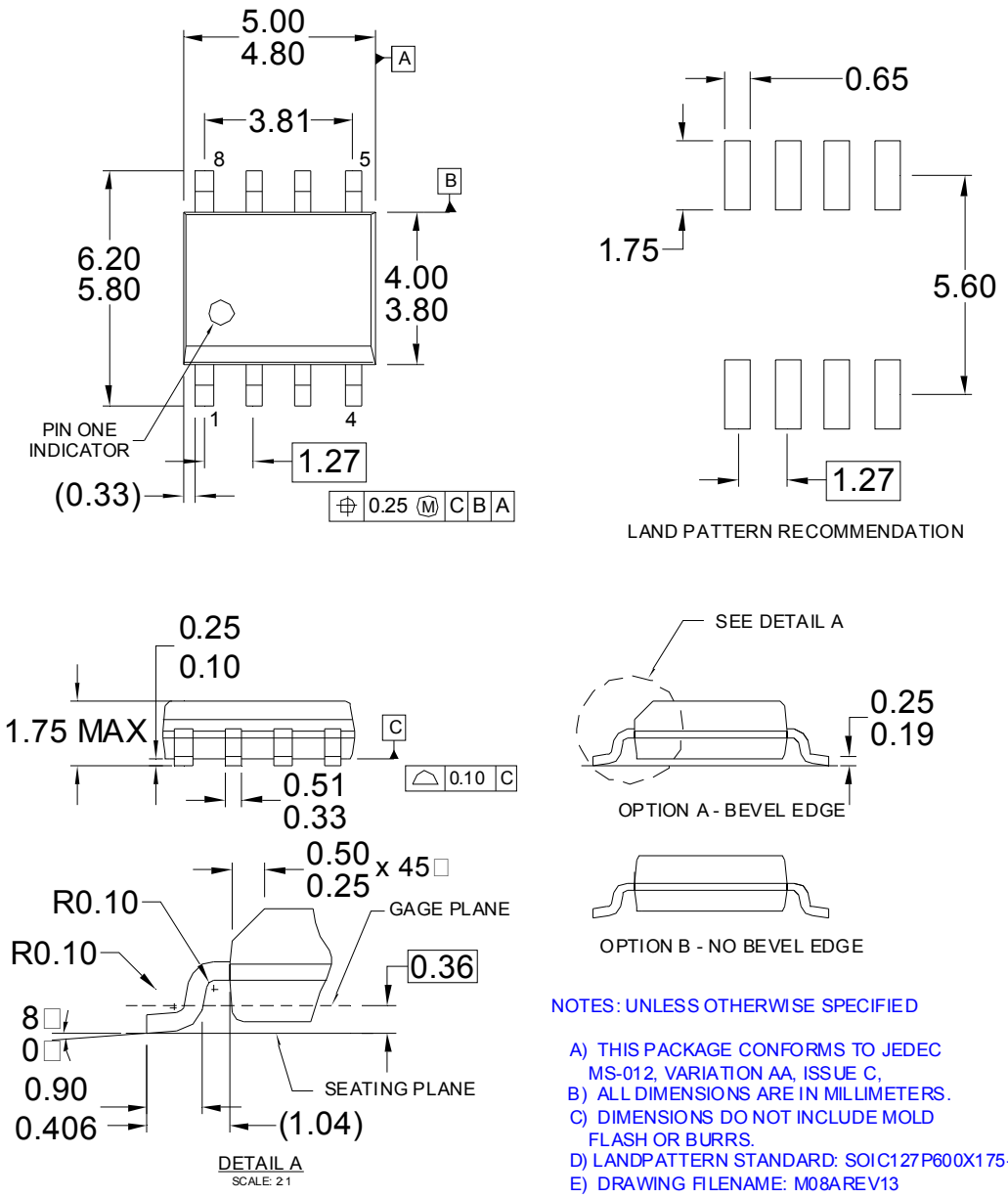


图 32. 8- 引脚小尺寸封装 (SOP)

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