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2015年6月

FAN7380 半桥栅极驱动器

FAN7380 — 半桥栅极驱动器

特性

- 浮动通道专为高达 +600 V 的自举运行而设计
- 两个通道的源 / 灌电流驱动能力典型值为 90 mA / 180 mA
- 共模 dv/dt 噪声消除电路
- 在 VCC=VBS= 15 V 时信号传播过程中, 扩展允许负 VS 摆幅低至 -9.8 V
- VCC 和 VBS 供电范围从 10 V 至 20 V
- 双通道的欠压锁定功能
- 兼容 TTL 的输入逻辑阈值电平
- 匹配传播延迟低于 50ns
- 内置 100ns 死区时间控制功能
- 输出信号与输入信号同相位

典型应用

- 荧光灯镇流器
- 紧凑型荧光灯镇流器

相关资源

- [AN-6076 — 高压栅极驱动 IC 自举电路的设计与应用指南](#)
- [AN-9052 — 自举元件选择的设计指南](#)
- [AN-8102 — 避免 HVIC 栅极驱动器应用中的短脉冲宽度问题的建议](#)

描述

FAN7380 是单片半桥栅极驱动 IC, 可以驱动工作电压最高达 +600 V 的 MOSFET 和 IGBT。飞兆的高压工艺和共模噪声消除技术可使高端驱动器在高 dv/dt 噪声环境下稳定运行。先进的电平转换电路, 能使高端栅极驱动器的工作电压在 $V_{BS}=15\text{ V}$ 时高达 $V_S = -9.8\text{ V}$ (典型值)。输入逻辑电平与标准 TTL 系列逻辑栅极兼容。内部击穿保护电路提供 100 ns 死区时间以阻止输出开关器件在转换期间不被导通。当 V_{CC} 和 V_{BS} 小于指定阈值电压时, 两个通道的欠压锁定 (UVLO) 电路可防止发生故障。输出驱动器的典型源电流 / 灌电流分别为 90 mA / 180 mA, 适合荧光灯 / 紧凑型荧光灯应用和要求低 di/dt 噪声的系统。

8-SOP



订购信息

器件	封装	无铅	工作温度	包装	描述
FAN7380MX ⁽¹⁾	8-SOP	是	-40°C ~ +125°C	卷带和卷盘	照明应用
FAN7380MX_OP ⁽¹⁾	8-SOP	是	-40°C ~ +125°C	卷带和卷盘	一般应用

说明:

1. 该器件已通过 JESD22A-111 波动焊接测试。

典型应用电路

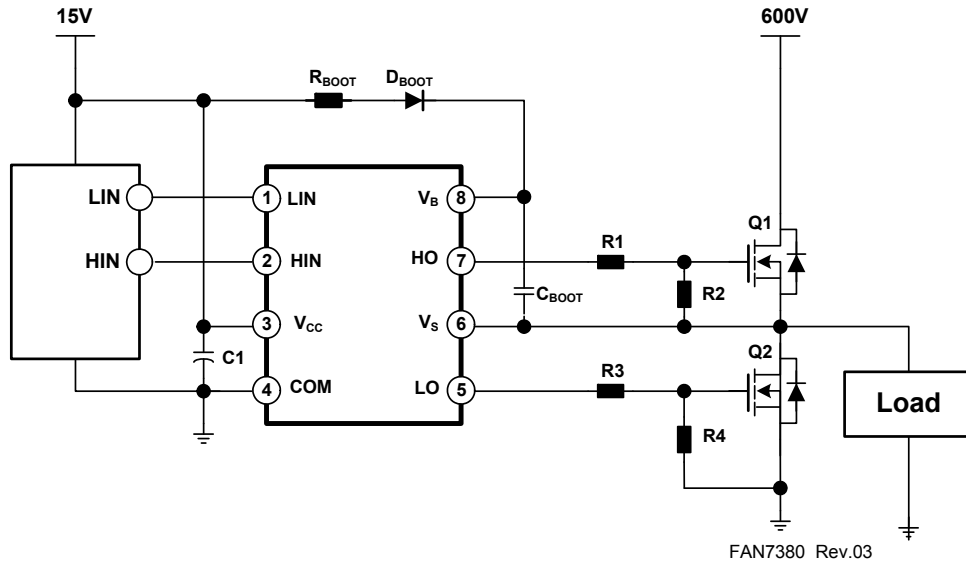


图 1. 荧光灯镇流器应用电路

内部框图

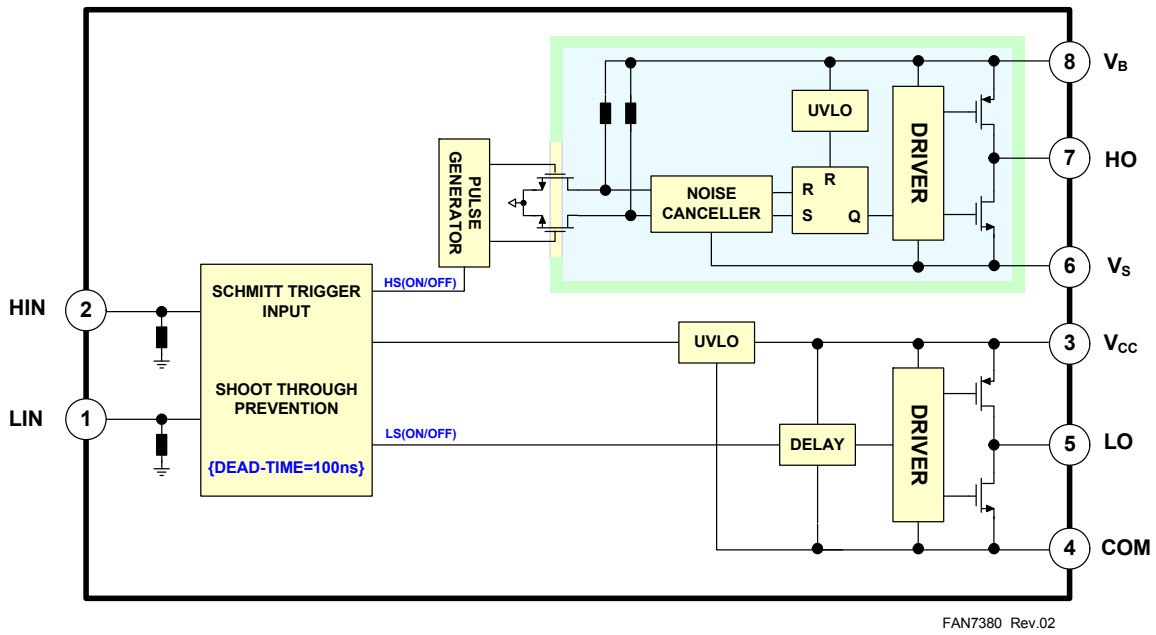


图 2. 功能框图

引脚配置

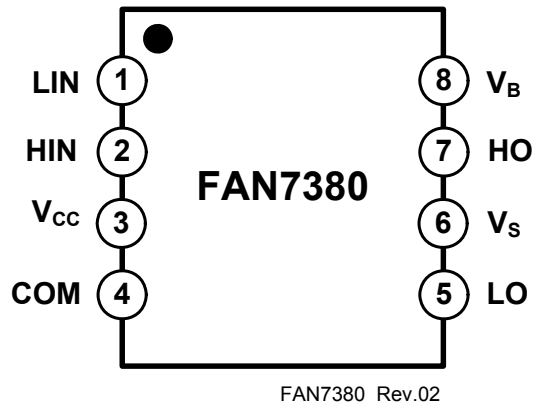


图 3. 引脚配置（俯视图）

引脚定义

引脚号	名称	I/O	描述
1	LIN	I	低侧栅极驱动器输出的逻辑输入
2	HIN	I	高侧栅极驱动器输出的逻辑输入
3	V _{CC}	I	低侧电源电压
4	COM		逻辑地和低侧驱动器返回
5	LO	O	低侧栅极输出
6	V _S	I	高侧浮动电源电压返回
7	HO	O	高侧驱动输出
8	V _B	I	高侧浮动电源

绝对最大额定值

应力超过绝对最大额定值，可能会损坏器件。在超出推荐的工作条件的情况下，该器件可能无法正常工作，所以不建议让器件在这些条件下长期工作。此外，长期在高于推荐的工作条件下工作，会影响器件的可靠性。绝对最大额定值仅是应力规格值。除非另有说明， $T_A=25^{\circ}\text{C}$ 。

符号	参数	最小值	最大值	单位
V_S	高侧偏置电压	V_B-25	$V_B+0.3$	V
V_B	高侧浮动电源电压	-0.3	625.0	
V_{HO}	高侧浮动输出电压 HO	$V_S-0.3$	$V_B+0.3$	
V_{CC}	低侧和固定逻辑电源电压	-0.3	25.0	
V_{LO}	低侧输出电压 LO	-0.3	$V_{CC}+0.3$	
V_{IN}	逻辑输入电压 (HIN、LIN)	-0.3	$V_{CC}+0.3$	
COM	逻辑地	$V_{CC}-25$	$V_{CC}+0.3$	
dV_S/dt	允许的偏置电压变化速率		50	V/ns
$P_D^{(2)(3)(4)}$	功耗		0.625	W
θ_{JA}	结至环境热阻		200	$^{\circ}\text{C}/\text{W}$
T_J	结温		150	$^{\circ}\text{C}$
T_S	存储温度	-50	150	$^{\circ}\text{C}$

注意：

2. 安装在 76.2 x 114.3 x 1.6 mm PCB 板上 (FR-4 环氧玻璃材料)。
3. 参考以下标准：
 - JESD51-2: 集成电路热测试方法环境条件 - 自然对流
 - JESD51-3: 含铅表面贴装封装的低有效导热系数测试板
4. 在任何情况下，都不要超过 P_D 。

推荐工作额定值

推荐的操作条件表明了器件的真实工作条件。指定建议工作条件是为了确保最佳性能。飞兆半导体建议不要超过推荐工作条件，也不能按照绝对最大额定值进行设计。

符号	参数	最小值	最大值	单位
V_B	高侧浮动电源电压	V_S+10	V_S+20	V
V_S	高侧浮动电源偏置电压	$6-V_{CC}$	600	
V_{HO}	高侧 (HO) 输出电压	V_S	V_B	
V_{LO}	低侧 (LO) 输出电压	COM	V_{CC}	
V_{IN}	逻辑输入电压 (HIN、LIN)	COM	V_{CC}	
V_{CC}	低侧电源电压	10	20	
T_A	环境温度	-40	125	$^{\circ}\text{C}$

静态电气特性

除非另有说明, $V_{BIAS} (V_{CC}, V_{BS}) = 15.0V$ 、 $T_A = 25^\circ C$ 。VIN 和 IIN 参数以 COM 为参考点。参数 VO 和 IO 以 V_S 和 COM 作为基准, 适用于相应的输出 HO 和 LO。

符号	参数	工作条件	最小值	典型值	最大值	单位
V_{CCUV+} V_{BSUV+}	V_{CC} 和 V_{BS} 电源欠压正向阈值		8.2	9.2	10.0	V
V_{CCUV-} V_{BSUV-}	V_{CC} 和 V_{BS} 电源欠压负向阈值		7.6	8.7	9.6	
V_{CCUVH} V_{BSUVH}	V_{CC} 电源欠压锁定滞回电压回差			0.5		
I_{LK}	偏置电源漏电流	$V_B = V_S = 600V$			50	μA
I_{QBS}	V_{BS} 静态电源电流	$V_{IN} = 0V$ or $5V$		44	100	
I_{QCC}	V_{CC} 静态电源电流	$V_{IN} = 0V$ or $5V$		70	180	
I_{PBS}	V_{BS} 工作电源电流	$f_{IN} = 20kHz?$ rms ?			600	μA
I_{PCC}	V_{CC} 工作电源电流	$f_{IN} = 20kHz?$ rms ?			610	
V_{IH}	逻辑“1”输入电压		2.5			V
V_{IL}	逻辑“0”输入电压				0.8	
V_{OH}	高电平输出电压, $V_{BIAS} - V_O$	$I_O = 20mA$			2.8	V
V_{OL}	低电平输出电压, V_O				1.2	
I_{IN+}	逻辑“1”输入偏置电流	$V_{IN} = 5V$		5	40	μA
I_{IN-}	逻辑“0”输入偏置电流	$V_{IN} = 0V$		1.0	2.0	
I_{O+}	输出高电平短路脉冲电流	$V_O = 0V, V_{IN} = 5V$ with $PW \leq 10\mu s$	60	90		mA
I_{O-}	输出低电平短路脉冲电流	$V_O = 15V, V_{IN} = 0V$ with $PW \leq 10\mu s$	130	180		
V_S	IN 信号传播到 HO 时允许的 V_S 引脚负电压			-9.8	-7.0	V

动态电气特性

除非另有规定, 否则 $V_{BIAS} (V_{CC}, V_{BS}) = 15.0V$ 、 $V_S = COM$ 、 $C_L = 1000pF$ 、 $T_A = 25^\circ C$ 。

符号	参数	工作条件	最小值	典型值	最大值	单位
t_{on}	导通传播延时	$V_S = 0V$	70	135	200	ns
t_{off}	关断传播延时	$V_S = 0V$ or $600V^{(5)}$	60	130	190	
t_r	导通上升时间		160	230	290	
t_f	关断下降时间		20	90	160	
DT	死区时间		80	120	190	
MT	延时匹配, HS 与 LS 导通 / 关断				50	

说明:

5. 该参数由设计保证。

典型性能特征

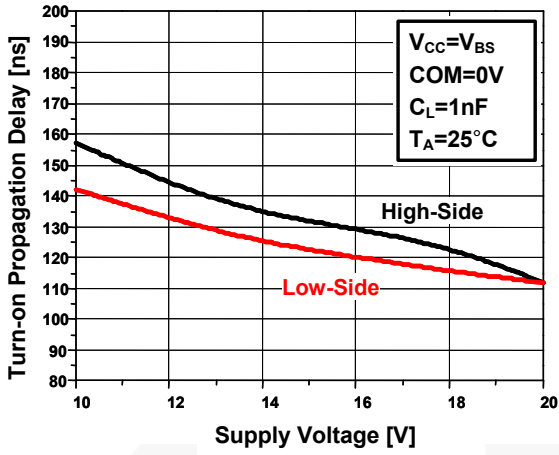


图 4. 导通传播延时与电源电压

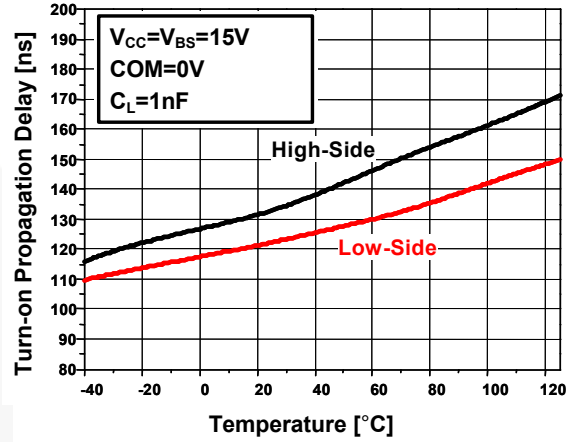


图 5. 导通传播延时与温度

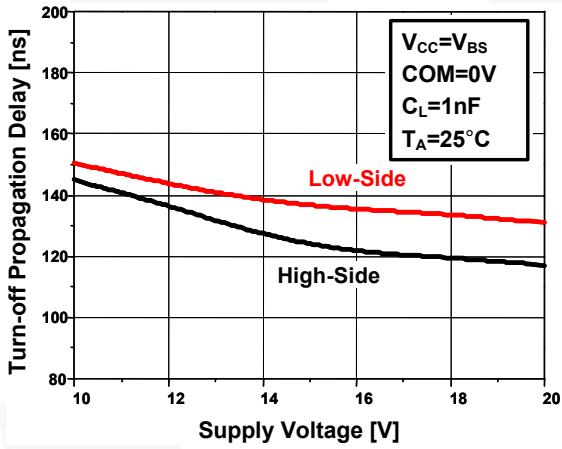


图 6. 关断传播延时与电源电压

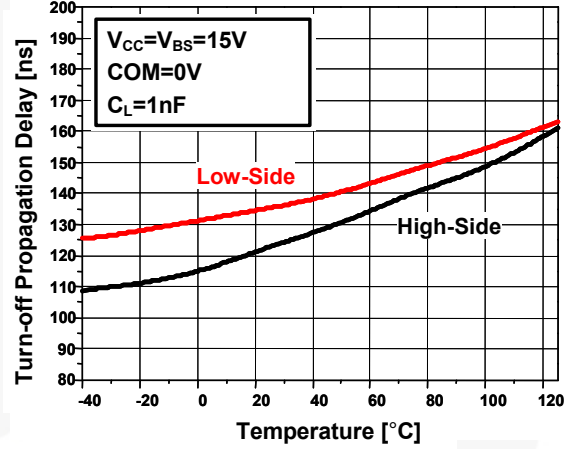


图 7. 关断传播延时与温度

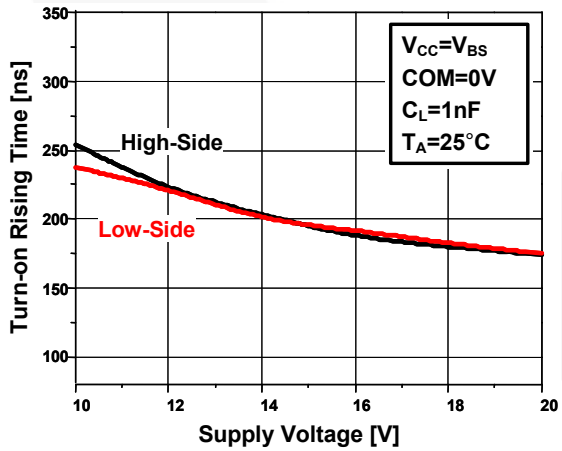


图 8. 导通上升时间与电源电压

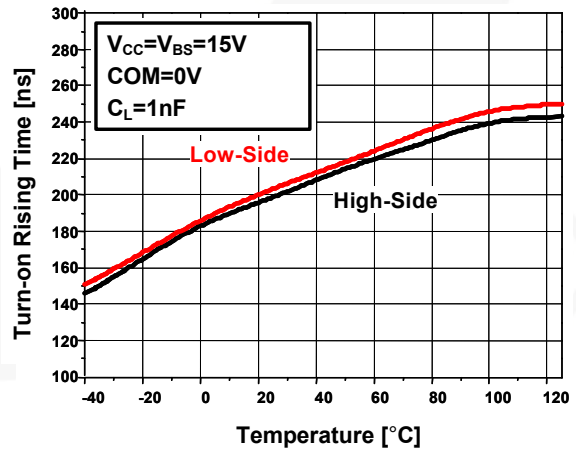


图 9. 导通上升时间与温度

典型性能特征 (接上页)

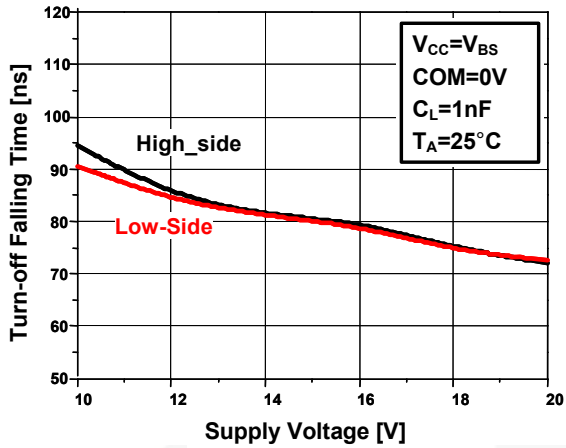


图 10. 关断下降时间与电源电压

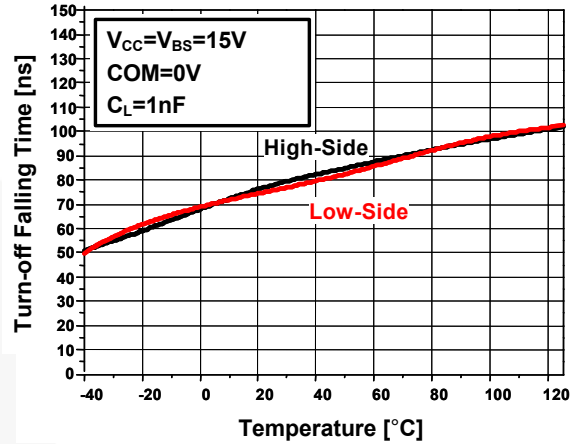


图 11. 关断下降时间与温度

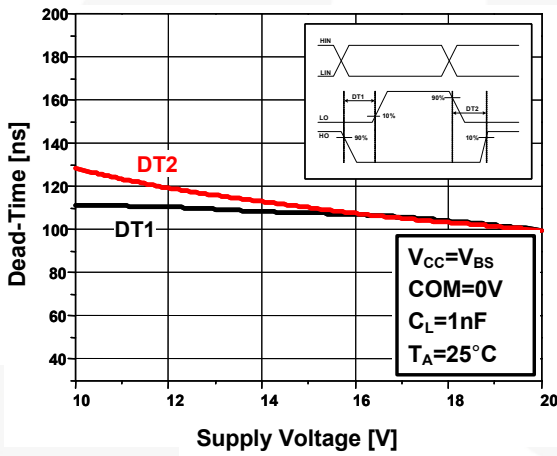


图 12. 死区时间与电源电压

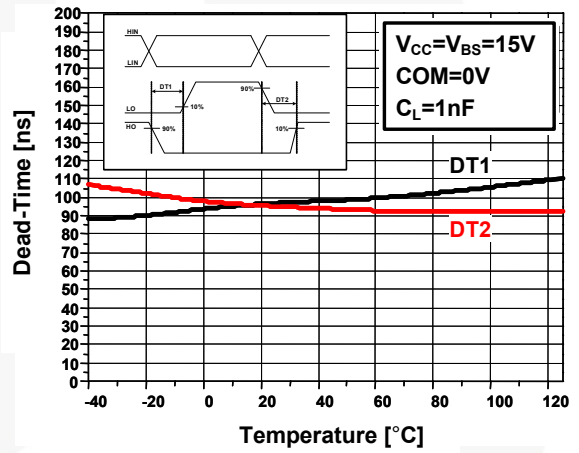


图 13. 死区时间与温度

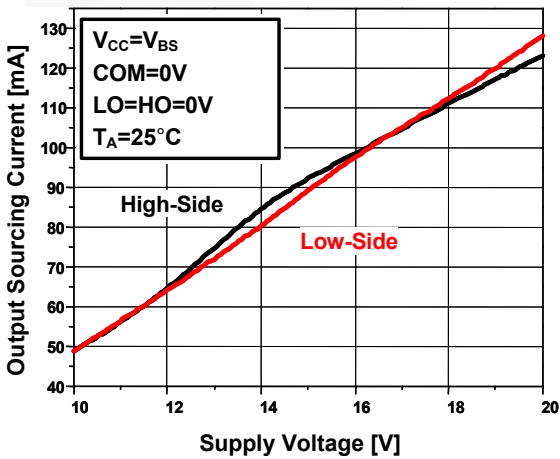


图 14. 输出源电流与电源电压

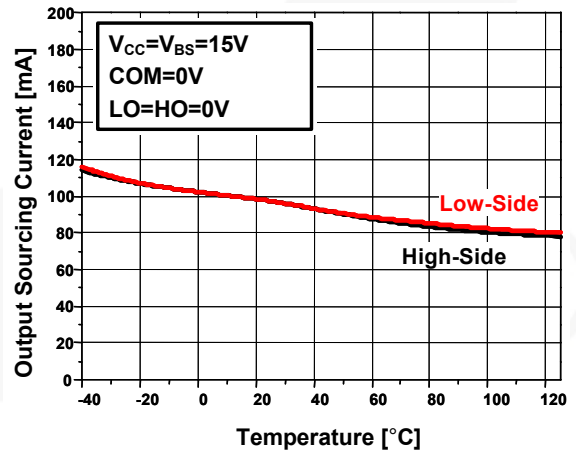


图 15. 输出源电流与温度

典型性能特征 (接上页)

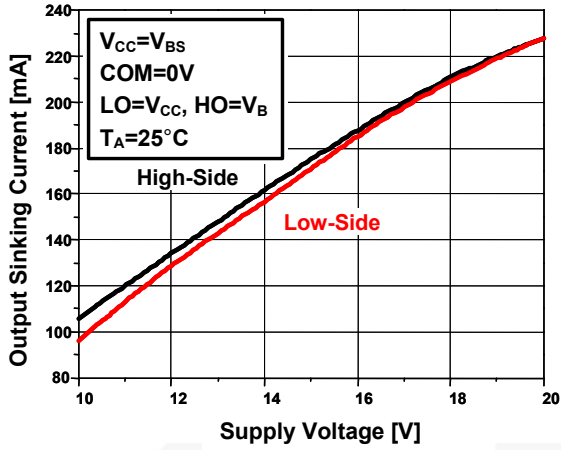


图 16. 输出灌电流与电源电压

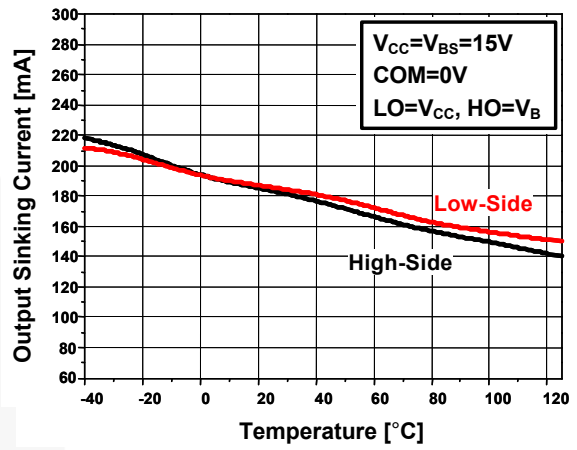


图 17. 输出灌电流与温度

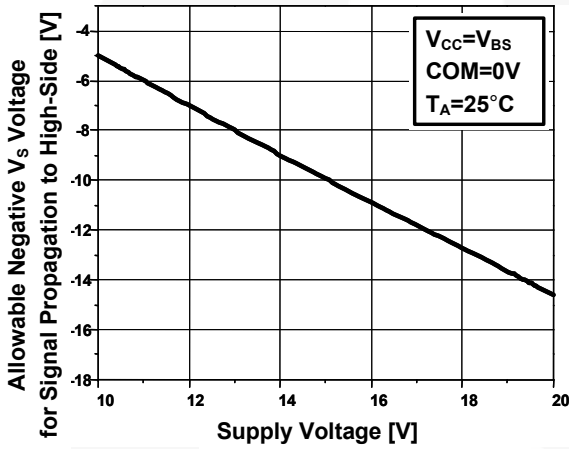


图 18. 信号传播至高端允许的 V_S 负电压与电源电压

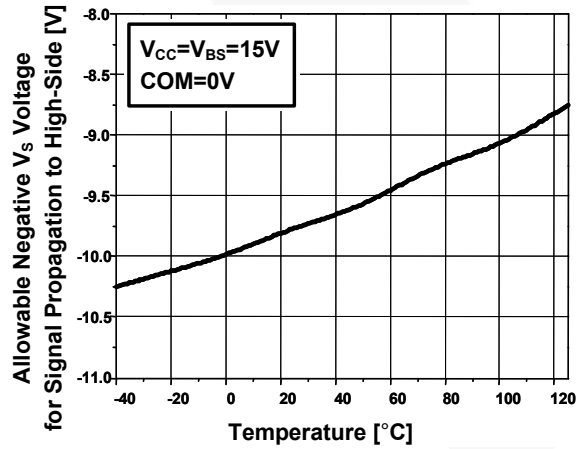


图 19. 信号传播至高端允许的 V_S 负电压与温度的关系

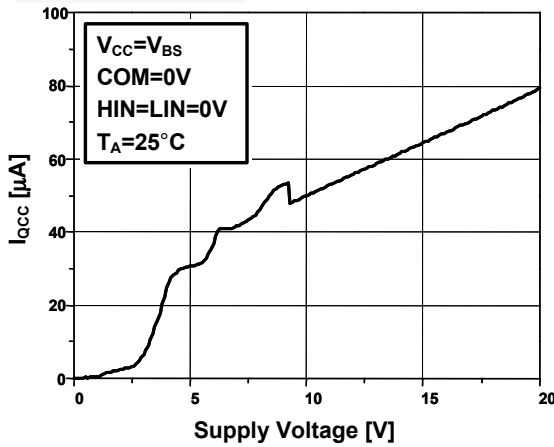


图 20. I_{QCC} 与 电源电压

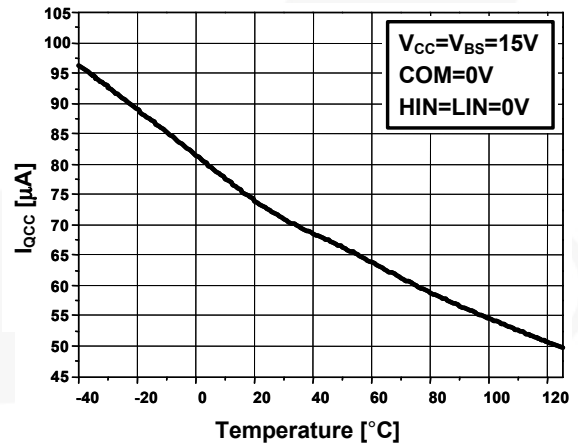


图 21. I_{QCC} 与 温度的关系

典型性能特征 (接上页)

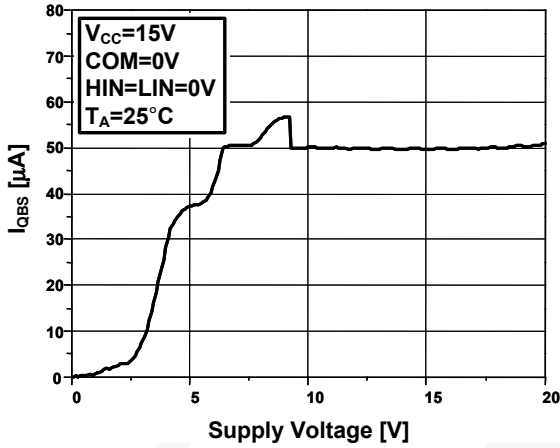


图 22. I_{QBS} 与电源电压

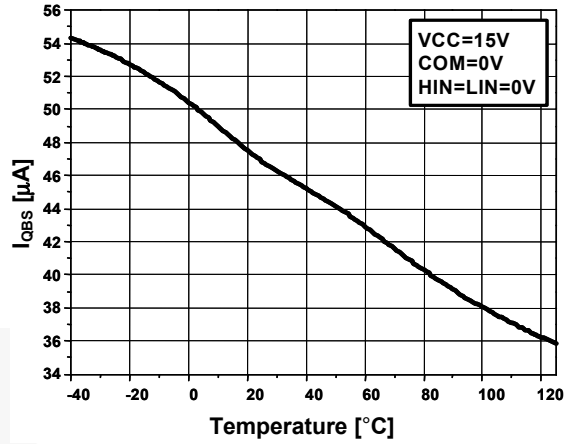


图 23. I_{QBS} 与温度的关系

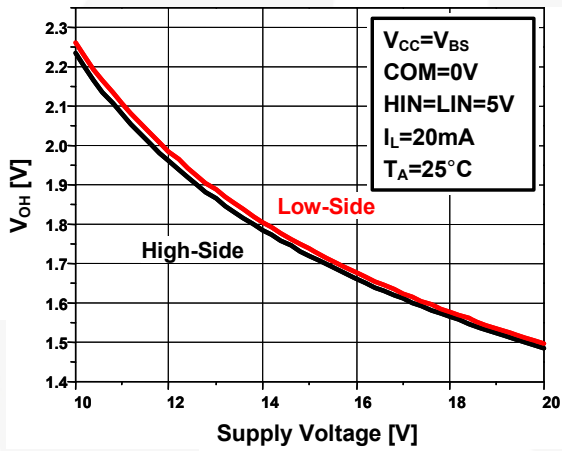


图 24. 高电平输出电压与电源电压

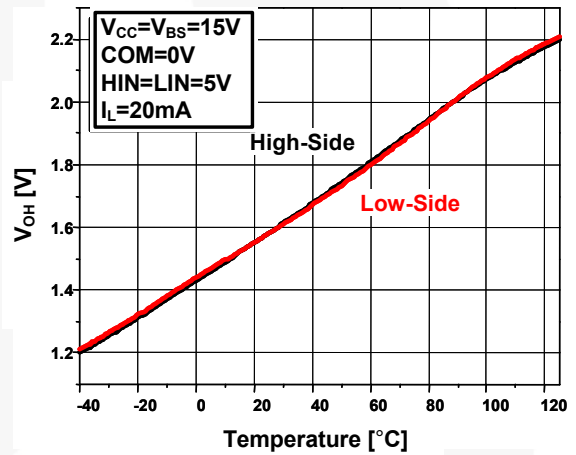


图 25. 高电平输出电压与温度

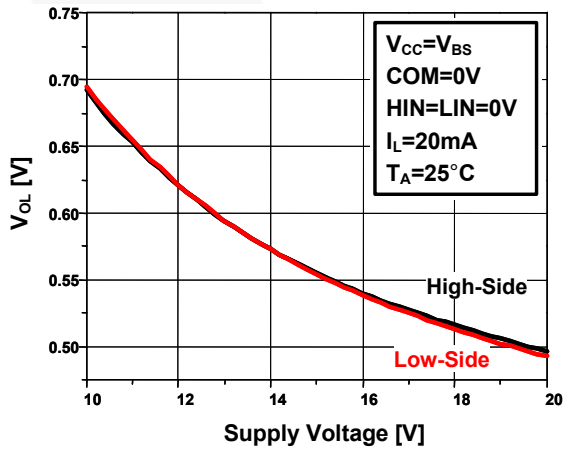


图 26. 低电平输出电压与电源电压

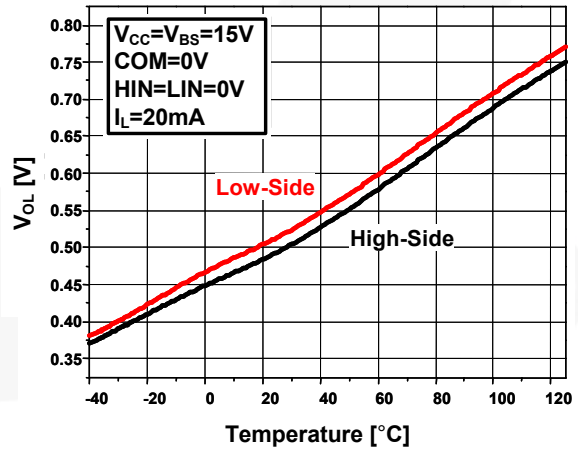


图 27. 低电平输出电压与温度

典型性能特征 (接上页)

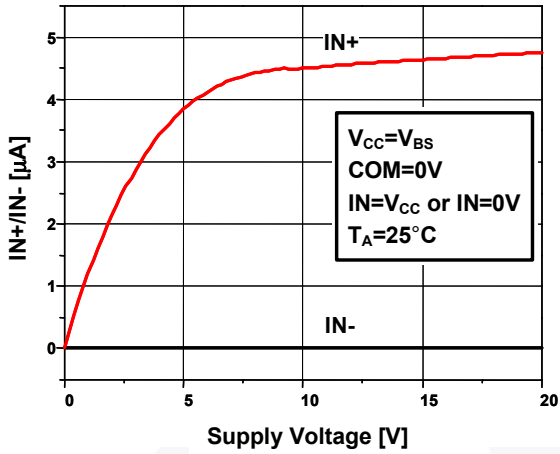


图 28. 输入偏置电流与电源电压

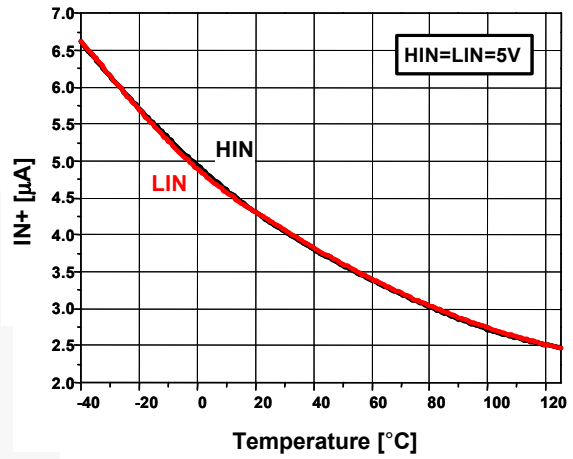


图 29. 输入偏置电流与温度的关系

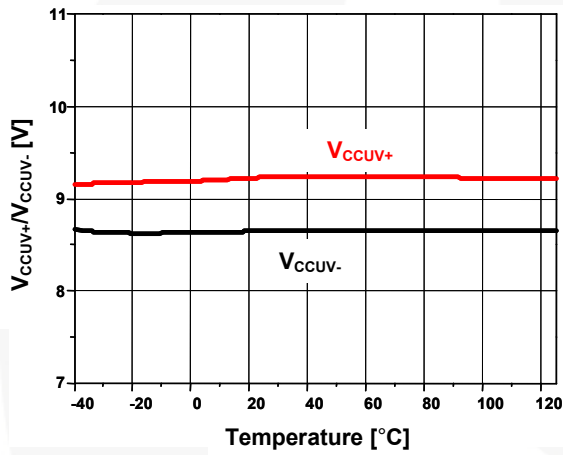


图 30. V_{CC} UVLO 阈值电压与温度

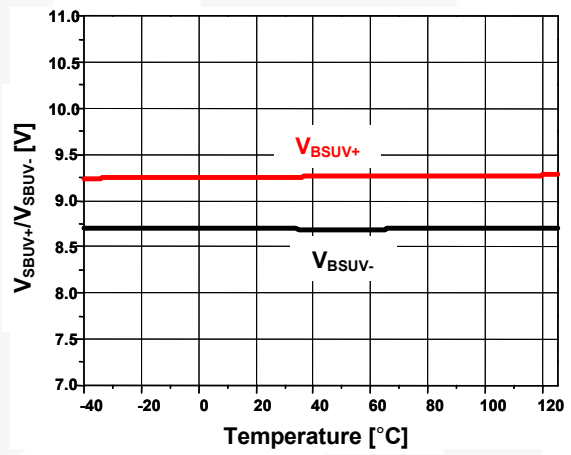


图 31. V_{BS} UVLO 阈值电压与温度

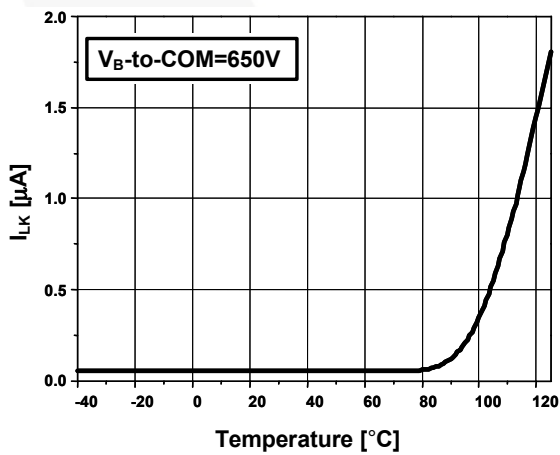


图 32. VB 至 COM 漏电流与温度

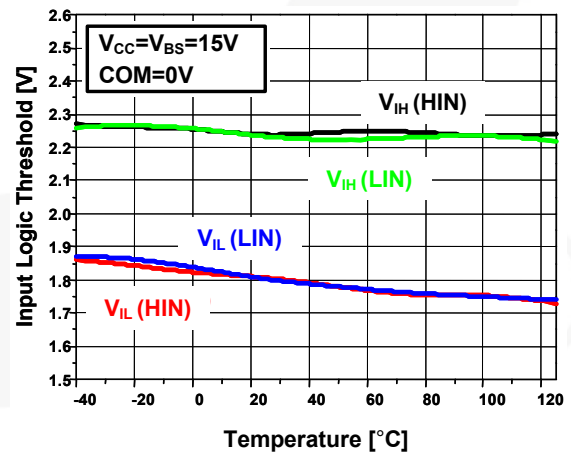


图 33. 输入逻辑阈值与温度

开关时间定义

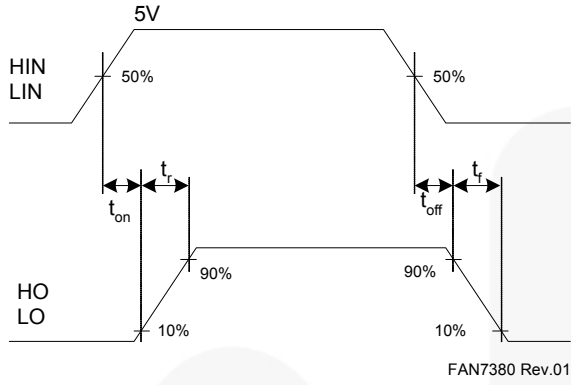


图 34. 开关时间波形

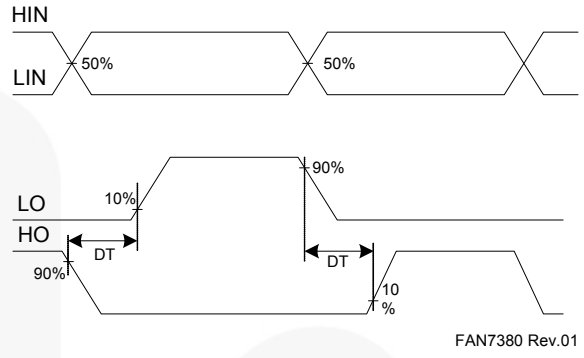


图 35. 内部死区时间时序



TOP VIEW



LAND PATTERN RECOMMENDATION



FRONT VIEW



OPTION A
BEVEL EDGE

OPTION B
NON-BEVEL EDGE

SIDE VIEW



DETAIL "B"
SCALE 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

- A. THIS PACKAGE CONFORMS TO JEDEC MS-012 VARIATION A EXCEPT WHERE NOTED.
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