



Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

74VCX162373

Low Voltage 16-Bit Transparent Latch with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistors in Outputs

General Description

The VCX162373 contains sixteen non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear to be transparent to the data when the Latch enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH, the outputs are in a high impedance state.

The VCX162373 is also designed with 26Ω resistors in the outputs. This design reduces line noise in applications such as memory address drivers, clock drivers and bus transceivers/transmitters.

The 74VCX162373 is designed for low voltage (1.4V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V.

The 74VCX162373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.4V–3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- 26Ω series resistors in outputs
- t_{PD} (I_n to O_n)
3.3 ns max for 3.0V to 3.6V V_{CC}
- Power-off high impedance inputs and outputs
- Support live insertion and withdrawal (Note 1)
- Static Drive (I_{OH}/I_{OL})
±12 mA @ 3.0V V_{CC}
- Uses proprietary noise/EMI reduction circuitry
- Latch-up performance exceeds 300 mA
- ESD performance:
Human body model > 2000V
Machine model > 200V

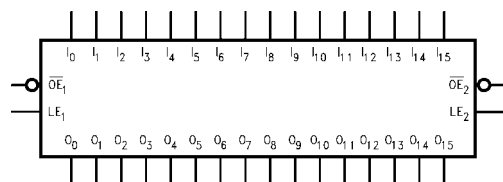
Note 1: To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Ordering Number	Package Number	Package Description
74VCX162373MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

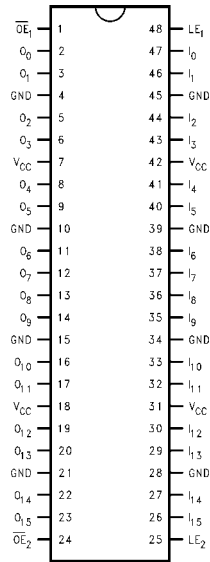
Logic Symbol



Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active LOW)
LE_n	Latch Enable Input
I_0 – I_{15}	Inputs
O_0 – O_{15}	Outputs

Connection Diagram



Truth Tables

Inputs			Outputs
LE ₁	\overline{OE}_1	I ₀ -I ₇	O ₀ -O ₇
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O ₀

Inputs			Outputs
LE ₂	\overline{OE}_2	I ₈ -I ₁₅	O ₈ -O ₁₅
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O ₀

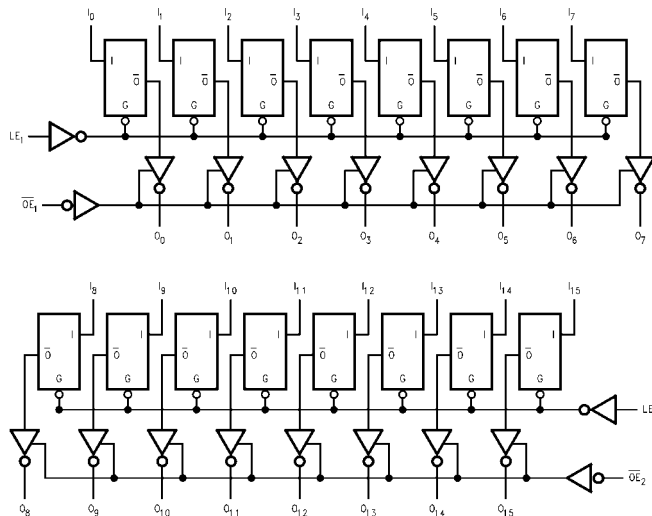
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial (HIGH or LOW, inputs may not float)
 Z = High Impedance
 O₀ = Previous O₀ before HIGH-to-LOW of Latch Enable

Functional Description

The 74VCX162373 contains sixteen edge D-type latches with 3-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the I_n enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time

its I input changes. When LE_n is LOW, the latches store information that was present on the I inputs a setup time preceding the HIGH-to-LOW transition on LE_n. The 3-STATE outputs are controlled by the Output Enable (\overline{OE}_n) input. When \overline{OE}_n is LOW the standard outputs are in the 2-state mode. When \overline{OE}_n is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	-0.5V to +4.6V
DC Input Voltage (V_I)	-0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-STATED	-0.5V to +4.6V
Outputs Active (Note 3)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current (I_{IK}) $V_I < 0V$	-50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	± 50 mA
DC V_{CC} or GND Current per	
Supply Pin (I_{CC} or GND)	± 100 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C

Recommended Operating Conditions (Note 4)

Power Supply	
Operating	1.4V to 3.6V
Input Voltage	-0.3V to +3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in "OFF" State	0.0V to 3.6V
Output Current in I_{OH}/I_{OL}	
$V_{CC} = 3.0V$ to 3.6V	± 12 mA
$V_{CC} = 2.3V$ to 2.7V	± 8 mA
$V_{CC} = 1.65V$ to 2.3V	± 3 mA
$V_{CC} = 1.4V$ to 1.6V	± 1 mA
Free Air Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Floating or unused inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	Min	Max	Units
			(V)			
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
			2.3 - 2.7	1.6		
			1.65 - 2.3	$0.65 \times V_{CC}$		
			1.4 - 1.6	$0.65 \times V_{CC}$		
V_{IL}	LOW Level Input Voltage		2.7 - 3.6		0.8	V
			2.3 - 2.7		0.7	
			1.65 - 2.3		$0.35 \times V_{CC}$	
			1.4 - 1.6		$0.35 \times V_{CC}$	
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.7 - 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -6$ mA	2.7	2.2		
		$I_{OH} = -8$ mA	3.0	2.4		
		$I_{OH} = -12$ mA	3.0	2.2		
		$I_{OH} = -100 \mu A$	2.3 - 2.7	$V_{CC} - 0.2$		
		$I_{OH} = -4$ mA	2.3	2.0		
		$I_{OH} = -6$ mA	2.3	1.8		
		$I_{OH} = -8$ mA	2.3	1.7		
		$I_{OH} = -100 \mu A$	1.65 - 2.3	$V_{CC} - 0.2$		
		$I_{OH} = -3$ mA	1.65	1.25		
		$I_{OH} = -100 \mu A$	1.4 - 1.6	$V_{CC} - 0.2$		
		$I_{OH} = -1$ mA	1.4	1.05		

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC}	Min	Max	Units
			(V)			
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.7 - 3.6		0.2	V
		I _{OL} = 6 mA	2.7	0.4		
		I _{OL} = 8 mA	3.0	0.55		
		I _{OL} = 12 mA	3.0	0.8		
		I _{OL} = 100 μA	2.3 - 2.7	0.2		
		I _{OL} = 6 mA	2.3	0.4		
		I _{OL} = 8 mA	2.3	0.6		
		I _{OL} = 100 μA	1.65 - 2.3	0.2		
		I _{OL} = 3 mA	1.65	0.3		
		I _{OL} = 100 μA	1.4 - 1.6	0.2		
		I _{OL} = 1 mA	1.4	0.35		
I _I	Input Leakage Current	0 ≤ V _I ≤ 3.6V	1.4 - 3.6		±5.0	μA
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 3.6V, V _I = V _{IH} or V _{IL}	1.4 - 3.6		±10.0	μA
I _{OFF}	Power-OFF Leakage Current	0 ≤ (V _I , V _O) ≤ 3.6V	0		10.0	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	1.4 - 3.6		20.0	μA
		V _{CC} ≤ (V _I , V _O) ≤ 3.6V (Note 5)	1.4 - 3.6		±20.0	μA
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.7 - 3.6		750	μA

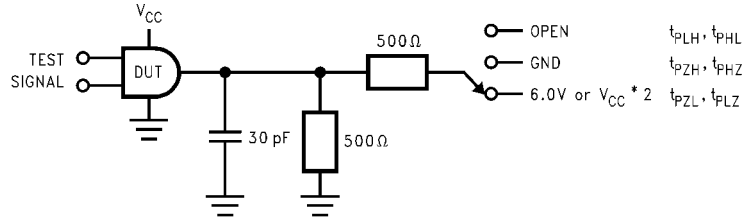
Note 5: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 6)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units	Figure Number
				Min	Max		
t _{PHL} t _{PLH}	Propagation Delay LE to O _n	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.8	3.6	ns	Figures 1, 2
			2.5 ± 0.2	1.0	4.9		
			1.8 ± 0.15	1.5	9.8		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	19.6		Figures 7, 8
t _{PHL} t _{PLH}	Propagation Delay I _n to O _n	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.8	3.3	ns	Figures 1, 2
			2.5 ± 0.2	1.0	4.5		
			1.8 ± 0.15	1.5	9.0		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	18.0		Figures 7, 8
t _{PZL} t _{PZH}	Output Enable Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.8	3.9	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	5.4		
			1.8 ± 0.15	1.5	9.8		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	19.6		Figures 7, 9, 10
t _{PLZ} t _{PHZ}	Output Disable Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.8	4.0	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	4.4		
			1.8 ± 0.15	1.5	7.9		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	15.8		Figures 7, 9, 10
t _S	Setup Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	1.5		ns	Figures 1, 6
			2.5 ± 0.2	1.5			
			1.8 ± 0.15	2.5			
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	3.0			Figures 6, 7
t _H	Hold Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	1.0		ns	Figures 1, 6
			2.5 ± 0.2	1.0			
			1.8 ± 0.15	1.0			
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	2.0			Figures 6, 7

AC Electrical Characteristics (Continued)							
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units	Figure Number
				Min	Max		
t _w	Pulse Width	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	1.5		ns	Figures 1, 5
			2.5 ± 0.2	1.5			
			1.8 ± 0.15	4.0			
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	4.0			Figures 5, 7
t _{OSSL}	Output to Output Skew (Note 7)	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3		0.5	ns	
t _{OSLH}			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
			1.5 ± 0.1		1.5		
<p>Note 6: For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.</p> <p>Note 7: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}).</p>							
Dynamic Switching Characteristics							
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C		Units	
				Typical			
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	0.15		V	
			2.5	0.25			
			3.3	0.35			
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	-0.15		V	
			2.5	-0.25			
			3.3	-0.35			
V _{OHV}	Quiet Output Dynamic Valley V _{OH}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	1.55		V	
			2.5	2.05			
			3.3	2.65			
Capacitance							
Symbol	Parameter	Conditions	T _A = +25°C		Units		
			Typical				
C _{IN}	Input Capacitance	V _{CC} = 1.8V, 2.5V or 3.3V, V _I = 0V or V _{CC}	6		pF		
C _{OUT}	Output Capacitance	V _I = 0V or V _{CC} , V _{CC} = 1.8V, 2.5V or 3.3V	7		pF		
C _{PD}	Power Dissipation Capacitance	V _I = 0V or V _{CC} , f = 10 MHz, V _{CC} = 1.8V, 2.5V or 3.3V	20		pF		

AC Loading and Waveforms (V_{CC} 3.3V ± 0.3V to 1.8V ± 0.15V)



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$; $V_{CC} * 2$ at $V_{CC} = 2.5 \pm 0.2V; 1.8V \pm 0.15V$
t_{PZH}, t_{PHZ}	GND

FIGURE 1. AC Test Circuit

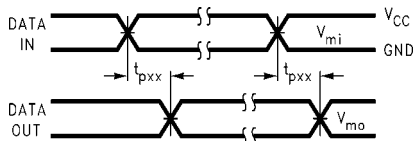


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

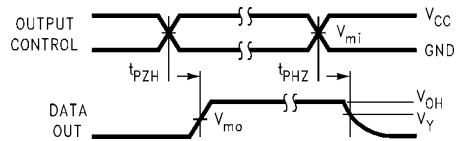


FIGURE 3. 3-STATE Output HIGH Enable and Disable Times for Low Voltage Logic

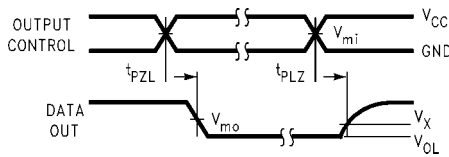


FIGURE 4. 3-STATE Output LOW Enable and Disable Times for Low Voltage Logic

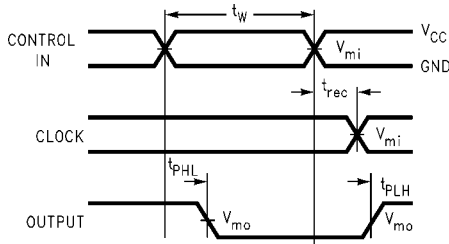


FIGURE 5. Propagation Delay, Pulse Width and t_{REC} Waveforms

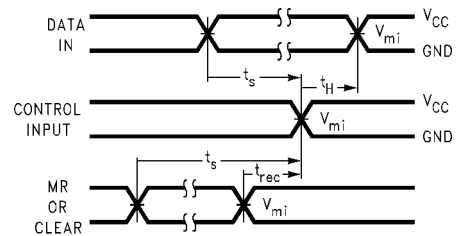
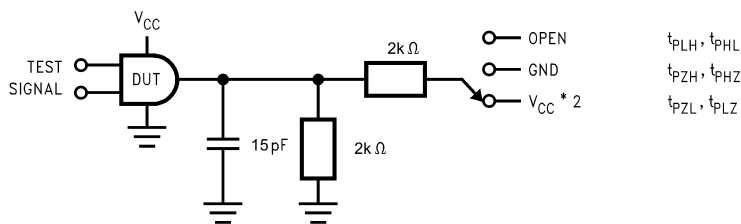


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Symbol	V_{CC}		
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

AC Loading and Waveforms ($V_{CC} 1.5V \pm 0.1V$)



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	$V_{CC} \times 2$ at $V_{CC} = 1.5V \pm 0.1V$
t_{PZH}, t_{PHZ}	GND

FIGURE 7. AC Test Circuit

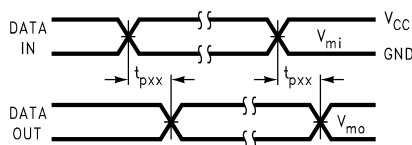


FIGURE 8. Waveform for Inverting and Non-Inverting Functions

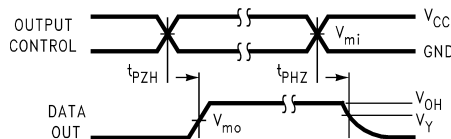


FIGURE 9. 3-STATE Output HIGH Enable and Disable Times for Low Voltage Logic

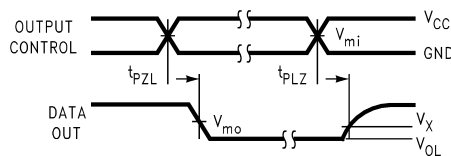
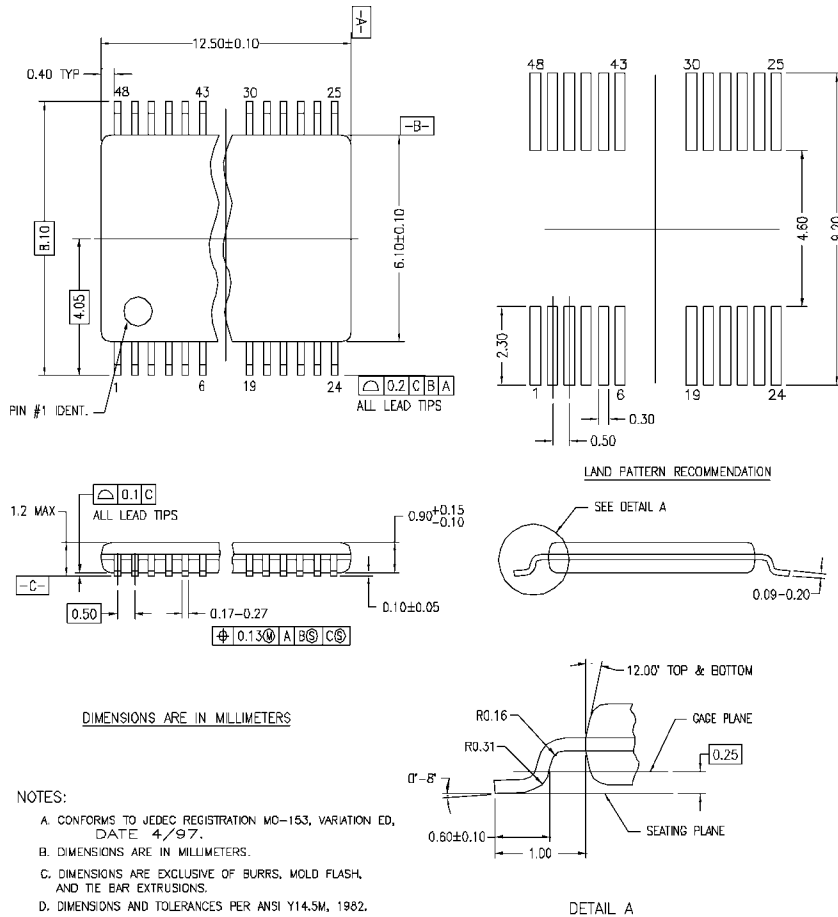


FIGURE 10. 3-STATE Output LOW Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}
	$1.5V \pm 0.1V$
V_{mi}	$V_{CC}/2$
V_{mo}	$V_{CC}/2$
V_X	$V_{OL} + 0.1V$
V_Y	$V_{OH} - 0.1V$

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ED, DATE 4/97.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
 - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48REV C

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative