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FAIRCHILD SEMICONDUCTOR®

June 2014

# FSA641 – 2:1 MIPI 开关，配备 2-数据和 1-数据线路

## 特性

- 开关类型:2:1
- 信号类型:MIPI, DPHY
- $V_{CC}$: 2.65 到 4.3 V
- 输入信号　　0 to $V_{CC}$
- $R_{ON}$:
  - 7 Ω 典型 HS MIPI
  - 10 Ω 典型 LS MIPI
- $\Delta R_{ON}$: 0.75 Ω 典型 HS & LS MIPI
- $I_{CC}$ :1 μA（最大值）
- $O_{IRR}$: 50 dB（典型值）
- $X_{TALK}$: 40 dB（典型值）
- 带宽: 1 GHz（典型值）
- 通道间相位差: 15 ps（典型值）
- $C_{ON}$: 8 pF（典型值）
- 封装20-引脚 UMLP

## 应用

- 移动电话，智能电话
- 显示屏

## 说明

FSA641 是一款 2:1 MIPI 开关，针对 2 数据通道和 1 数据通道模块设计。该部件配置为单刀双掷开关 (SPDT)，经过优化用于在两个高速或低功耗 MIPI 源之间进行切换。FSA641 特别针对 MIPI 规格设计，可连接至 CSI 或 DSI 模块。FSA641 具有 8 pF 的极低导通电容 ($C_{ON}$)。宽带宽 (1 GHz) 使信号具有更小的边缘和相位失真。出色的通道间串扰性能可实现最小的干扰。

## 相关资源

- 有关样品、疑问，请联系：Analog.Switch@fairchildsemi.com。
- FSA641 展示板

## 订购信息

| 器件编号 | 顶标 | 工作温度范围 | 封装 |
|---|---|---|---|
| FSA641UMX | F641 | -40 至 +85° C | 20-引脚，方形，超薄膜塑无铅封装 (UMLP)，3.0 x 3.0 mm |

## 典型应用

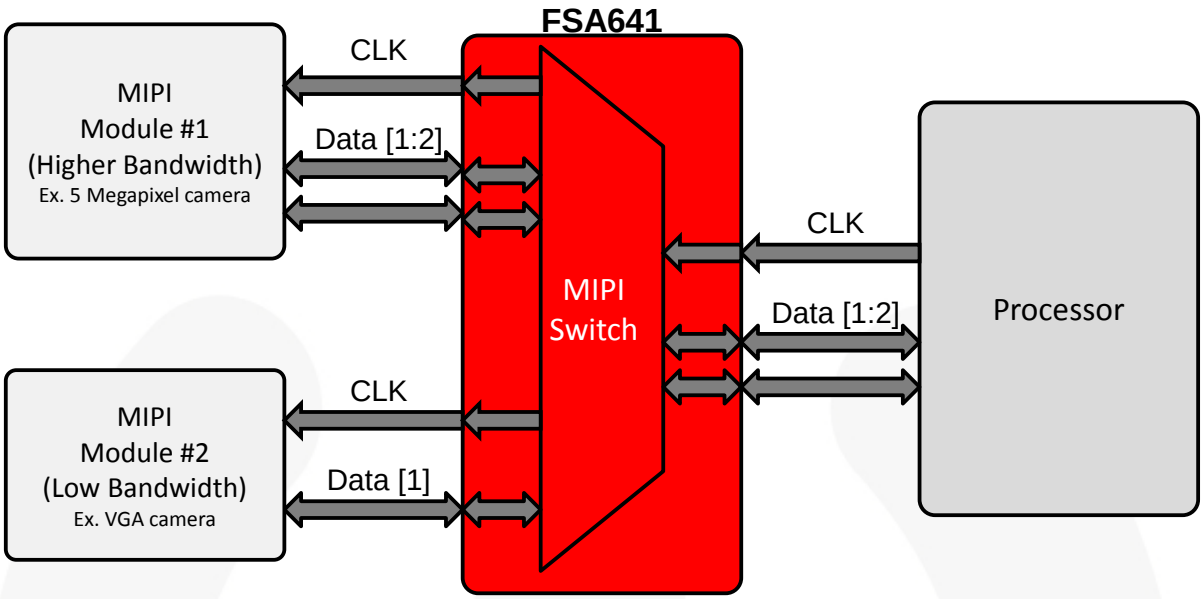



图 1. 移动电话示例

## 引脚布局

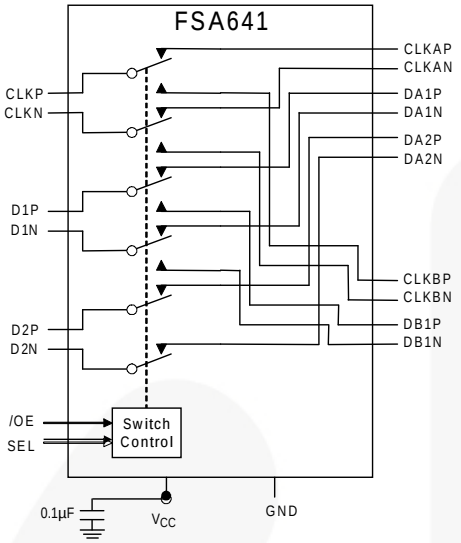



图 2. 功能框图

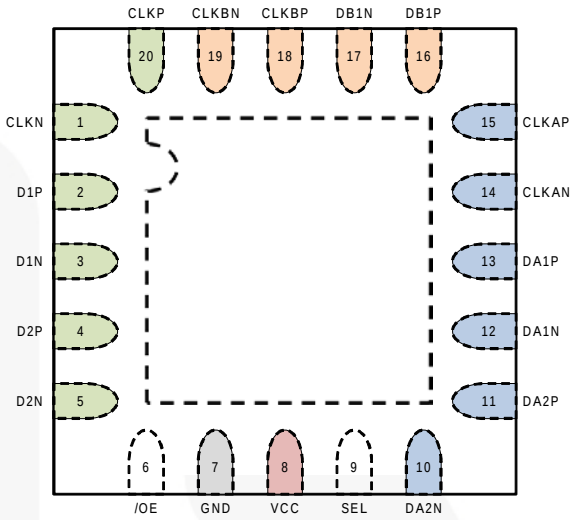



图 3. 引脚分配（俯视图）

## 引脚描述

| 引脚号 | 引脚名 | 类型 | 说明 | |
|---|---|---|---|---|
| 20 | CLKP | I/O | 时钟路径公共正端 | |
| 1 | CLKN | I/O | 时钟路径公共负端 | |
| 2 | D1P | I/O | 数据1路径公共正端 | |
| 3 | D1N | I/O | 数据1路径公共负端 | |
| 4 | D2P | I/O | 数据2路径公共正端 | |
| 5 | D2N | I/O | 数据2路径公共负端 | |
| 15 | CLKAP | I/O | 正向时钟路径A端口 | |
| 14 | CLKAN | I/O | 负向时钟路径A端口 | |
| 13 | DA1P | I/O | 正向数据1路径 A 端口 | |
| 12 | DA1N | I/O | 负向数据1路径 A 端口 | |
| 11 | DA2P | I/O | 正向数据2路径 A 端口 | |
| 10 | DA2N | I/O | 负向数据2路径 A 端口 | |
| 18 | CLKBP | I/O | 正向时钟路径 B 端口 | |
| 19 | CLKBN | I/O | 负向时钟路径 B 端口 | |
| 16 | DB1P | I/O | 正向数据1路径 B 端口 | |
| 17 | DB1N | I/O | 负向数据1路径 B 端口 | |
| 6 | /OE | 输入 | 输出使能（低电平有效） | |
| 7 | GND | 接地 | 接地 | |
| 8 | VCC | 电源 | 功率；推荐 0.1 µF 去耦电容器接地 | |
| 9 | SEL | 输入 | A 端口或 B 端口选择引脚 | 0=A-端口，1= B-端口 |
| 引脚座 | 不适用 | NC | 未连接 | |

## 真值表

| SEL | /OE | 功能 |
|---|---|---|
| 无关 | 高 | 未连接 |
| 低 | 低 | D1，D2，CLK=DA1，DA2，CLKA |
| 高 | 低 | D1，CLK=DB1，CLKB；D2 OPEN |

## 绝对最大额定值

应力超过绝对最大额定值，可能会损坏设备。在超出推荐的工作条件的情况下，该器件可能无法正常运行或操作，且不建议让器件在这些条件下长期工作。此外，过度暴露在高于推荐的工作条件下，会影响器件的可靠性。绝对最大额定值仅是额定应力值。

| 符号 | 参数 | | 最小值 | 最大值 | 单位 |
|---|---|---|---|---|---|
| $V_{CC}$ | 电源电压 | | -0.50 | +5.25 | V |
| $V_{CNTRL}$ | DC 输入电压 (SEL, /OE) (1) | | -0.5 | $V_{CC}$ | V |
| $V_{SW}$ | 直流开关I/O电压 (1) | | -0.5 | $V_{CC}$ + 0.3 | V |
| $I_{IK}$ | 直流输入二极管电流 | | -50 | | mA |
| $I_{OUT}$ | 直流输出电流 | | | 50 | mA |
| $T_{STG}$ | 存储温度 | | -65 | +150 | °C |
| ESD | 人体模型，JEDEC: JESD22-A114 | 全部引脚 | | 6.5 | kV |
| | | 输入/输出至地 | | 8.0 | |
| | | 电源至地 | | 16.0 | |
| | 充电器件模型，JEDEC: JESD22-C101 | | | 2.0 | |

**注意：**

1. 当测量输入与输出二极管电流额定值时，该输入与输出可能超出负额定值。

## 推荐工作条件

推荐的操作条件表定义了器件的真实工作条件。指定推荐的工作条件，以确保设备的最佳性能达到数据表中的规格。飞兆半导体建议不要超过推荐工作条件，也不能按照绝对最大额定值进行设计。

| 符号 | 参数 | 最小值 | 最大值 | 单位 |
|---|---|---|---|---|
| $V_{CC}$ | 电源电压 | 2.65 | 4.30 | V |
| $V_{CNTRL}$ | 控制输入电压 (SEL, /OE) (2) | 0 | $V_{CC}$ | V |
| $V_{SW}$ | 开关I/O电压 | -0.5 | $V_{CC}$ | V |
| $T_A$ | 工作温度 | -40 | +85 | °C |

**注意：**

2. 控制输入必须保持高电平或低电平，不允许浮动。

## 直流电气特性

若无其他说明，所有典型值都在 $T_A$=25° C 下测得。

| 符号 | 参数 | 工作条件 | $V_{CC}$ (V) | $T_A$=-40 至 +85°C | | | 单位 |
|---|---|---|---|---|---|---|---|
| | | | | 最小值 | 典型值 | 最大值 | |
| $V_{IK}$ | 箝位二极管电压 | $I_{IN}$=-18 mA | 2.775 | | | -1.2 | V |
| $I_{IN}$ | 控制脚输入漏电流 | $V_{SW}$=0 至 4.3 V | 4.3 | -1 | | 1 | μA |
| $V_{IH}$ | 输入电压高电平 | $V_{IN}$=0 至 $V_{CC}$ | 2.650 至 2.775 | 1.3 | | | V |
| | | | 4.3 | 1.7 | | | |
| $V_{IL}$ | 输入电压低电平 | $V_{IN}$=0 至 $V_{CC}$ | 2.650 至 2.775 | | | 0.5 | V |
| $I_{OZ}$ | 关断漏电流 | A, B=0+0.3 V to $V_{CC}$-0.3 | 4.3 | -2 | | 2 | μA |
| $I_{CC}$ | 静态电源电流 | $V_{CNTRL}$=0 或 $V_{CC}$, $I_{OUT}$=0 | 4.3 | | | 1.0 | μA |
| $I_{CCT}$ | 每个控制电压和Vcc的$I_{CC}$ 电流增量 | $V_{CNTRL}$=1.8 V | 2.775 | | | 1.5 | μA |

## 直流电气特性，低速模式

若无其他说明，所有典型值都在 $T_A$=25° C 下测得。

| 符号 | 参数 | 工作条件 | $V_{CC}$ (V) | $T_A$=-40 至 +85°C | | | 单位 |
|---|---|---|---|---|---|---|---|
| | | | | 最小值 | 典型值 | 最大值 | |
| $R_{ON}$ | LS 开关导通电阻(3) | $V_{SW}$=1.2 V, $I_{ON}$=-10 mA, 图 4 | 2.65 | | 10 | 14 | Ω |
| $\Delta R_{ON}$ | LS Delta $R_{ON}$(4) | $V_{SW}$=1.2 V, $I_{ON}$=-10 mA（内部成对） | 2.65 | | 0.75 | | Ω |

**注意：**

3. 在指定通过电流下，由 A/B 和 CLK/Dn 引脚之间的电压降测得。
4. 由产品特性保证。

## 直流电气特性，高速模式

若无其他说明，所有典型值都在 $T_A$=25° C 下测得。

| 符号 | 参数 | 工作条件 | $V_{CC}$ (V) | $T_A$=-40 至 +85°C | | | 单位 |
|---|---|---|---|---|---|---|---|
| | | | | 最小值 | 典型值 | 最大值 | |
| $R_{ON}$ | HS 开关导通电阻(5) | $V_{SW}$=0.4 V, $I_{ON}$=-10 mA, 图 4 | 2.65 | | 7.0 | 9.5 | Ω |
| $\Delta R_{ON}$ | HS Delta $R_{ON}$(6) | $V_{SW}$=0.4 V, $I_{ON}$=-10 mA（内部成对） | 2.65 | | 0.75 | | Ω |

**注意：**

5. 在指定通过电流下，由 A、B 和 Dn 引脚之间的电压降测得。
6. 由产品特性保证。

## 交流电气特性

所有值的测量条件为 $R_L$=50 Ω 和 $R_S$=50 Ω，典型值为 $V_{CC}$=2.775 V，$T_A$=25° C，除非另有说明。

| 符号 | 参数 | 工作条件 | $V_{CC}$ (V) | $T_A$=-40°C 至 +85°C | | | 单位 |
|---|---|---|---|---|---|---|---|
| | | | | 最小值 | 典型值 | 最大值 | |
| $O_{IRR}$ | 关断隔离(7) | f=100 MHz, $R_T$=50 Ω<br>图 14 | 2.775 | | -50 | | dB |
| Xtalk | 非相邻通道串扰(7) | f=100 MHz, $R_T$=50 Ω<br>图 15 | 2.775 | | -40 | | dB |
| BW | -3db 带宽(7) | $C_L$=0 pF, $R_T$=50 Ω<br>图 13 | 2.775 | | 1.0 | | GHz |
| $t_{ON}$ | 开机时间<br>SEL，/OE 至输出 | $C_L$=5 pF, $V_{SW}$=1.2 V<br>图 6, 图 7 | 2.650 至 2.775 | | 20 | 37 | ns |
| $t_{OFF}$ | 关断时间<br>SEL，/OE 至输出 | $C_L$=5 pF, $V_{SW}$=1.2 V<br>图 6, 图 7 | 2.650 至 2.775 | | 15 | 27 | ns |
| $t_{PD}$ | 传输延迟(7) | $C_L$=5 pF<br>图 6, 图 8 | 2.775 | | 0.25 | | ns |
| $t_{BBM}$ | "先开后合"时间 | $C_L$=5 pF, $V_{SW1}$=$V_{SW2}$=1.2 V<br>图 12 | 2.650 至 2.775 | 7 | 9 | 12 | ns |

**注意：**

7. 由产品特性保证。

## 交流电气特性，高速模式

若无其他说明，所有典型值都在 $V_{CC}$=2.775V，$T_A$=25° C 下测得。

| 符号 | 参数 | 工作条件 | $T_A$=-40°C 至 +85°C | | | 单位 |
|---|---|---|---|---|---|---|
| | | | 最小值 | 典型值 | 最大值 | |
| $t_{SK(Part\_Part)}$ | 多器件通道间相位差(8,9) | TDR 方法<br>($V_{SW}$=0.2$V_{PP}$, $C_L$ = $C_{ON}$) | | 40 | 80 | ps |
| $t_{SK(Chl\_Chl)}$ | 单器件通道间相位差(8) | TDR 方法<br>($V_{SW}$=0.2$V_{PP}$, $C_L$ = $C_{ON}$) | | 15 | 30 | ps |
| $t_{SK(Pulse)}$ | 同一差分通道内的反向转换相位差(8) | TDR方法<br>($V_{SW}$=0.2$V_{PP}$, $C_L$ = $C_{ON}$) | | 10 | 20 | ps |

**注意：**

8. 由产品特性保证。
9. 假设所有器件应用相同的 $V_{CC}$ 和温度。

## 电容值

| 符号 | 参数 | 工作条件 | $T_A$=-40°C 至 +85°C | | | 单位 |
|---|---|---|---|---|---|---|
| | | | 最小值 | 典型值 | 最大值 | |
| $C_{IN}$ | 控制引脚输入电容(10) | $V_{CC}$=0 V | | 1.5 | | pF |
| $C_{ON}$ | Dn/CLK- 导通电容(10) | $V_{CC}$=2.775 V, /OE=0V, f=1 MHz<br>图 11 | | 8.0 | | |
| $C_{OFF}$ | Dn/CLK- 关断电容(9) | $V_{CC}$=2.775 V, /OE=2.775 V, f=1 MHz<br>图 10 | | 2.5 | | |

**注意：**

10. 由产品特性保证。

## 测试框图

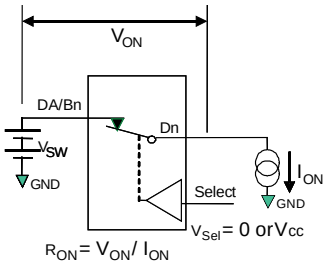
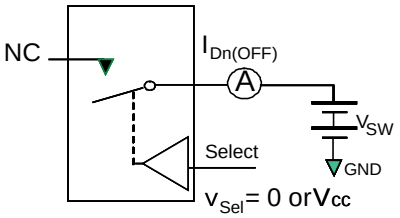
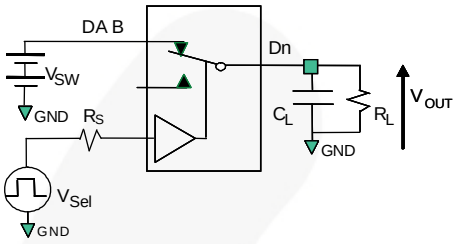



图 4. 导通电阻




**Each switch port is tested separately

图 5. 关断漏电流




$R_L$, $R_S$, an $C_L$ ar fu ctions of th ap lication environment (se AC Tables for spe ific v lues)
$C_L$ inclu es test fixture an stra capacitance

图 6. 交流测试电路负载

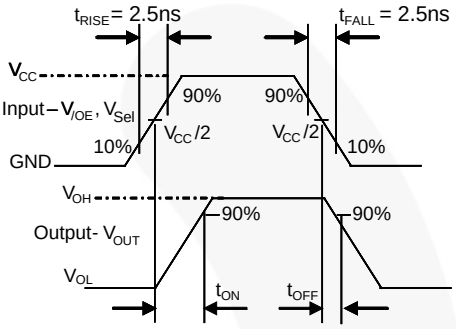



图 7. 开通/关断波形

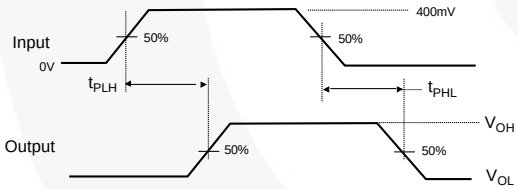



图 8. 传输延迟 ($t_R t_F$ – 500 ps)

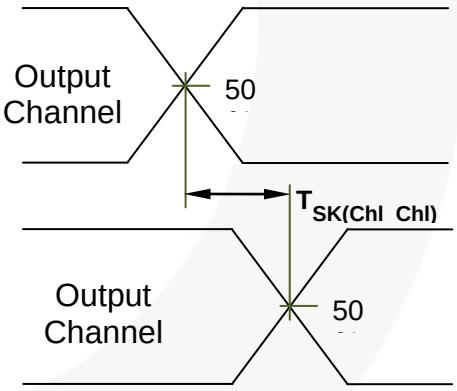



图 9. 通道间相位差

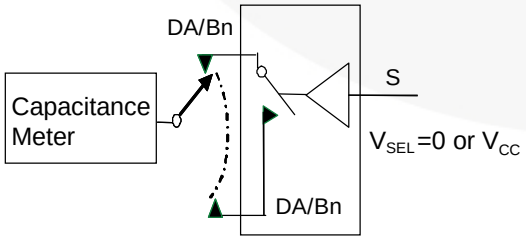



图 10. 通道关断电容

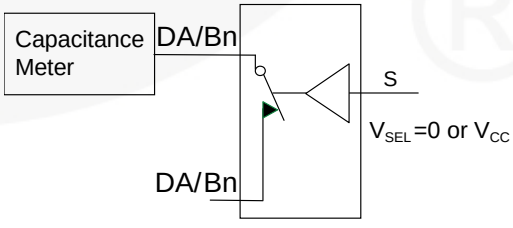
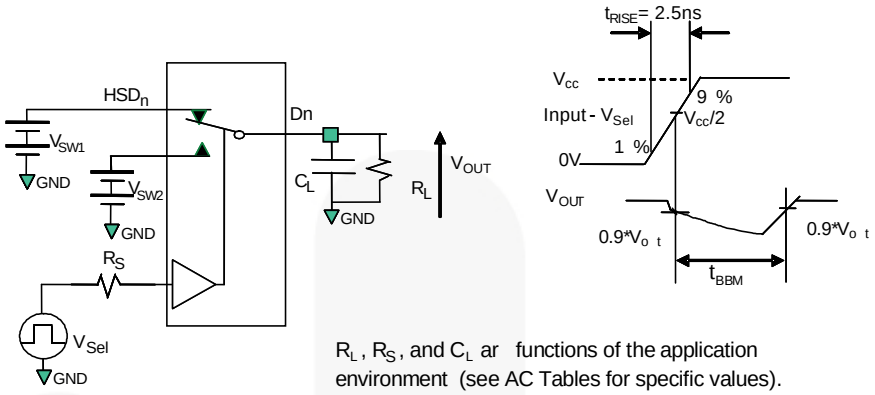


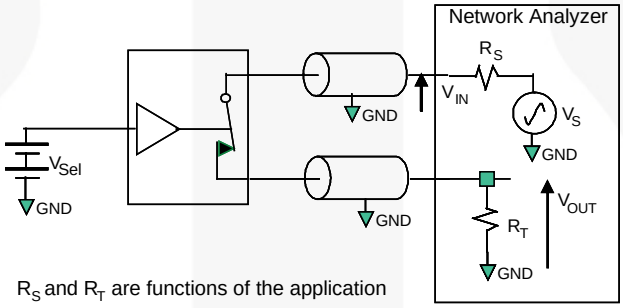

图 11. 通道导通电容

## 测试框图（续）



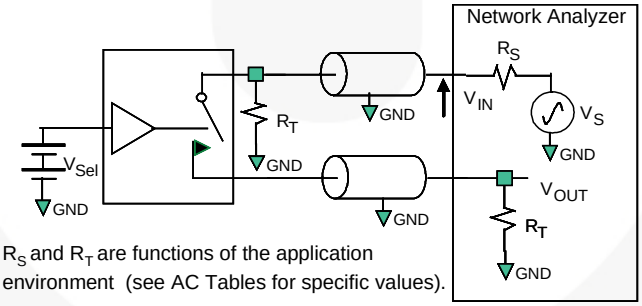

$R_L$, $R_S$, and $C_L$ ar functions of the application environment (see AC Tables for specific values). $C_L$ includes test fixture and stray capacitance.

**图 12. 先开后合间隔时序**




$R_S$ and $R_T$ are functions of the application environment (see AC Tables for specific values).

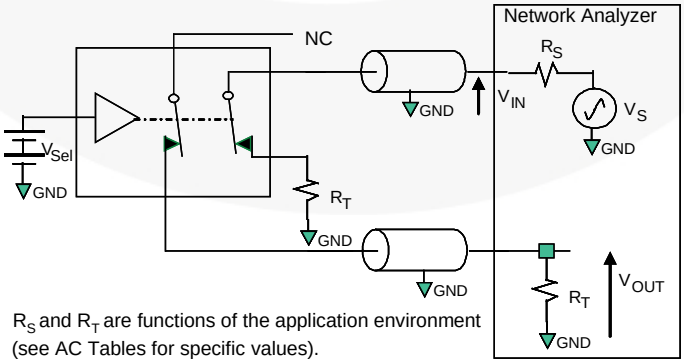
**图 13. 带宽**




$R_S$ and $R_T$ are functions of the application environment (see AC Tables for specific values).

Off isolation = 20 Log ($V_{OUT}$ / $V_{IN}$)

**图 14. 通道的关断隔离**

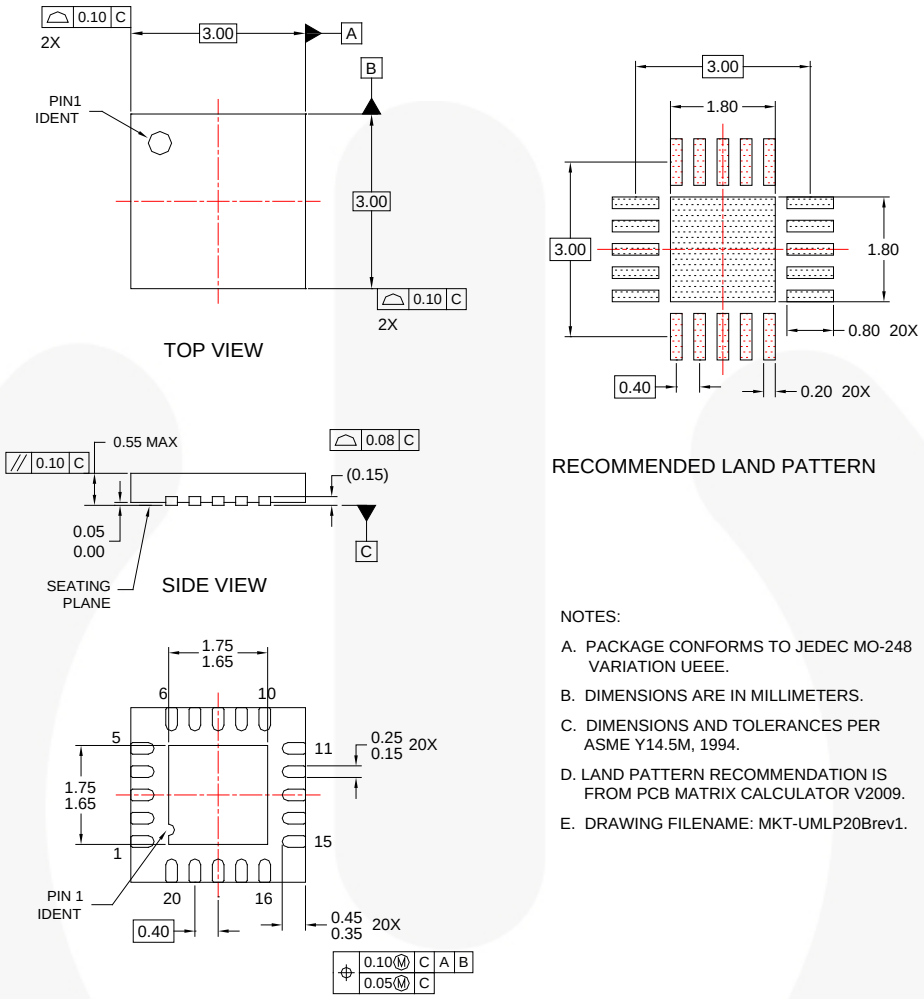



$R_S$ and $R_T$ are functions of the application environment (see AC Tables for specific values).

Crosstalk = 20 Log ($V_{OUT}$ / $V_{IN}$)

**图 15. 非相邻通道间串扰**

## 物理尺寸测试




NOTES:

A. PACKAGE CONFORMS TO JEDEC MO-248 VARIATION UEEE.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. LAND PATTERN RECOMMENDATION IS FROM PCB MATRIX CALCULATOR V2009.

E. DRAWING FILENAME: MKT-UMLP20Brev1.

**图 16. 20-引脚，方形，超薄膜塑无铅封装 (UMLP)，3.0 x 3.0 mm**

*封装图纸是作为一项服务而提供给考虑选用飞兆半导体产品的客户。具体参数可进行改动，且无需做出相应通知。请注意图纸上的版本和/或日期，并联系飞兆半导体代表核实或获得最新版本。封装规格并不超出飞兆公司全球范围内的条款与条件，尤其指保修，保修涉及飞兆半导体的全部产品。*

*随时访问飞兆半导体在线封装网页，可以获得最新的封装图：*
*http://www.fairchildsemi.com/dwg/UM/UMLP20B.pdf*。

*随时访问飞兆半导体在线封装网页，可以获得最新的卷带规格：*

HYPERLINK "http://www.fairchildsemi.com/packaging/3.0x3.0_UMLP_Pack_TNR_Spec.pdf%20"
*http://www.fairchildsemi.com/packaging/3.0x3.0_UMLP_Pack_TNR_Spec.pdf* 。

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