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# FSA646 2:1 MIPI D-PHY (2.5Gbps) 4-Data Lane Switch

## Features

- Switch Type: SPDT(10x)
- Signal Types:
  - MIPI, D-PHY
- V<sub>CC</sub>: 1.5 to 5.0 V
- Input Signals: 0 to 1.3 V
- R<sub>ON</sub>:
  - 6 Ω Typical HS MIPI
  - 6 Ω Typical LP MIPI
- ΔR<sub>ON</sub>: 0.1 Ω Typical LP & HS MIPI
- R<sub>ON\_FLAT</sub>: 0.9 Ω Typical LP & HS MIPI
- I<sub>CCZ</sub>: 1 μA Maximum
- I<sub>CC</sub>: 32 μA Typical
- O<sub>IRR</sub>: -24 dB Typical
- Bandwidth: 2500 MHz Minimum
- Xtalk: -30 dB Typical
- C<sub>ON</sub>: 1.5 pF Typical
- Skew of Opposite Transitions of the Same Output: 6 ps Typical

## Description

The FSA646 is a four-data-lane MIPI, D-PHY switch. This single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed or low-power MIPI sources. The FSA646 is designed for the MIPI specification and allows connection to a CSI or DSI module.

## Applications

- Cellular Phones, Smart phones
- Tablets
- Laptops
- Displays

## Ordering Information

Part Number	Operating Temperature Range	Package	Top Mark
FSA646UCX	-40 to +85°C	36-Ball WLCSP, Non-JEDEC 2.43 mm x 2.43 mm, 0.4 mm Pitch	GS

FSA646 — 2:1 MIPI D-PHY (2.5Gbps) 4-Data Lane Switch

### Typical Application

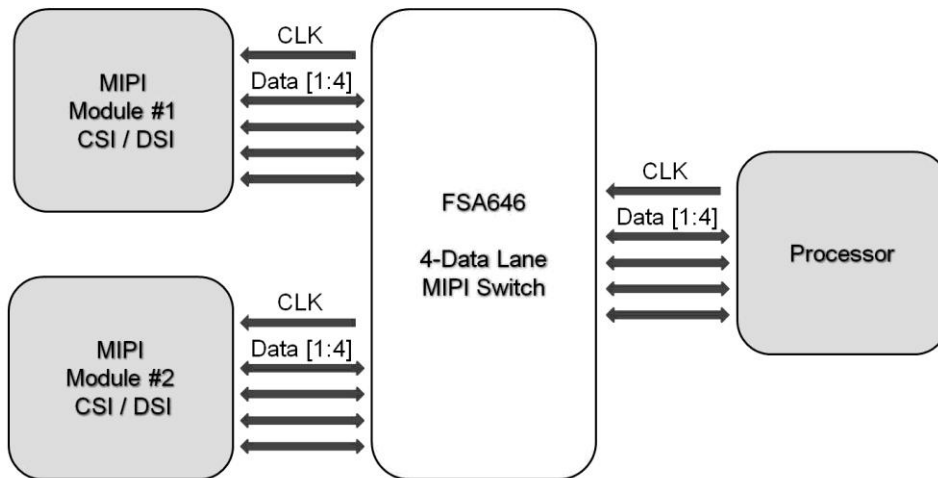


Figure 1. Typical Application

### Pin Descriptions

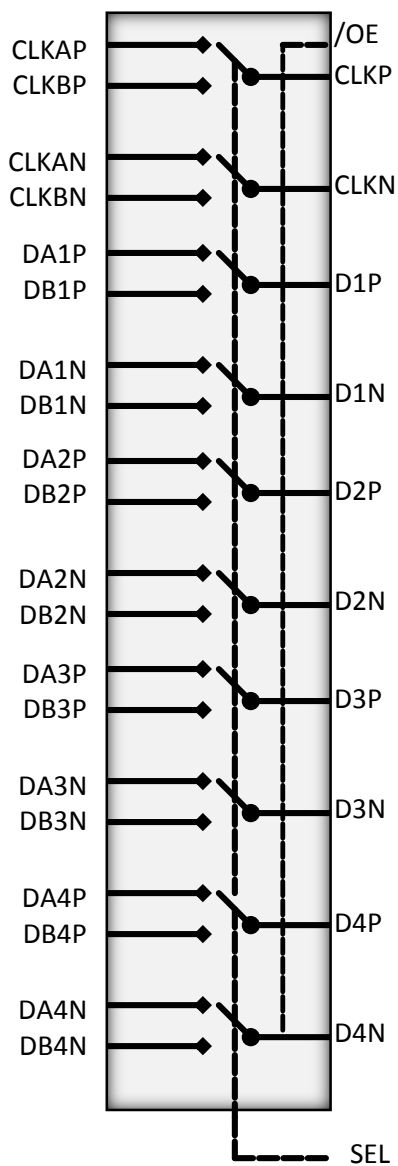


Figure 2. Analog Symbol

Pin Name	Description		
CLKBP/N	B Side Clock Path		
DB1P/N	B Side Data Path 1		
DB2P/N	B Side Data Path 2		
DB3P/N	B Side Data Path 3		
DB4P/N	B Side Data Path 4		
CLKAP/N	A Side Clock Path		
DA1P/N	A Side Data Path 1		
DA2P/N	A Side Data Path 2		
DA3P/N	A Side Data Path 3		
DA4P/N	A Side Data Path 4		
CLKP/N	Common Clock Path		
D1P/N	Common Data Path 1		
D2P/N	Common Data Path 2		
D3P/N	Common Data Path 3		
D4P/N	Common Data Path 4		
/OE	Output Enable		
SEL	Control Pin	SEL=0	CLKP/N=CLKAP/N, DnP/N=DAnP/N
		SEL=1	CLKP/N=CLKBP/N, DnP/N=DBnP/N
VCC	Power		
GND	Ground		
NC	No Connect		

## Pin Definitions

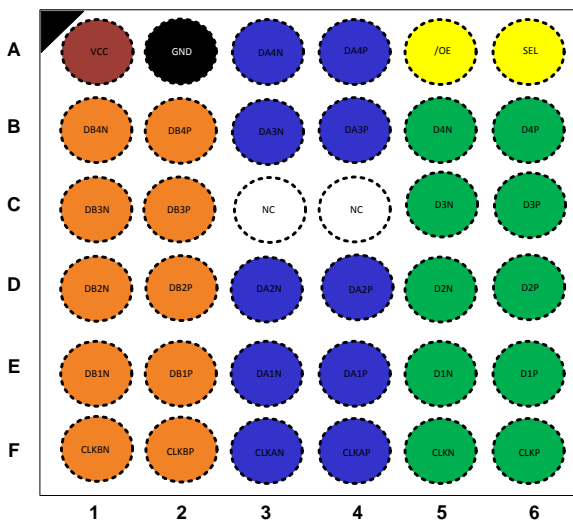


Figure 3. Top Through View

Ball	Pin Name
A1	V <sub>CC</sub>
A2	GND
A3	DA4N
A4	DA4P
A5	/OE
A6	SEL
B1	DB4N
B2	DB4P
B3	DA3N
B4	DA3P
B5	D4N
B6	D4P
C1	DB3N
C2	DB3P
C3	NC
C4	NC
C5	D3N
C6	D3P
D1	DB2N
D2	DB2P
D3	DA2N
D4	DA2P
D5	D2N
D6	D2P
E1	DB1N
E2	DB1P
E3	DA1N
E4	DA1P
E5	D1N
E6	D1P
F1	CLKBN
F2	CLKBP
F3	CLKAN
F4	CLKAP
F5	CLKN
F6	CLKP

Table 1. Ball-to-Pin Mappings

## Truth Table

SEL	/OE	Function
LOW	LOW	CLK <sub>P</sub> =CLKA <sub>P</sub> , CLK <sub>N</sub> =CLKA <sub>N</sub> , D <sub>n</sub> (P/N)=DA <sub>n</sub> (P/N)
HIGH	LOW	CLK <sub>P</sub> =CLKB <sub>P</sub> , CLK <sub>N</sub> =CLKB <sub>N</sub> , D <sub>n</sub> (P/N)=DB <sub>n</sub> (P/N)
X	HIGH	Clock and Data Ports High Impedance

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply Voltage	-0.5	6.0	V
$V_{CNTRL}$	DC Input Voltage (/OE, SEL) <sup>(1)</sup>	-0.5	$V_{CC}$	V
$V_{SW}$	DC Switch I/O Voltage <sup>(1,2)</sup>	-0.3	1.8	V
$I_{IK}$	DC Input Diode Current	-50		mA
$I_{OUT}$	DC Output Current		25	mA
$T_{STG}$	Storage Temperature	-65	+150	°C
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins	2.0	kV
	Charged Device Model, JEDEC: JESD22-C101		1.0	
	IEC 61000-4-2 System	Contact	8.0	
		Air Gap	15.0	

### Notes:

- The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
- $V_{SW}$  refers to analog data switch paths.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit	
$V_{CC}$	Supply Voltage	1.5	5.0	V	
$V_{CNTRL}$	Control Input Voltage (SEL, /OE) <sup>(3)</sup>	0	$V_{CC}$	V	
$V_{SW}$	Switch I/O Voltage (CLKn, Dn, CLKAn, CLKBn, DAn, DBn)	- HS Mode	0	0.3	V
		- LP Mode	0	1.3	V
$T_A$	Operating Temperature	-40	+85	°C	

### Note:

- The control inputs must be held HIGH or LOW; they must not float.

## DC and Transient Characteristics

All typical values are at  $T_A=25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$			Unit
				Min.	Typ.	Max.	
$V_{IK}$	Clamp Diode Voltage (/OE, SEL)	$I_{IN} = -18\text{ mA}$	1.5	-1.2		-0.6	V
$V_{IH}$	Input Voltage High	SEL, /OE	1.5 to 5	1.3			V
$V_{IL}$	Input Voltage Low	SEL, /OE	1.5 to 5			0.5	V
$I_{IN}$	Control Input Leakage (SEL, /OE)	$V_{CNTRL} = 0$ to $V_{CC}$	5	-0.5		0.5	$\mu\text{A}$
$I_{NO(OFF)}$ $I_{NC(OFF)}$	Off Leakage Current of Port CLKAn, DAn, CLKBn and DBn	$V_{SW} = 0.0 \leq \text{DATA} \leq 1.3\text{ V}$	5	-0.5		0.5	$\mu\text{A}$
$I_{A(ON)}$	On Leakage Current of Common Ports (CLKn, Dn)	$V_{SW} = 0.0 \leq \text{DATA} \leq 1.3\text{ V}$	5	-0.5		0.5	$\mu\text{A}$
$I_{OFF}$	Power-Off Leakage Current (All I/O Ports)	$V_{SW} = -0.0$ or $1.3\text{ V}$	0	-0.5		0.5	$\mu\text{A}$
$I_{OZ}$	Off-State Leakage	$V_{SW} = 0.0 \leq \text{DATA} \leq 1.3\text{ V}$ , /OE = High	5	-0.5		0.5	$\mu\text{A}$
$R_{ON\_MIPL\_HS}$	Switch On Resistance for HS MIPI Applications <sup>(4)</sup>	$I_{ON} = -8\text{ mA}$ , /OE = 0 V, SEL = $V_{CC}$ or 0 V, CLKA,CLKB, DB <sub>N</sub> or DA <sub>N</sub> = 0.2 V	1.5		6		$\Omega$
			2.5				
			3.3				
			5				
$R_{ON\_MIPL\_LP}$	Switch On Resistance for LP MIPI Applications <sup>(4)</sup>	$I_{ON} = -8\text{ mA}$ , /OE = 0 V, SEL = $V_{CC}$ or 0 V, CLKA,CLKB, DB <sub>N</sub> or DA <sub>N</sub> = 1.2 V	1.5		6		$\Omega$
			2.5				
			3.3				
			5				
$\Delta R_{ON\_MIPL\_HS}$	On Resistance Matching Between HS MIPI Channels <sup>(4)</sup>	$I_{ON} = -8\text{ mA}$ , /OE = 0 V, SEL = $V_{CC}$ or 0 V, CLKA,CLKB, DB <sub>N</sub> or DA <sub>N</sub> = 0.2 V	1.5		0.1		$\Omega$
			2.5				
			3.3				
			5				
$\Delta R_{ON\_MIPL\_LP}$	On Resistance Matching Between LP MIPI Channels <sup>(4)</sup>	$I_{ON} = -8\text{ mA}$ , /OE = 0 V, SEL = $V_{CC}$ or 0 V, CLKA,CLKB, DB <sub>N</sub> or DA <sub>N</sub> = 1.2 V	1.5		0.1		$\Omega$
			2.5				
			3.3				
			5				
$R_{ON\_FLAT\_MIPL\_HS}$	On Resistance Flatness for HS MIPI Signals <sup>(4)</sup>	$I_{ON} = -8\text{ mA}$ , /OE = 0 V, SEL = $V_{CC}$ or 0 V, CLKA,CLKB, DB <sub>N</sub> or DA <sub>N</sub> = 0 to 0.3 V	1.5		0.9		$\Omega$
			2.5				
			3.3				
			5				

Continued on the following page...

### DC and Transient Characteristics (Continued)

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> =- 40°C to +85°C			Unit
				Min.	Typ.	Max.	
R <sub>ON_FLAT_MIPI_LP</sub>	On Resistance Flatness for LP MIPI Signals <sup>(4)</sup>	I <sub>ON</sub> = -8 mA, /OE = 0 V, SEL = V <sub>CC</sub> or 0 V, CLKA, CLKB, DB <sub>N</sub> or DA <sub>N</sub> = 0 to 1.3 V	1.5	0.9			Ω
			2.5				
			3.3				
			5				
I <sub>CC</sub>	Quiescent Supply Current (Includes Charge Pump)	V <sub>SEL</sub> = 0 or V <sub>CC</sub> , I <sub>OUT</sub> = 0, /OE = 0 V	5			30	μA
I <sub>CCZ</sub>	Quiescent Supply Current (High Impedance)	V <sub>SEL</sub> = 0 or V <sub>CC</sub> , I <sub>OUT</sub> = 0, OE = V <sub>CC</sub>	5			1	μA
I <sub>CCCT</sub>	Increase in I <sub>CC</sub> Current Per Control Voltage and V <sub>CC</sub>	V <sub>SEL</sub> = 0 or V <sub>CC</sub> , /OE = 1.5 V	5		1		μA

**Note:**

4. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (A or B ports).

### AC Electrical Characteristics

All typical value are for V<sub>CC</sub> = 3.3 V and T<sub>A</sub> = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> =- 40°C to +85°C			Units
				Min.	Typ.	Max.	
t <sub>INIT</sub>	Initialization Time V <sub>CC</sub> to Output <sup>(5)</sup>	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 0 pF, V <sub>SW</sub> = 0.6 V	1.5 to 5		60		μs
t <sub>EN</sub>	Enable Time /OE to Output	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 0 pF, V <sub>SW</sub> = 0.6 V	1.5 to 5		60	150	μs
t <sub>DIS</sub>	Disable Time /OE to Output	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 0 pF, V <sub>SW</sub> = 0.6 V	1.5 to 5		35	250	ns
t <sub>ON</sub>	Turn-On Time SEL to Output	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 0 pF, V <sub>SW</sub> = 0.6 V	1.5 to 5		350	1100	ns
t <sub>OFF</sub>	Turn-Off Time SEL to Output	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 0 pF, V <sub>SW</sub> = 0.6 V	1.5 to 5		125	800	ns
t <sub>BBM</sub>	Break-Before-Make Time	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 0 pF, V <sub>SW</sub> = 0.6 V	1.5 to 5	50		450	ns
t <sub>PD</sub>	Propagation Delay <sup>(5)</sup>	C <sub>L</sub> = 0 pF, R <sub>L</sub> = 50 Ω	1.5 to 5		0.25		ns
O <sub>IRR</sub>	Off Isolation for MIPI <sup>(5)</sup>	R <sub>L</sub> = 50 Ω, f = 1250 MHz, /OE = HIGH, V <sub>SW</sub> = 0.2 V <sub>PP</sub>	1.5 to 5		-24		dB
X <sub>TALK</sub>	Crosstalk for MIPI <sup>(5)</sup>	R <sub>L</sub> = 50 Ω, f = 1250 MHz, SEL = High, V <sub>SW</sub> = 0.2 V <sub>PP</sub>	1.5 to 5		-30	-25	dB
		R <sub>L</sub> = 50 Ω, f = 1250 MHz, SEL = Low, V <sub>SW</sub> = 0.2 V <sub>PP</sub>			-30	-25	
BW (Insertion Loss)	-3db Bandwidth <sup>(5)</sup>	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 0 pF, V <sub>SW</sub> = 0.2 V <sub>PP</sub>	1.5 to 5	2500			MHz

**Note:**

5. Guaranteed by characterization.



### High-Speed-Related AC Electrical Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> =- 40°C to +85°C			Unit
				Min.	Typ.	Max.	
t <sub>SK(P)</sub>	HS Mode Skew of Opposite Transitions of the Same Output <sup>(6)</sup>	R <sub>L</sub> =50 Ω, C <sub>L</sub> = 0 pF, V <sub>SW</sub> = 0.3 V	1.5 to 5		6		ps

**Notes:**

6. Guaranteed by characterization.

### Capacitance

Symbol	Parameter	Conditions	T <sub>A</sub> =- 40°C to +85°C			Unit
			Min.	Typ.	Max.	
C <sub>IN</sub>	Control Pin Input Capacitance <sup>(7)</sup>	V <sub>CC</sub> = 0 V, f = 1 MHz		2.1		pF
C <sub>ON</sub>	On Capacitance <sup>(7)</sup>	V <sub>CC</sub> = 3.3 V, /OE = 0 V, f = 1250 MHz (In HS common value)		1.5		
C <sub>OFF</sub>	Off Capacitance <sup>(7)</sup>	V <sub>CC</sub> and /OE = 3.3 V, f = 1250 MHz (Both sides in HS common value)		0.9		

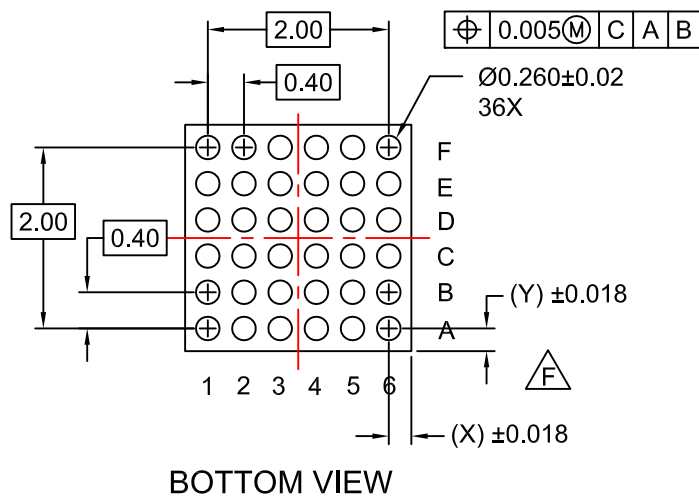
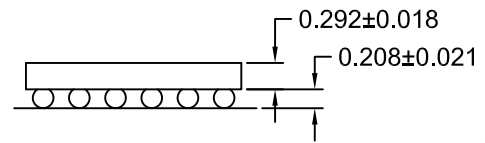
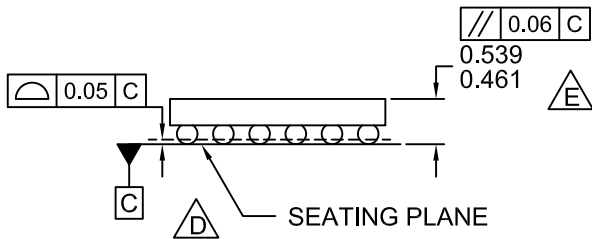
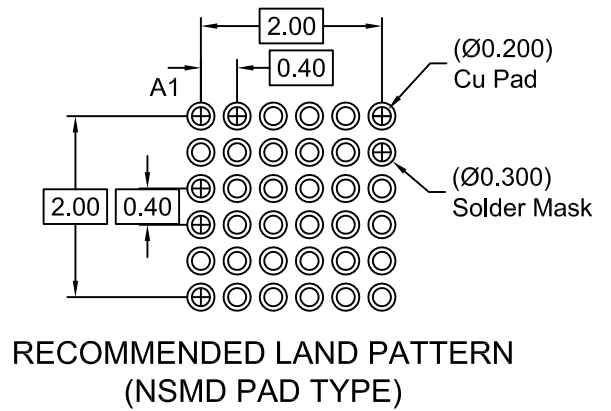
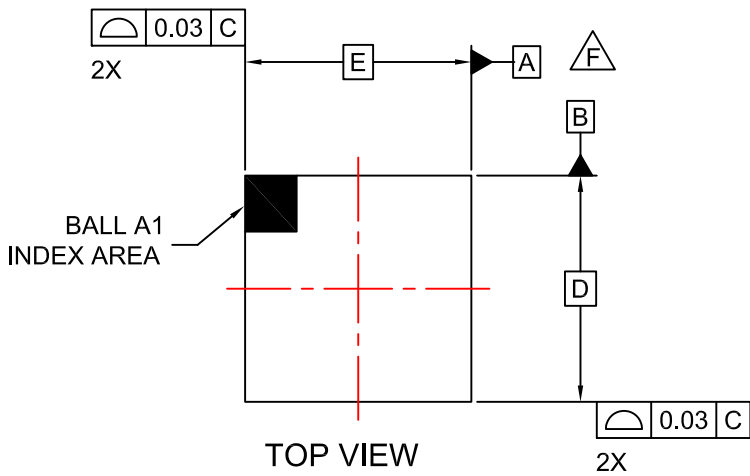
**Note:**

7. Guaranteed by characterization.

The table below pertains to the Packaging information on the following page.

### Product Specific Dimensions

D	E	X	Y
2.43 mm	2.43 mm	0.215 mm	0.215 mm



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- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS  $500 \pm 39$  MICRONS (461-539 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
- G. DRAWING FILNAME: MKT-UC036AArev1.

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