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## FSA2567 - 低功率、双通道 SIM 卡模拟开关

### 特性

- 数据路径的低导通电容: 10 pF 典型值
- 数据路径的低导通电阻: 6  $\Omega$  典型值
- 电源路径的低导通电阻: 0.4  $\Omega$  典型值
- 较宽的  $V_{CC}$  工作电压范围: 1.65 V 至 4.3 V
- 低功耗: 1  $\mu$ A 最大值
  - 15  $\mu$ A 在扩展的电压范围内提供最大的  $I_{CCT}$  ( $V_{IN}=1.8$  V,  $V_{CC}=4.3$  V)
- 宽 -3 db 带宽: > 160 MHz
- 封装:
  - 无铅 16 引脚 MLP & 16 引脚 UMLP
- 额定值 8 kV ESD; > 12 kV 电源/接地 ESD 额定值

### 描述

FSA2567 是一款双向, 低功率, 双通道双刀双掷 (4PDT) 模拟开关, 主要用于双通道 1 位 SIM 卡多路复用。它专为切换 WLAN-SIM 数据和控制信号进行了优化, 将一个通道专门用作电源开关。

FSA2567 符合 SIM 卡要求, 具有 10 pF 的低导通电容 ( $C_{ON}$ ) 以确保高速数据传输。 $V_{SIM}$  开关路径具有低  $R_{ON}$  特性, 以确保双通道 SIM 卡电源路径的最低压降。

FSA2567 包含特殊的电路, 当应用于 SEL 引脚的控制电压低于电源电压 ( $V_{CC}$ ) 时, 可最大限度地降低电流消耗。此特性对超便携式应用 (例如手机) 尤为重要, 可便于与基带处理器的通用 I/O 进行直接的接口连接。其他应用包括便携手机, PDA, 数码相机, 打印机和笔记本电脑中共享的开关和连接器。

### 应用

- 手机, PDA, 数码相机和笔记本
- 液晶显示器, 电视和机顶盒

### 订购信息

器件编号	顶标	工作温度范围	封装
FSA2567MPX	FSA2567	-40 至 +85°C	16 引脚, 模塑无铅封装 (MLP), 四通道, JEDEC MO-220, 3 mm <sup>2</sup>
FSA2567UMX	GX		16 引脚, 四通道, 超薄膜塑无铅封装 (UMLP), 1.8 x 2.6 mm

 关于飞兆对生态状况的定义, 请访问: [http://www.fairchildsemi.com/company/green/rohs\\_green.html](http://www.fairchildsemi.com/company/green/rohs_green.html)。

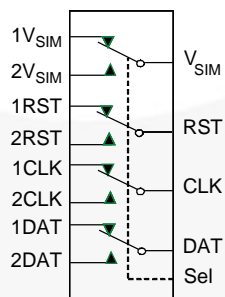


图 1. 模拟符号

## 引脚分配

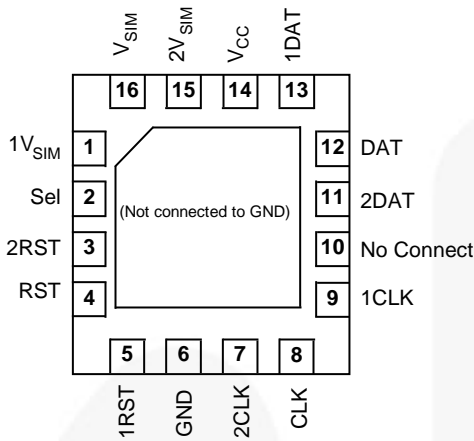


图 2. 焊盘分配 MLP16 (顶视图)

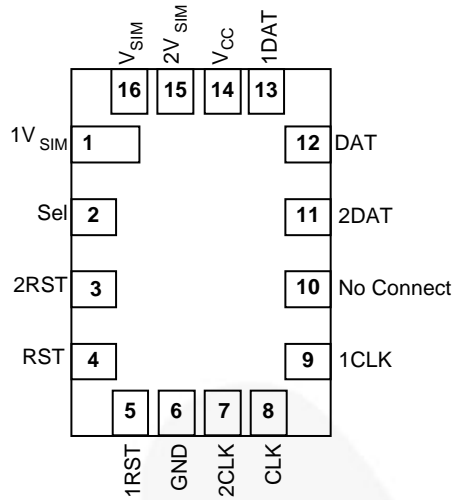


图 3. 焊盘分配 UMLP16 (顶视图)

## 引脚定义

引脚	描述
nDAT, nRST, nCLK	多路复用数据源输入
nV <sub>SIM</sub>	多路复用 SIM 电源输入
V <sub>SIM</sub> , DAT, RST, CLK	通用 SIM 端口
Sel	开关选择

## 真值表

Sel	功能
逻辑低电平	1 DAT = DAT, 1 RST = RST, 1 CLK = CLK, 1 V <sub>SIM</sub> = V <sub>SIM</sub>
逻辑高电平	2 DAT = DAT, 2 RST = RST, 2 CLK = CLK, 2 V <sub>SIM</sub> = V <sub>SIM</sub>

## 绝对最大额定值

应力超过绝对最大额定值，可能会损坏器件。在超出推荐的工作条件的情况下，该器件可能无法正常工作，所以不建议让器件在这些条件下长期工作。此外，长期在高于推荐的工作条件下工作，会影响器件的可靠性。绝对最大额定值仅是应力规格值。

符号	参数	最小值	最大值	单位
$V_{CC}$	电源电压	-0.5	+5.5	V
$V_{CNTRL}$	直流输入电压 (Sel) <sup>(1)</sup>	-0.5	$V_{CC}$	V
$V_{SW}$	直流开关 I/O 电压 <sup>(1)</sup>	-0.5	$V_{CC} + 0.3$	V
$I_{IK}$	直流输入二极管电流	-50		mA
$I_{SIM}$	直流输出电流 - $V_{SIM}$		350	mA
$I_{OUT}$	直流输出电流 - DAT, CLK, RST		35	mA
$T_{STG}$	存储温度	-65	+150	°C
ESD	人体模型, JEDEC: JESD22-A114	全部引脚	3	kV
		I/O 至 GND	12	
	元件充电模型, JEDEC: JESD22-C101		2	

注:

1. 当测量输入与输出二极管电流额定值时，该输入与输出可能超出负额定值。

## 推荐工作条件

推荐的操作条件表明了器件的真实工作条件。指定推荐的工作条件，以确保器件的最佳性能达到数据表中的规格。飞兆半导体建议不要超过推荐工作条件，也不能按照绝对最大额定值进行设计。

符号	参数	最小值	最大值	单位
$V_{CC}$	电源电压	1.65	4.30	V
$V_{CNTRL}$	控制输入电压 (Sel) <sup>(2)</sup>	0	$V_{CC}$	V
$V_{SW}$	开关 I/O 电压	-0.5	$V_{CC}$	V
$I_{SIM}$	直流输出电流 - $V_{SIM}$		150	mA
$I_{OUT}$	直流输出电流 - DAT, CLK, RST		25	mA
$T_A$	工作温度	-40	+85	°C

注:

2. 控制输入必须保持高电平或低电平，不允许浮动。

## 直流电气特性

所有典型值都在 25°C, 3.3 V  $V_{CC}$  下测得, 若无其他说明。

符号	参数	工作条件	$V_{CC}$ (V)	$T_A = -40^\circ\text{C}$ 至 $+85^\circ\text{C}$			单位
				最小值	典型值	最大值	
$V_{IK}$	箝位二极管电压	$I_{IN} = -18\text{ mA}$	2.7			-1.2	V
$V_{IH}$	输入电压高电平		1.65 至 2.3	1.1			V
			2.7 至 3.6	1.3			
			4.3	1.7			
$V_{IL}$	输入电压低电平		1.65 至 2.3			0.4	V
			2.7 至 3.6			0.5	
			4.3			0.7	
$I_{IN}$	控制脚输入漏电流	$V_{SW} = 0$ 至 $V_{CC}$	4.3	-1		1	$\mu\text{A}$
$I_{nc(off)}$ , $I_{no(off)}$	关断漏电流	$nRST, nDAT, nCLK, nV_{SIM}$ $= 0.3\text{ V}$ 或 $3.6\text{ V}$ 图 10	4.3	-60		60	nA
$R_{OND}$	数据路径导通电阻 <sup>(3)</sup>	$V_{SW} = 0, 1.8\text{ V}, I_{ON} = -20\text{ mA}$ 图 9	1.8		7.0	12.0	$\Omega$
			$V_{SW} = 0, 2.3\text{ V}, I_{ON} = -20\text{ mA}$ 图 9	2.7		6.0	
$R_{ONV}$	$V_{SIM}$ 开关导通电阻 <sup>(3)</sup>	$V_{SW} = 0, 1.8\text{ V}, I_{ON} = -100\text{ mA}$ 图 9	1.8		0.5	0.7	$\Omega$
			$V_{SW} = 0, 2.3\text{ V}, I_{ON} = -100\text{ mA}$ 图 9	2.7		0.4	
$\Delta R_{OND}$	数据路径德尔塔导通电阻 <sup>(4)</sup>	$V_{SW} = 0\text{ V}, I_{ON} = -20\text{ mA}$	2.7		0.2		$\Omega$
$I_{CC}$	静态电源电流	$V_{CNTRL} = 0$ 或 $V_{CC}, I_{OUT} = 0$	4.3			1.0	$\mu\text{A}$
$I_{CCT}$	每个控制电压和 $V_{CC}$ 的 $I_{CC}$ 电流增量	$V_{CNTRL} = 2.6\text{ V}, V_{CC} = 4.3\text{ V}$	4.3		5.0	10.0	$\mu\text{A}$
		$V_{CNTRL} = 1.8\text{ V}, V_{CC} = 4.3\text{ V}$	4.3		7.0	15.0	$\mu\text{A}$

### 注意:

- 在通过开关的指定电流下, 由  $nDAT, nRST, nCLK$  和相对通用端口引脚之间的电压降测得。导通电阻决定于相对端口上的较低电压。
- 由产品特性保证。

## 交流电气特性

所有典型值都在  $V_{CC} = 3.3\text{ V}$ ,  $25^\circ\text{C}$  时测得, 若无其他说明。

符号	参数	工作条件	$V_{CC}$ (V)	$T_A = -40^\circ\text{C}$ 至 $+85^\circ\text{C}$			单位
				最小值	典型值	最大值	
$t_{OND}$	导通时间 Sel 至输出 (DAT, CLK, RST)	$R_L = 50\ \Omega$ , $C_L = 35\ \text{pF}$ $V_{SW} = 1.5\ \text{V}$ 图 11, 图 12	1.8 <sup>(5)</sup>		65	95	ns
			2.7 to 3.6		42	60	ns
$t_{OFFD}$	关断时间 Sel 至输出 (DAT, CLK, RST)	$R_L = 50\ \Omega$ , $C_L = 35\ \text{pF}$ $V_{SW} = 1.5\ \text{V}$ 图 11, 图 12	1.8 <sup>(5)</sup>		30	50	ns
			2.7 至 3.6		20	40	ns
$t_{ONV}$	导通时间 Sel 至输出 ( $V_{SIM}$ )	$R_L = 50\ \Omega$ , $C_L = 35\ \text{pF}$ $V_{SW} = 1.5\ \text{V}$ 图 11, 图 12	1.8 <sup>(5)</sup>		55	80	ns
			2.7 至 3.6		35	55	ns
$t_{OFFV}$	关断时间 Sel 至输出 ( $V_{SIM}$ )	$R_L = 50\ \Omega$ , $C_L = 35\ \text{pF}$ $V_{SW} = 1.5\ \text{V}$ 图 11, 图 12	1.8 <sup>(5)</sup>		35	50	
			2.7 至 3.6		22	40	ns
$t_{PD}$	传输延迟 <sup>(5)</sup> (DAT, CLK, RST)	$C_L = 35\ \text{pF}$ , $R_L = 50\ \Omega$ 图 11, 图 13	3.3		0.25		ns
$t_{BBMD}$	先开后合 <sup>(5)</sup> (DAT, CLK, RST)	$R_L = 50\ \Omega$ , $C_L = 35\ \text{pF}$ $V_{SW1} = V_{SW2} = 1.5\ \text{V}$ 图 15	2.7 至 3.6	3	18		ns
$t_{BBMV}$	先开后合 <sup>(5)</sup> ( $V_{SIM}$ )	$R_L = 50\ \Omega$ , $C_L = 35\ \text{pF}$ $V_{SW1} = V_{SW2} = 1.5\ \text{V}$ 图 15	2.7 至 3.6	3	12		ns
Q	电荷注入 (DAT, CLK, RST)	$C_L = 50\ \text{pF}$ , $R_{GEN} = 0\ \Omega$ , $V_{GEN} = 0\ \text{V}$	2.7 至 3.6		10		pC
$O_{IRR}$	关断隔离 (DAT, CLK, RST)	$R_L = 50\ \Omega$ , $f = 10\ \text{MHz}$ 图 17	2.7 至 3.6		-60		dB
Xtalk	非相邻通道串扰 (DAT, CLK, RST)	$R_L = 50\ \Omega$ , $f = 10\ \text{MHz}$ 图 18	2.7 至 3.6		-60		dB
BW	-3 db 带宽 (DAT, CLK, RST)	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$ 图 16	2.7 至 3.6		475		MHz

注:

5. 由产品特性保证。

## 电容值

符号	参数	工作条件	T <sub>A</sub> = -40°C 至 +85°C			单位
			最小值	典型值	最大值	
C <sub>IN</sub>	控制引脚输入电容	V <sub>CC</sub> = 0 V		1.5		pF
C <sub>OND</sub>	RST, CLK, DAT 导通电容 <sup>(6)</sup>	V <sub>CC</sub> = 3.3 V, f = 1 MHz 图 20		10	12	
C <sub>ONV</sub>	V <sub>SIM</sub> 导通电容 <sup>(6)</sup>	V <sub>CC</sub> = 3.3 V, f = 1 MHz 图 20		110	150	
C <sub>OFFD</sub>	RST, CLK, DAT 关断电容	V <sub>CC</sub> = 3.3 V, 图 19		3		
C <sub>OFFV</sub>	V <sub>SIM</sub> 关断电容	V <sub>CC</sub> = 3.3 V, 图 19		40		

注:

6. 由产品特性保证。

典型性能特征

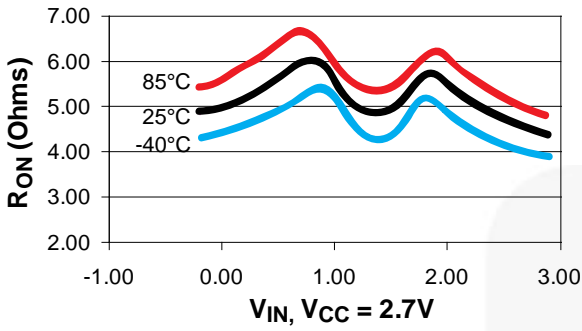


图 4. RON 数据路径

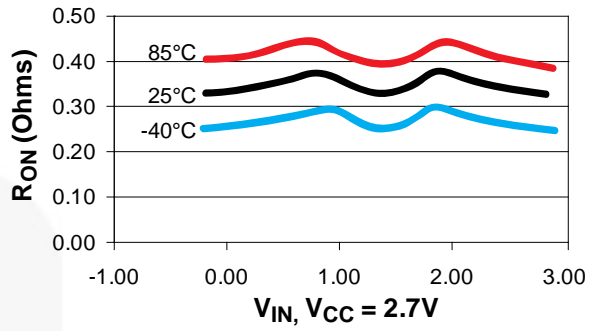


图 5. RON Vsim

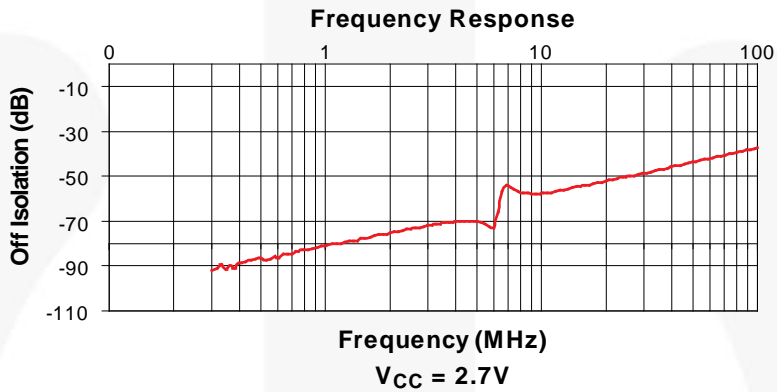


图 6. 关断隔离

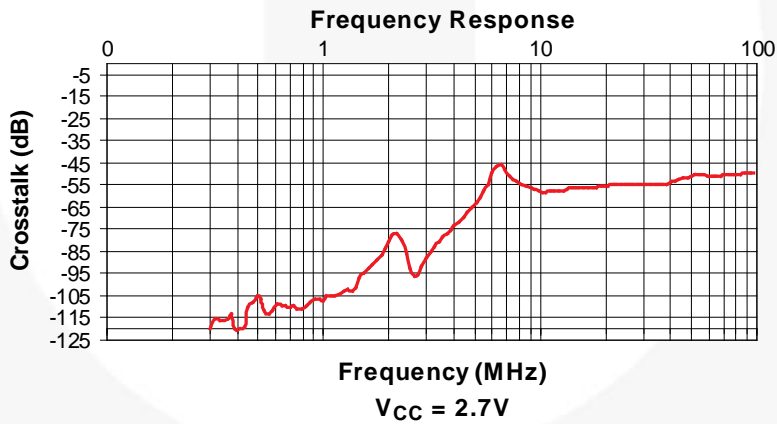


图 7. 串扰

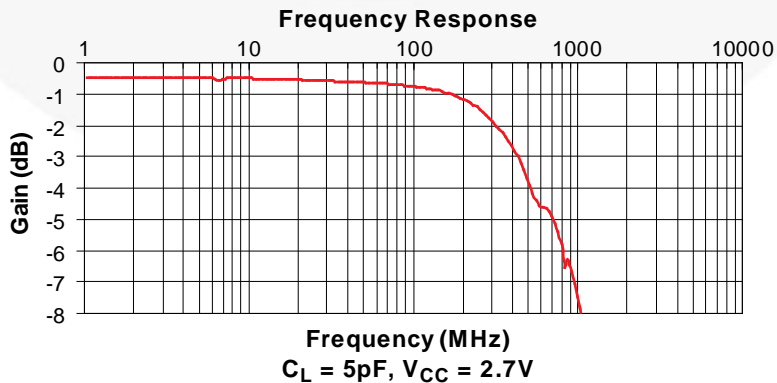


图 8. 带宽



测试框图

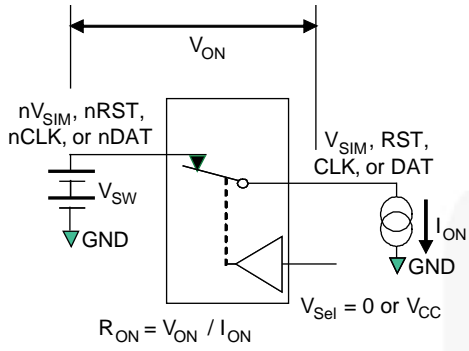


图 9. 导通电阻

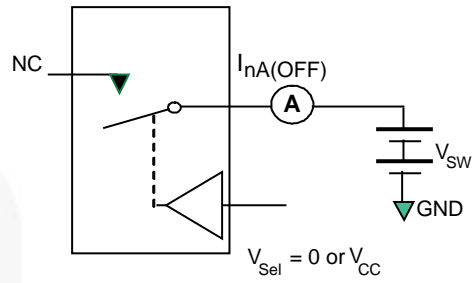
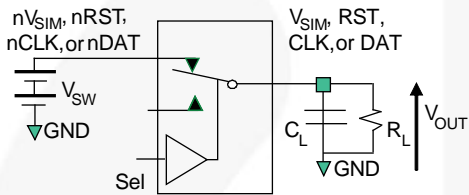


图 10. 关断漏电流



$R_L$  and  $C_L$  are functions of the application environment (see tables for specific values).  $C_L$  includes test fixture and stray capacitance.

图 11. 交流测试电路负载

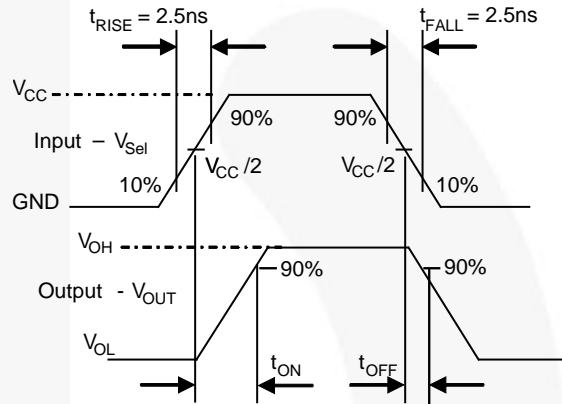


图 12. 开通/关断波形

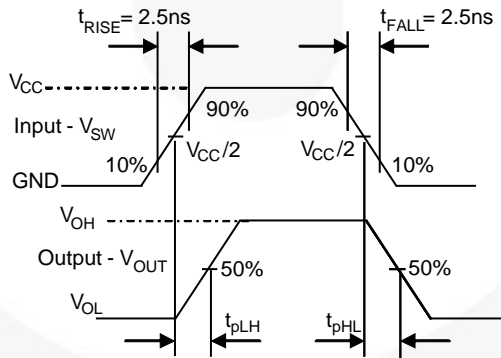


图 13. 传播延迟

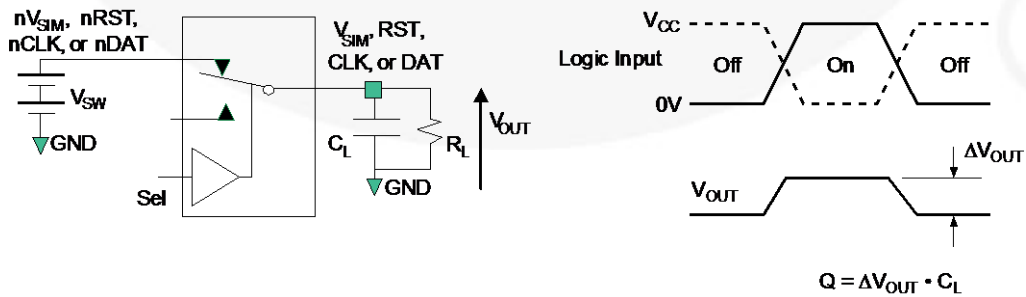
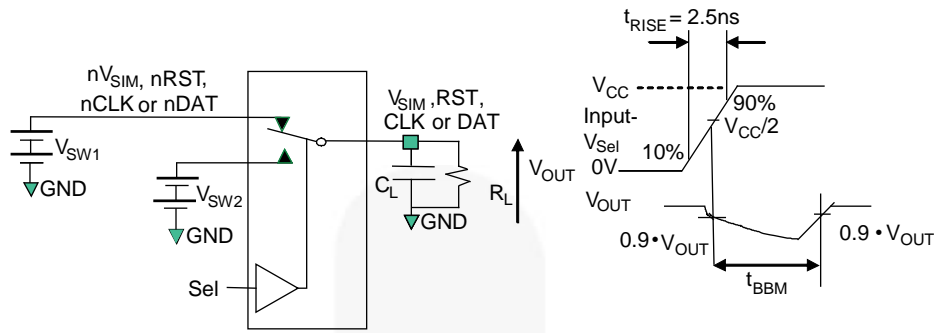


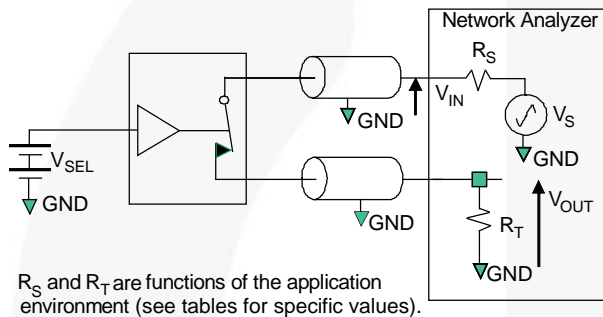
图 14. 电荷注入

测试框图 (续)



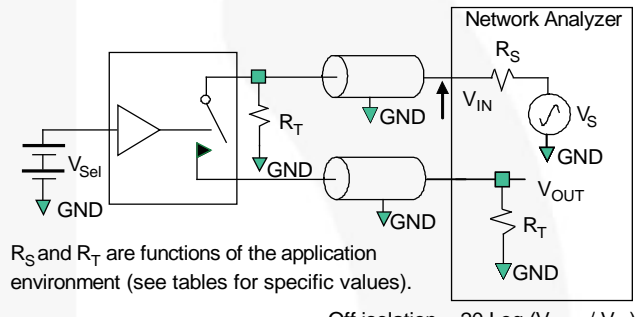
$R_L$  and  $C_L$  are functions of the application environment (see tables for specific values).  $C_L$  includes test fixture and stray capacitance.

图 15. 先开后合间隔时序



$R_S$  and  $R_T$  are functions of the application environment (see tables for specific values).

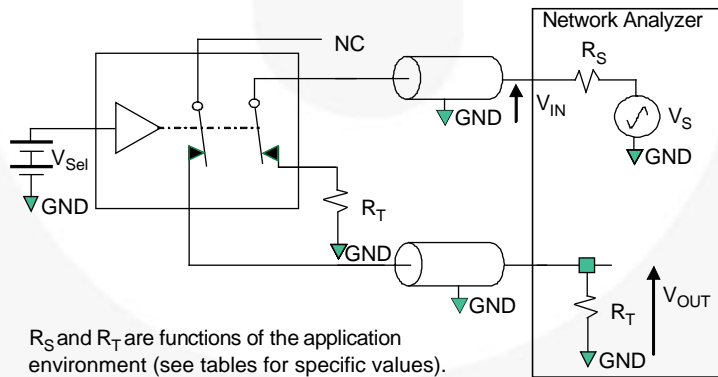
图 16. 带宽



$R_S$  and  $R_T$  are functions of the application environment (see tables for specific values).

$$\text{Off isolation} = 20 \text{ Log} (V_{OUT} / V_{IN})$$

图 17. 通道的关断隔离



$R_S$  and  $R_T$  are functions of the application environment (see tables for specific values).

$$\text{Crosstalk} = 20 \text{ Log} (V_{OUT} / V_{IN})$$

图 18. 非相邻通道间串扰

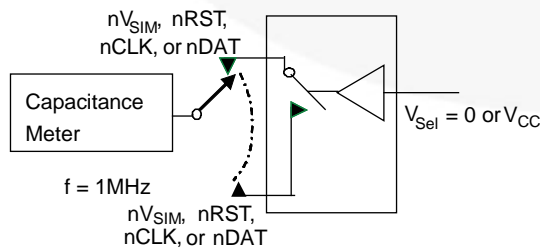


图 19. 通道关断电容

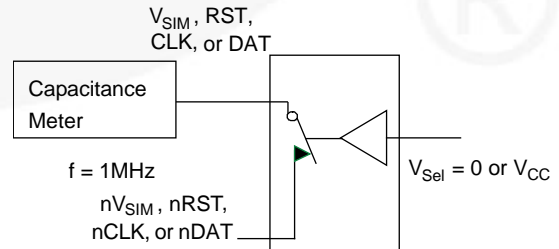
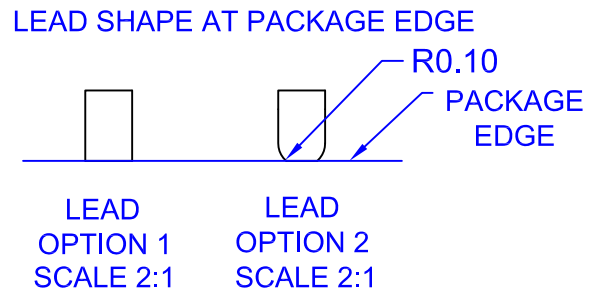
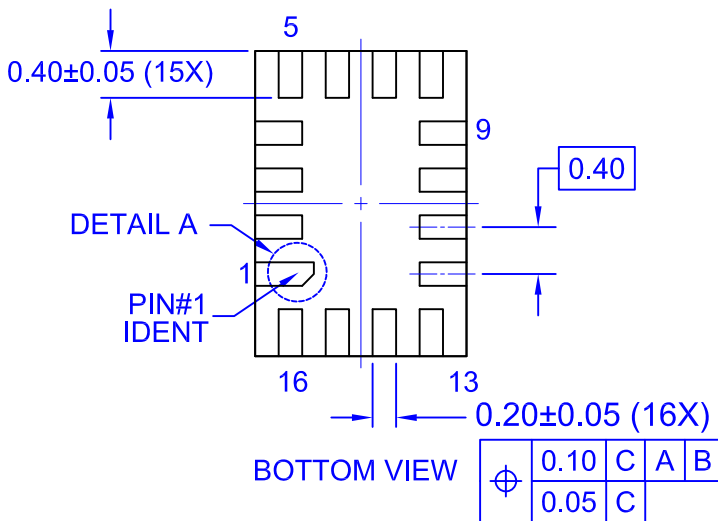
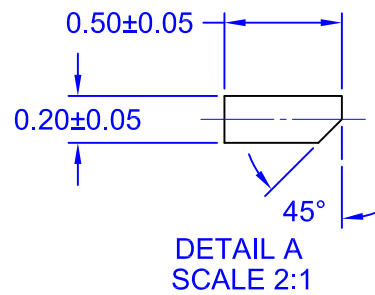
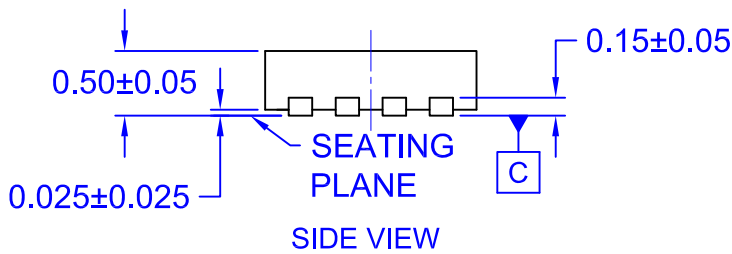
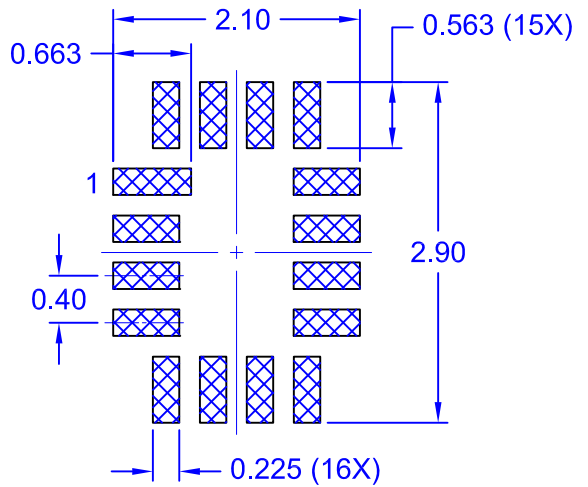
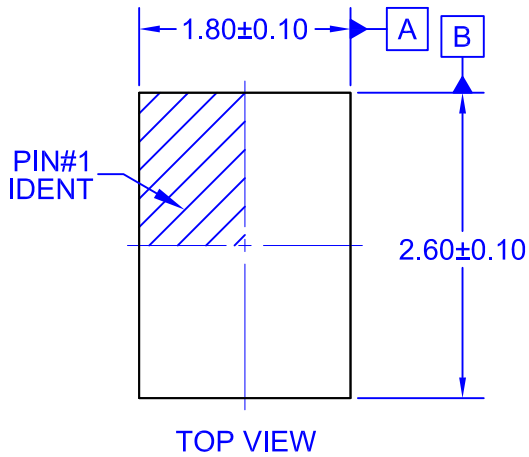


图 20. 通道导通电容

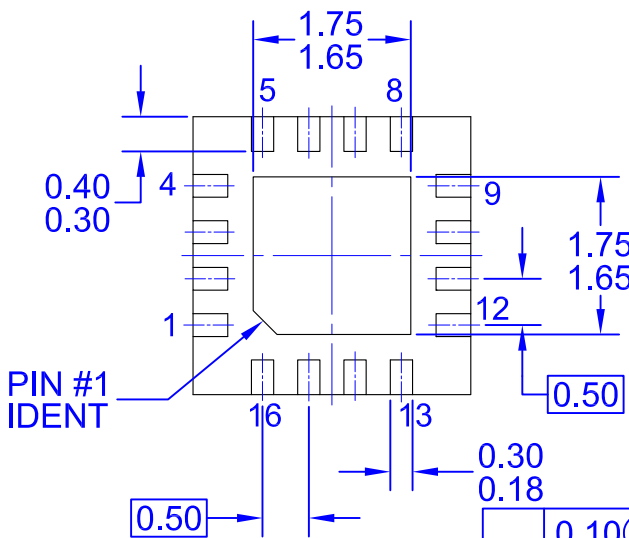
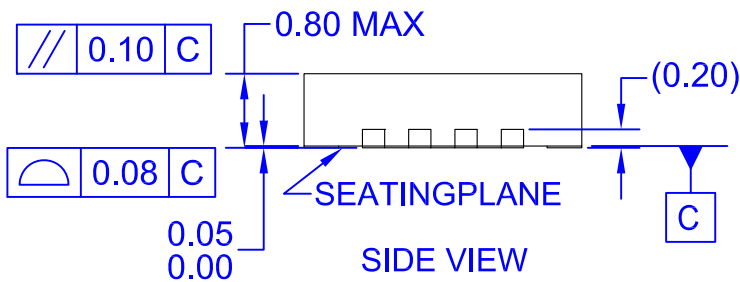
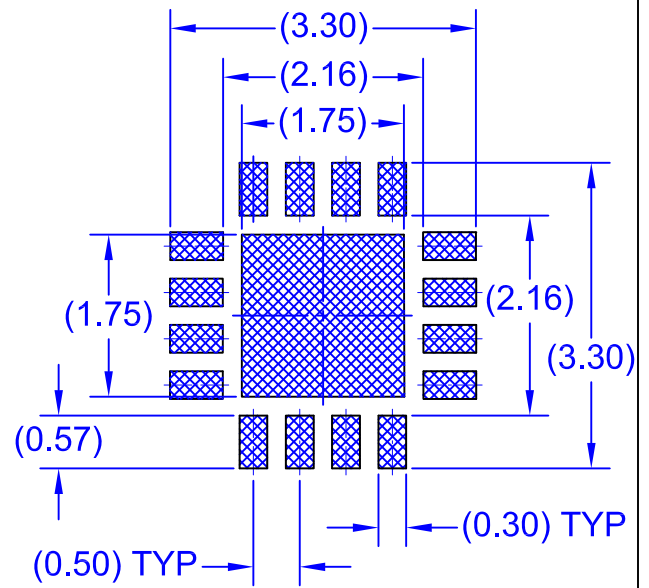
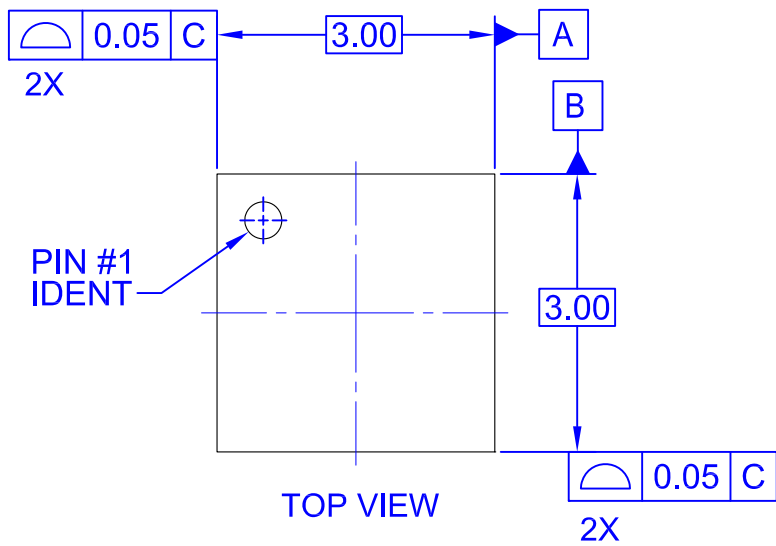


NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- D. DRAWING FILENAME: MKT-UMLP16ArevG.
- E. TERMINAL SHAPE MAY VARY ACCORDING TO PACKAGE SUPPLIER, SEE TERMINAL SHAPE VARIANTS.

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$\phi$	0.10 (M)	C	A	B
	0.05 (M)	C		

- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-220
  - B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
  - D. DRAWING FILE NAME: MKT-MLP16Brev3



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