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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

August 2009

FSA2457 — 四路单刀双掷5Ω 模拟数据开关

特性

- 对于数据路径具有12pF的典型的低导通电容
- 对于数据路径具有5Ω的典型的低导通电阻
- 低功耗：1μA最大值
- 宽广的 -3db带宽: > 160MHz
- 封装保证环境绿化16引脚的UMLP (1.8 x 2.6mm)
- 4kV JEDEC: JESD22-A114 HBM
- 2kV JEDEC: JESD22-C101 CDM

应用

- 手机, PDA, 数字相机, 便携式GPS
- LCD显示屏, TV, 机顶盒

重要提示：

欲知其它详情，请联系
analogswitch@fairchildsemi.com.

描述

FSA2457是双向的低功耗四路单刀双掷模拟开关专门针对双路的1个字节的SIM/SD/MMC 卡和或GPS信号多路复用器而设计。它对于切换WLAN-SIM数据和 52Mbps的控制信号是最佳选择。

FSA2457与1个字节的SIM/SD/MMC卡的要求相兼容并且是连接GPS基带处理器的理想选择。双FSA2457拥有12pF的低导通电容来确保高速数据的传送。

当供给 SEL 管脚的控制电压低于供电电压 时FSA2457因包含有特殊的电路可以最小化电流的功耗，这种特性在象手机类超便携式应用中特别有价值，通过它可以直接与基带处理器通用I/O口连接．其它应用包括在便携式手机，PDAs，数字相机，打印机，和便携式GPS系统的切换和连接。

订货信息

订货编号	表面标记	生态状况	操作温度范围	封装
FSA2457UMX	GD	环境绿化	-40 至 +85°C	16-引脚，方型, 超薄模塑无脚封装(UMLP), 1.8 x 2.6mm

对于Fairchild关于“环境绿化”生态状况的定义，请参阅 http://www.fairchildsemi.com/company/green/rohs_green.html

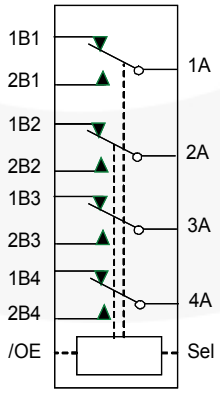


图1.模拟符号

管脚分配图

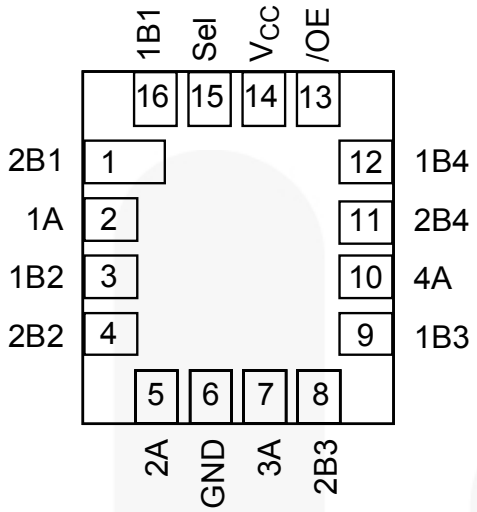


图2. UMLP16 分配图(俯视图)

管脚定义

管脚	描述
1Bn, 2Bn	多路复用数据源输入
nA	共同数据端
Sel	开关选择端
/OE	输出使能(低电平有效)

真值表

Sel	/OE	功能
逻辑低电平	逻辑低电平	1B1 = 1A, 1B2 = 2A, 1B3 = 3A, 1B4 = 4A
逻辑高电平	逻辑低电平	2B1 = 1A, 2B2 = 2A, 2B3 = 3A, 2B4 = 4A
X	逻辑高电平	数据端口断开

最大绝对额定值

超出绝对最大额定值会破坏设备 ,设备会不工作或者说不建议设备在和超过建议的工作条件下被操作。另外,过长的暴露在超过建议工作条件下会影响设备的可靠性，这种绝对最大额定值仅仅是极端额定值。

表达符号	参数		最小值	最大值	单位
V_{CC}	供电电压		-0.5	+4.6	V
V_{CNTRL}	DC输入电压 (Sel, /OE)(1)		-0.5	+4.6	V
V_{SW}	DC 开关 I/O电压(1) 1Bn, 2Bn, nA		-0.5	V_{CC} + 0.5	V
I_{IK}	DC输入钳位电流		-50		mA
I_{OUT}	DC输出电流 – V_{SW}			128	mA
T_{STG}	储存温度		-65	+150	°C
MSL	湿度敏感性			1	等级
ESD	人体电流模式, JEDEC: JESD22-A114	所有管脚		4	kV
		I/O 接地		8	
	充放电模式, JEDEC: JESD22-C101			2	

注解:

1. 如输入及输出二极管电流额定值均达到时则可能会超出输入及输出负额定值。

推荐工作条件

推荐工作条件表中定义的是实际元件工作的条件。 推荐工作条件指定用于保证实现数据表规范的最佳性能, Fairchild 建议不得超出以上值或设计至最大绝对额定值。

表达符号	参数	最小值	最大值	单位
V_{CC}	供电电压	2.7	3.6	V
V_{CNTRL}	控制输入电压 (Sel, /OE)(2)	0	V_{CC}	V
V_{SW}	开关 I/O电压 1Bn, 2Bn, nA	-0.5	V_{CC}	V
I_{OUT}	DC输出电流 1Bn, 2Bn, nA		25	mA
T_A	操作温度	-40	85	°C

注解:

2. 控制输入必须保持高平或 低平且不得悬空。

DC电气特性

如未说明均为25ºC, 3.3V V_{CC}下的标准值.

表达符号	参数	条件	V_{CC} (V)	T_A = - 40ºC 至+85ºC			单位
				最小	典型	最大	
V_{IK}	钳位二极管电压	I_{IN} = -18mA	2.7			-1.2	V
V_{IH}	输入电压高电平		2.7 至 3.0	1.8			V
			3.3 至 3.6	2.0			
V_{IL}	输入电压低电平		2.7 至3.6			0.8	V
I_{IN}	控制输入漏电流(Sel)	V_{SW} = 0 to V_{CC}	3.6	-1		1	µA
$I_{nc(off)}$, $I_{no(off)}$,	断开漏电流	1Bn, 2Bn = 0V or Vcc 图4	3.6	-1		1	µA
R_{ON}	数据路径开关导通电阻(3)	V_{SW} = 0, 2.0V, I_{ON} = -20mA 图3, 图12	2.7		5.0	7.0	Ω
ΔR_{ON}	数据路径Δ导通电阻(4)	V_{SW} = 0V, I_{ON} = -20mA	2.7		0.3		Ω
I_{CC}	静态工作电流	V_{CNTRL} = 0 或V_{CC}, I_{OUT} = 0	3.6			1.0	µA

注解:

3. 在开关指定电流下, 通过测量管脚nB0, 1Bn和相关的共同端之间的电压降获得. 导通电阻由两管脚上较低的电压决定。
4. 由特性保证。

AC电气特性

如未说明均为25ºC, 3.3V V_{CC}下的标准值.

表达符号	参数	条件	V_{CC} (V)	T_A = - 40ºC to +85ºC			单位
				最小	典型	最大	
t_{ON}	开启时间Sel 或 /OE至输出 (nA)	R_L = 50Ω, C_L = 30pF V_{SW} = 1.5V 图5, 图6	2.7 至 3.6			7.0	ns
t_{OFF}	关闭时间Sel 或 /OE至输出 (nA)	R_L = 50Ω, C_L = 30pF V_{SW} = 1.5V 图5, 图6	2.7 至 3.6			4.0	ns
O_{IRR}	隔离度(5) (nA)	R_L = 50Ω, f = 25MHz, C_L = 30pF 图9, 图13	2.7 至 3.6		-45		dB
Xtalk	非相邻通道串扰(5) (nA)	R_L = 50Ω, f = 25MHz, C_L = 30pF 图7	2.7至 3.6		-54		dB
BW	-3db带宽(5) (nA)	R_L = 50Ω, C_L = 30pF 图8, 图14	2.7至 3.6		>160		MHz

注解:

5. 由特性保证.

电容

表达符号	参数	条件	T_A = - 40ºC 至 +85ºC			Units
			最小	典型	最大	
C_{IN}	控制端输入电容	V_{CC} = 0V		1.8		pF
C_{ON}	导通电容(6) (nA)	V_{CC} = 3.3V, f = 1MHz 图10		12.0		pF
C_{OFF}	断开电容(6) (nA)	V_{CC} = 3.3V 图9		6.0		pF

Note:

6. 由特性保证.

测试图

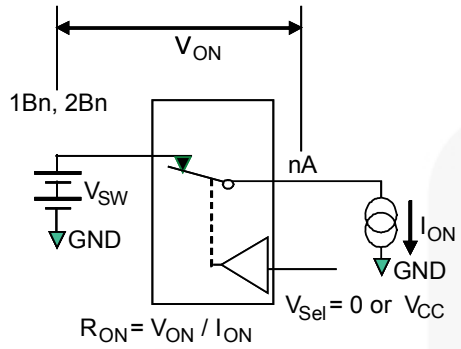


图3.导通电阻

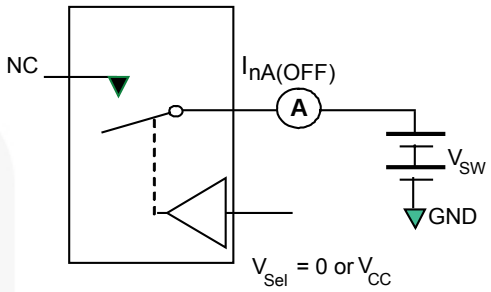
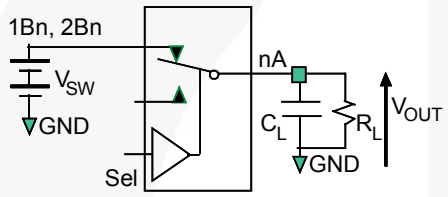


图4。断开漏电流



R_L and C_L are functions of the application environment (see tables for specific values).
C_L includes test fixture and stray capacitance.

图5. AC测试电路负载

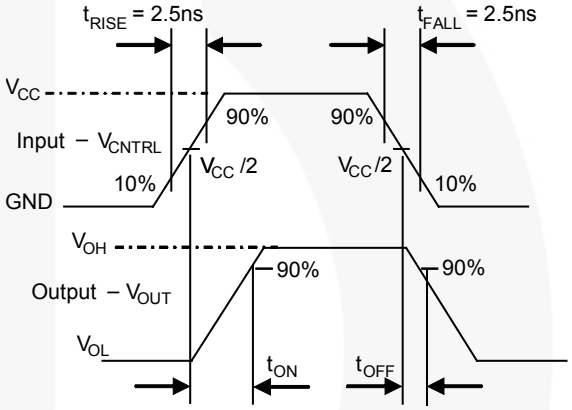
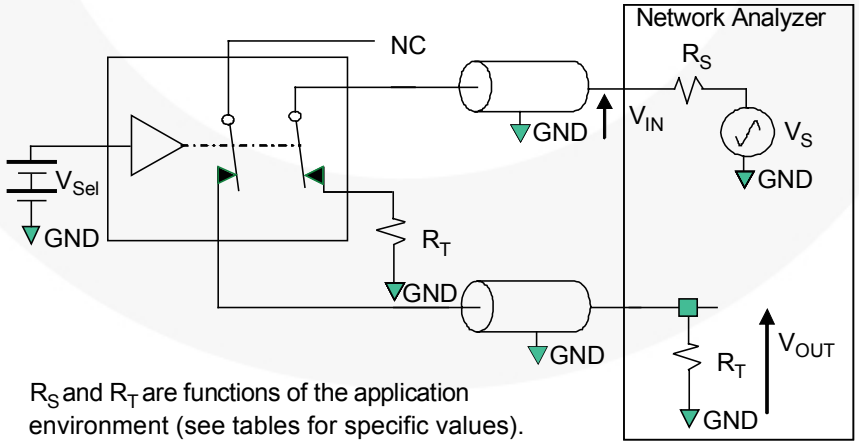


图6.开启 / 关闭波形

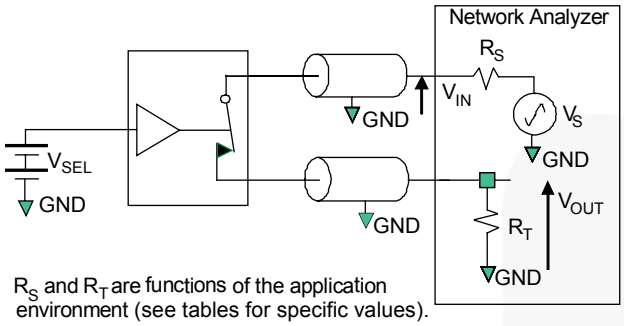


R_S and R_T are functions of the application environment (see tables for specific values).

Crosstalk = 20 Log (V_{OUT} / V_{IN})

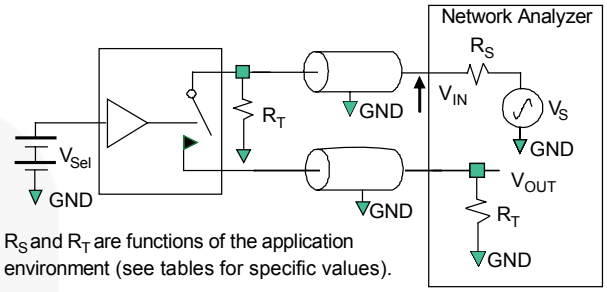
图7.非相邻通道串扰

测试图(续)



R_S and R_T are functions of the application environment (see tables for specific values).

图8.带宽



R_S and R_T are functions of the application environment (see tables for specific values).

Off Isolation = 20 Log (V_{OUT} / V_{IN})

图9.通道隔离度

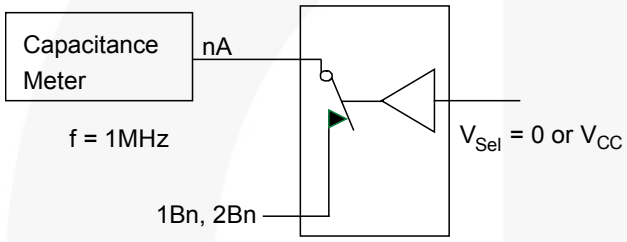


图10.通道导通电容

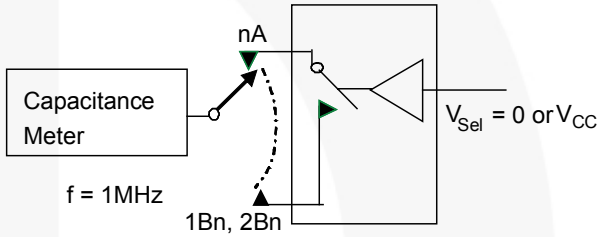


图11. 通道断开电容

典型特性

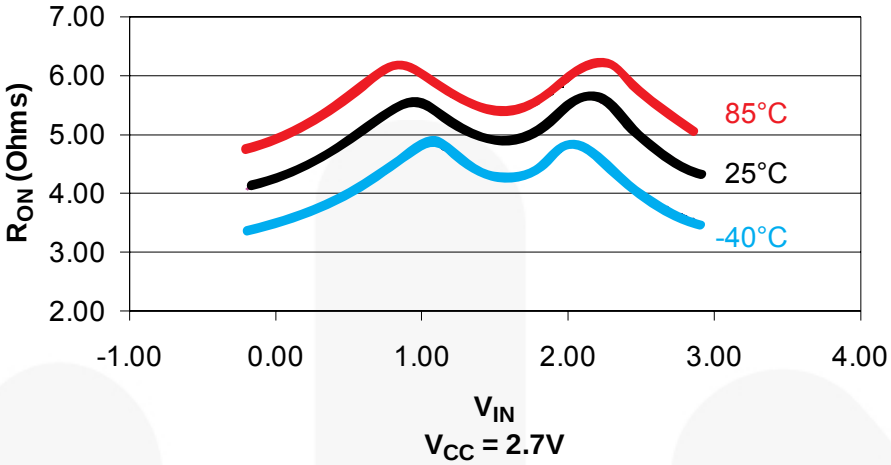


图12. R_{ON}

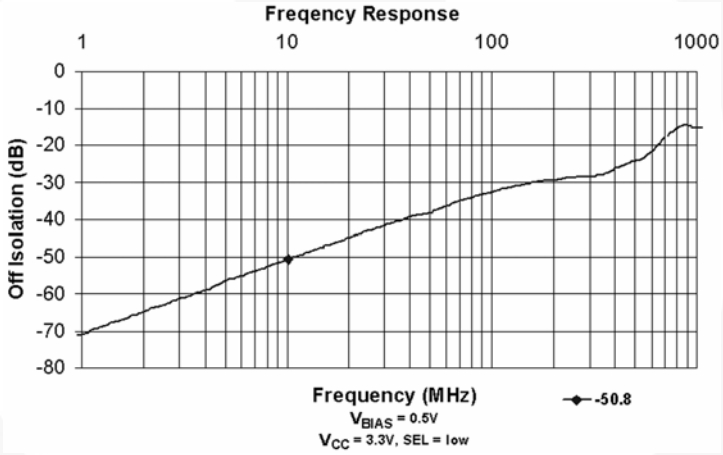


图13.隔离度

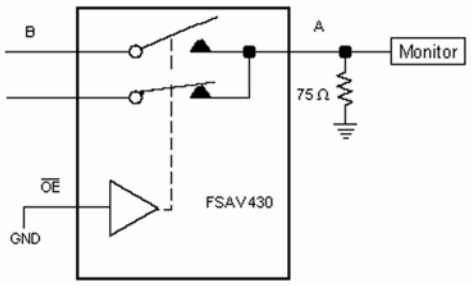
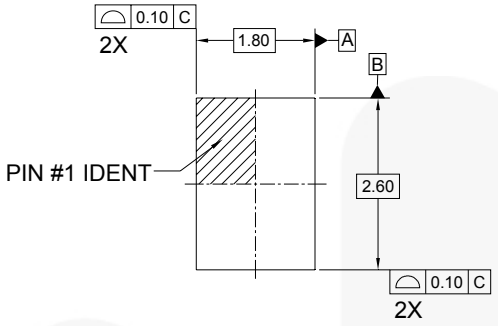
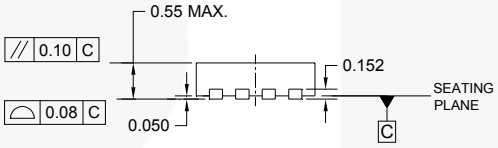


图14. 带宽

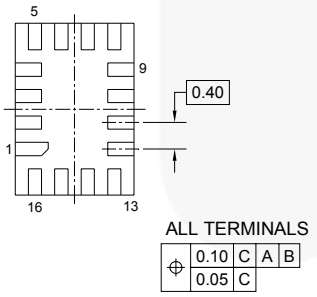
物理尺寸



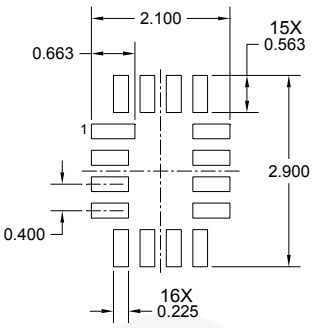
TOP VIEW



SIDE VIEW

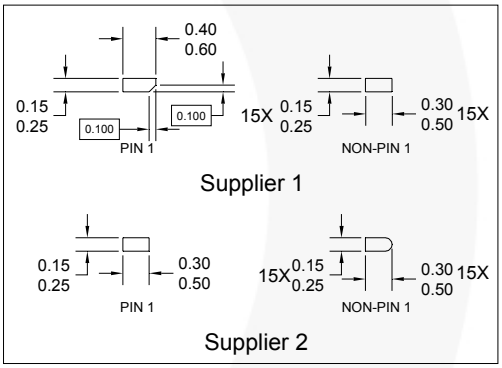


BOTTOM VIEW



RECOMMENDED LAND PATTERN

TERMINAL SHAPE VARIANTS



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E. LAND PATTERN IS A MINIMAL TOE DESIGN
F. DRAWING FILE NAME : UMLP16AREV3

图15.16-引脚，方型, 超薄模塑无脚封装 (UMLP)

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I42

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