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FSA2276 — DPDT (0.5 Ω) HiFi Audio Switch w/ Negative Swing

Features

- V_{DD} Operating Range: 1.65 to 5.5 V
- External Capacitor Connection for Pop and Click Noise Suppression
- Power-Off Protection on Common Ports
- R_{ON} = 0.5 Ω (Typ.) at 1.8 V
- THD+N = -115 dB; 2 V_{RMS}, 20 kΩ Load; f = 1 kHz
- X_{TALK} = -122 dB at 1 V_{RMS}, 50 Ω Load; f = 1 kHz
- Off Isolation = -115 dB at 1 V_{RMS}, 50 Ω Load; f = 1 kHz
- 12-Lead UMLP 1.8 mm x 1.8 mm

Applications

- Mobile Phone, Tablet, Notebook PC, Media Player
- Docking Station, TV, Set-Top Box, LCD Monitor

Description

The FSA2276 is a high-performance, Double-Pole Double-Throw (DPDT) analog switch with negative swing audio capability. The FSA2276 features ultra-low audio R_{ON} of 0.5 Ω (typical) at 1.8 V V_{DD}. The FSA2276 operates over a V_{DD} range of 1.65 V to 5.5 V, is fabricated with sub-micron CMOS technology to achieve fast switching speeds, and is designed for break-before-make operation. To minimize pop and click during operation, the turn on ramp time is selectable using an external capacitor (C_EXT).

The FSA2276 features THD+N specifications that target a Hi-Fidelity audio quality into both 32 Ω headphones and line out type loads (>600 Ω).

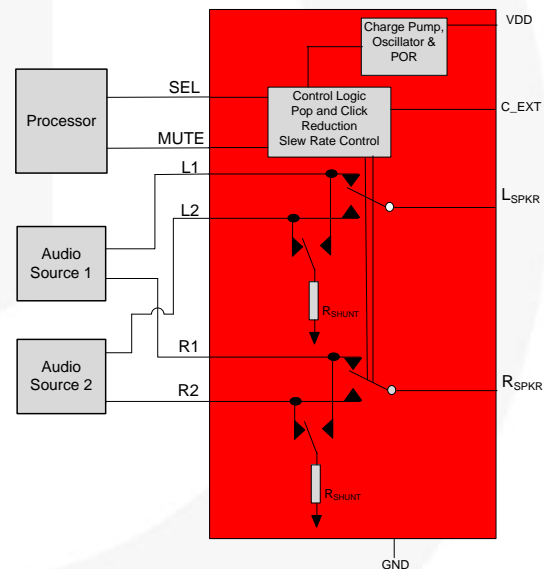


Figure 1. Application Block Diagram

Ordering Information

Part Number	Top Mark	Package Description
FSA2276UMX	EN	12-Lead, UMLP, Quad, JEDEC MO252, 1.8 mm x 1.8 mm

Pin Configuration

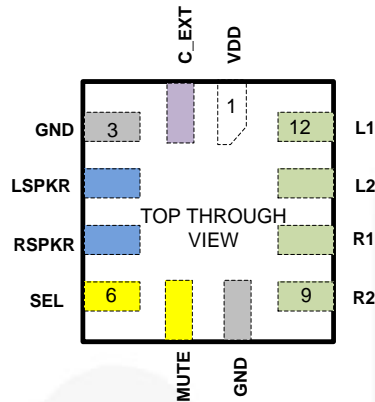


Figure 2. Pin Assignment (Top Through View)

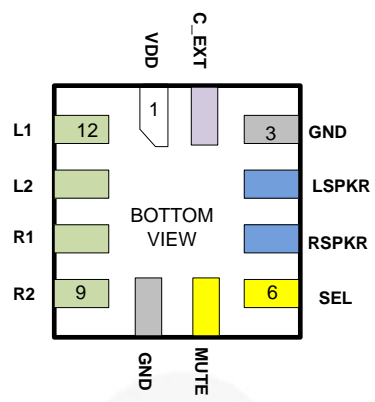


Figure 3. Pin Assignment (Bottom View)

Pin Descriptions

Pin	Name	Description
1	VDD	Power Supply (1.65 to 5.5 V)
2	C_EXT	Slow Turn On External Capacitor
3	GND	Ground
4	LSPKR	Audio L _{SPPKR} Common I/O Port
5	RSPKR	Audio R _{SPPKR} Common I/O Port
6	SEL	Select Pin
7	MUTE	Mute Enable - Active High
8	GND	Ground
9	R2	Audio – Right Channel Source2 I/O Port
10	R1	Audio – Right Channel Source1 I/O Port
11	L2	Audio – Left Channel Source2 I/O Port
12	L1	Audio – Left Channel Source1 I/O Port

Truth Table

Mute	SEL	Function	Resistor Terminations
0	0	L1 = L _{SPKR} ; R1 = R _{SPKR}	R _{SHUNT(s)} connect to L2/R2
0	1	L2 = L _{SPKR} ; R2 = R _{SPKR}	R _{SHUNT(s)} connect to L1/R1
1	0	L1 ≠ L _{SPKR} ; L2 ≠ L _{SPKR} ; R1 ≠ R _{SPKR} ; R2 ≠ R _{SPKR} (All Paths Hi-Z)	R _{SHUNT(s)} OPEN
1	1	L1 ≠ L _{SPKR} ; L2 ≠ L _{SPKR} ; R1 ≠ R _{SPKR} ; R2 ≠ R _{SPKR} (All Paths Hi-Z)	R _{SHUNT(s)} OPEN

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V _{DD}	Supply/Control Voltage		-0.3	6.0	V
V _{CNTRL}	Control Input Voltage	SEL, MUTE	-0.3	6.0	V
V _{SW}	DC Switch I/O Voltage	L1, L2, R1, R2, L _{SPKR} , R _{SPKR}	-3.5	3.5	V
I _{IK}	ESD Input Diode Current			-50	mA
I _{SW}	Switch I/O Current			700	mA
ESD	Human Body Model, ANSI/ESDA/ JEDEC JS-001-2012	All Pins	5		kV
	Charged Device Model, JEDEC: JESD22-C101		2		
	IEC 61000-4-2 System	Contact	8		
		Air Gap	15		
T _A	Absolute Maximum Operating Temperature		-40	+85	°C
T _{STG}	Storage Temperature		-65	+150	°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		1.65	1.80	5.50	V
V _{SW}	DC Switch I/O Voltage	L1, L2, R1, R2, L _{SPKR} , R _{SPKR}	-3.0		3.0	V
V _{CNTRL}	Control Input Voltage	SEL, MUTE	0		V _{DD}	V
I _{SW}	DC Switch I/O Current			100		mA
T _A	Ambient Operating Temperature		-40	25	+85	°C

DC Characteristics

$V_{DD} = 1.65 \text{ V to } 5.5 \text{ V}$, $V_{DD} (\text{Typ.}) = 1.8 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$, and $T_A (\text{Typ.}) = 25^\circ\text{C}$, unless otherwise specified.⁽¹⁾

Symbol	Parameter	Condition	V_{DD} (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			Unit
				Min.	Typ.	Max.	
V_{IH}	VCNTRL Pin Input High Voltage (SEL, MUTE)	$C_{EXT} = \text{FLOAT}$		1.17		VDD	V
V_{IL}	VCNTRL Pin Input Low Voltage (SEL, MUTE)	$C_{EXT} = \text{FLOAT}$		0		0.5	V
I_{ON}	Switch-to-Gnd ON Leakage Current	$L1, R1, L2, R2 = -3 \text{ V to } 3 \text{ V}$, L_{SPKR} , $R_{SPKR} = \text{Float}$ ($I_{SW} = 0 \text{ mA}$) MUTE=LOW, SEL=0 or VDD $C_{EXT} = \text{FLOAT}$, Figure 6	1.65 to 5.5	-1.0	0.1	1.0	μA
I_{NO_MUTE}	Switch-to-Gnd OFF Leakage Current (when Muted)	$L1, R1, L2, R2 = -3 \text{ V to } 3 \text{ V}$, L_{SPKR} , $R_{SPKR} = \text{Float}$ ($I_{SW} = 0 \text{ mA}$) MUTE = HIGH, SEL = 0 or VDD $C_{EXT} = \text{FLOAT}$, Figure 5	1.65 to 5.5	-1.0	0.1	1.0	μA
I_{OFF}	Input Leakage Current ⁽²⁾	$L1, R1, L2, R2 = -3 \text{ V to } 3 \text{ V}$, L_{SPKR} , $R_{SPKR} = \text{Float}$ ($I_{SW} = 0 \text{ mA}$) MUTE = LOW, SEL = 0 or VDD, $C_{EXT} = \text{FLOAT}$	0	-1.0	0.1	1.0	μA
I_{IN}	Control Input Leakage Current ⁽³⁾ (SEL, MUTE)	$L1, R1, L2, R2 = -3 \text{ V to } 3 \text{ V}$, L_{SPKR} , $R_{SPKR} = \text{Float}$ ($I_{SW} = 0 \text{ mA}$), $C_{EXT} = \text{FLOAT}$	1.65 to 5.5	-0.5	0.1	0.5	μA
I_{DD}	VDD Supply Current	MUTE = LOW, SEL = 0 or VDD, $C_{EXT} = \text{FLOAT}$	5.5		16	30	μA
I_{DDZ}	VDD Hi-Z Supply Current	MUTE = HIGH, SEL = 0 or VDD, $C_{EXT} = \text{FLOAT}$	5.5			1	μA
I_{DDT}	Increase in IDD per Control Voltage	MUTE = LOW, SEL = 0 or 1.8 V SEL = LOW, MUTE = 0 or 1.8 V $C_{EXT} = \text{FLOAT}$	5.5			1	μA
R_{ON}	Switch On Resistance	$I_{SW} = 100 \text{ mA}$, $V_{SW} = -3 \text{ V to } 3 \text{ V}$ $C_{EXT} = \text{FLOAT}$, Figure 4	1.65 to 5.5		0.5	1.0	Ω
ΔR_{ON}	On Resistance Matching, Channel to Channel	$I_{SW} = 100 \text{ mA}$, $V_{SW} = -3 \text{ V to } 3 \text{ V}$ $C_{EXT} = \text{FLOAT}$	1.65 to 5.5		30		m Ω
R_{FLAT}	On Resistance Flatness	$I_{SW} = 100 \text{ mA}$, $V_{SW} = -3 \text{ V to } 3 \text{ V}$ $C_{EXT} = \text{FLOAT}$	1.65 to 5.5		1		m Ω
R_{SHUNT}	Click and Pop Resistance (L1, L2, R1, R2, L_{SPKR} , R_{SPKR})	$V_{LX_RX} = 3.0 \text{ V}$, MUTE = 0, SEL = 0 or VDD, $C_{EXT} = \text{FLOAT}$		6	10	14	k Ω

Notes:

- Limits over the recommended temperature operating range ($T_A = -40^\circ\text{C to } +85^\circ\text{C}$) are correlated by statistical quality.
- Only valid for $V_{SW} > 0 \text{ V}$.
- $V_{MUTE} \leq V_{DD} + 0.3$ otherwise additional input leakage current may flow.

AC Characteristics

$V_{DD} = 1.65 \text{ V to } 5.5 \text{ V}$, $V_{DD} (\text{Typ.}) = 1.8 \text{ V}$. $T_A = -40^\circ\text{C to } 85^\circ\text{C}$. $T_A (\text{Typ.}) = 25^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Condition		$V_{DD} (\text{V})$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			Unit
					Min.	Typ.	Max.	
$t_{\text{MUTE_ON}}$	Enable Time (MUTE to Output)	L1 = R1 = L2 = R2 = 1.5 V, L_{SPKR} , $R_{\text{SPKR}} = 50 \Omega$ to GND, SEL = 0 or V_{DD} ; See Figure 7 and Figure 8	C_EXT = Float	1.8, 3.3		0.5		ms
			C_EXT = 0.1 μF	1.8		60		
			C_EXT = 0.1 μF	3.3		100		
$t_{\text{ON_MUTE}}$	Disable Time (MUTE to Output)	L1 = R1 = L2 = R2 = 1.5 V, L_{SPKR} , $R_{\text{SPKR}} = 50 \Omega$ to GND, SEL = 0 or V_{DD} ; See Figure 7 and Figure 8	C_EXT = Float	1.8, 3.3		35		μs
			C_EXT = 0.1 μF			35		
$t_{\text{ON_SEL}}$	Turn On Time (SEL to Output)	L1 (L2) = R1 (R2) = 1.5 V, L2 (L1) = R2 (R1) = 0 V, L_{SPKR} , $R_{\text{SPKR}} = 50 \Omega$ to GND, SEL = 0 or V_{DD} ; MUTE = 0 See Figure 7 and Figure 8	C_EXT = Float	1.8, 3.3		0.5		ms
			C_EXT = 0.1 μF	1.8		50		
			C_EXT = 0.1 μF	3.3		100		
$t_{\text{OFF_SEL}}$	Turn On Time (SEL to Output)	L1 (L2) = R1 (R2) = 1.5 V, L2 (L1) = R2 (R1) = 0 V, L_{SPKR} , $R_{\text{SPKR}} = 50 \Omega$ to GND, SEL = 0 or V_{DD} ; MUTE = 0 See Figure 7 and Figure 8	C_EXT = Float	1.8, 3.3		20		μs
			C_EXT = 0.1 μF			20		
t_{BBM}	Break Before Make Time (SEL to Output)	L1 (L2) = R1 (R2) = 1.5 V, L_{SPKR} , $R_{\text{SPKR}} = 50 \Omega$ to GND, SEL = 0 or V_{DD} ; C_EXT = FLOAT, MUTE = 0 V; See Figure 7 and Figure 9		1.8, 3.3		500		μs
O_{IRR}	Off Isolation ⁽⁴⁾	f = 1 kHz, $R_L = 50 \Omega$, $C_L = 0 \text{ pF}$, MUTE = 0 $V_{\text{SW}} = 1 V_{\text{RMS}}$ Figure 11		1.8, 3.3		-115		dB
		f = 1 MHz, $R_L = 50 \Omega$, $C_L = 0 \text{ pF}$, MUTE = 0 $V_{\text{SW}} = 1 V_{\text{RMS}}$ Figure 11				-92		
O_{IRRM}	Off Isolation-Muted ⁽⁴⁾	f = 1 kHz, $R_L = 50 \Omega$, $C_L = 0 \text{ pF}$, MUTE = V_{DD} ; $V_{\text{SW}} = 1 V_{\text{RMS}}$ Figure 11		1.8, 3.3		-113		dB
		f = 1 MHz, $R_L = 50 \Omega$, $C_L = 0 \text{ pF}$, MUTE = V_{DD} ; $V_{\text{SW}} = 1 V_{\text{RMS}}$ Figure 11				-95		
X_{TALK}	Cross Talk (Adjacent) ⁽⁴⁾	f = 1 kHz, $R_L = 50 \Omega$, $V_{\text{SW}} = 1 V_{\text{RMS}}$ Figure 12		1.8, 3.3		-122		dB
BW	-3 dB Bandwidth ⁽⁴⁾	$R_L = 50 \Omega$ Figure 10		1.8, 3.3		380		MHz
PSRR	Power Supply Rejection Ratio ⁽⁴⁾	$V_{\text{PSRR}} = V_{DD} + 100 \text{ mV}_{\text{RMS}}$, $R_L = 20 \text{ k}\Omega$ or 32Ω (at L_{SPKR} , R_{SPKR}), MUTE = 0 or V_{DD} , f = 1 kHz, $V_{\text{SW}} = \text{GND or Float}$)	$R_L = 32 \Omega$	1.8, 3.3		-119		dB
			$R_L = 20 \text{ k}\Omega$			-105		
THD+N	Total Harmonic Distortion + Noise ⁽⁴⁾	$R_L = 20 \text{ k}\Omega$, f = 1 kHz, $V_{\text{SW}} = 2 V_{\text{RMS}}$, With A-weighted, Figure 15				0.00018		%
						-115		dB
			$R_L = 600 \Omega$, f = 1 kHz, $V_{\text{SW}} = 2 V_{\text{RMS}}$ With A-weighted, Figure 15			0.00018		%
						-115		dB
			$R_L = 32 \Omega$, f = 1 kHz, $V_{\text{SW}} = 1 V_{\text{RMS}}$, With A-weighted, Figure 15			0.00018		%
						-115		dB

Note:

4. Guaranteed by characterization. Not production tested.

Capacitance

Unless otherwise stated, $V_{DD} = 1.65\text{ V to }5.5\text{ V}$, $V_{DD}(\text{Typ.}) = 1.8\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$, and $T_A(\text{Typ.}) = 25^\circ\text{C}$.⁽⁵⁾

Symbol	Parameter	Condition	V_{DD} (V)	$T_A = -40^\circ\text{C to }+85^\circ\text{C}$			Unit
				Min.	Typ.	Max.	
C_{ON}	On Capacitance (Common Port) ⁽⁶⁾	$f = 1\text{ MHz}$, 100 mV_{PK-PK} , 100 mV DC bias MUTE = 0 V Figure 14	1.8, 3.3		22		pF
C_{OFF1}	Off Capacitance (Common Port) ⁽⁶⁾	$f = 1\text{ MHz}$, 100 mV_{PK-PK} , 100 mV DC bias MUTE = V_{DD} Figure 13	1.8, 3.3		25		pF
C_{OFF2}	Off Capacitance (Non-Common Ports) ⁽⁶⁾	$f = 1\text{ MHz}$, 100 mV_{PK-PK} , 100 mV DC bias MUTE = 0 V Figure 13	1.8, 3.3		14		pF
C_{OFF_MUTE}	Off Capacitance - MUTED (Non-Common Ports) ⁽⁶⁾	$f = 1\text{ MHz}$, 100 mV_{PK-PK} , 100 mV DC bias, MUTE = V_{DD}	1.8, 3.3		14		pF
C_{CNTRL}	Control Input Pin Capacitance (MUTE, SEL) ⁽⁶⁾	$f = 1\text{ MHz}$, 100 mV_{PP} , 100 mV DC bias	0	SEL	3		pF
				MUTE	6		

Notes:

5. Limits over the recommended temperature operating range ($T_A = -40^\circ\text{C to }+85^\circ\text{C}$) are correlated by statistical quality control methods.
6. Guaranteed by characterization. Not production tested.

Test Diagrams

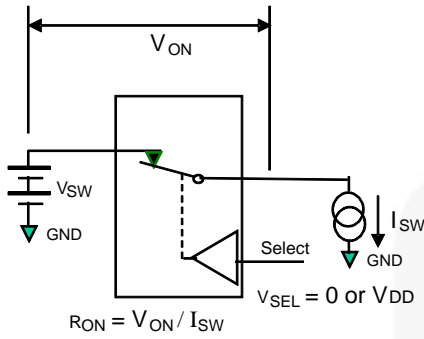


Figure 4. On Resistance

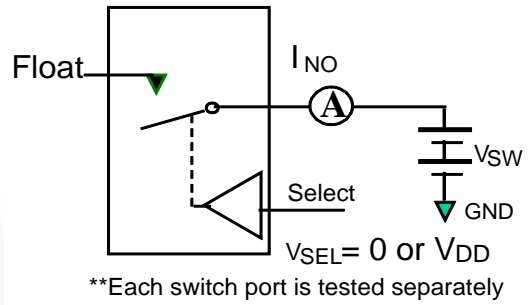


Figure 5. Off Leakage

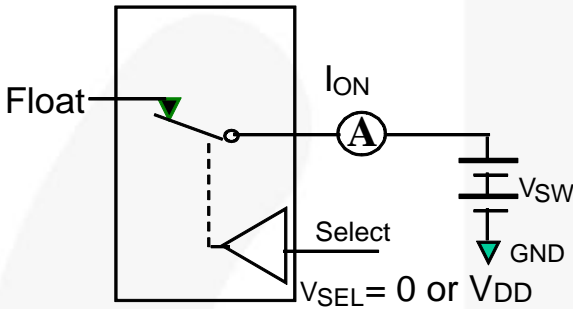


Figure 6. On Leakage

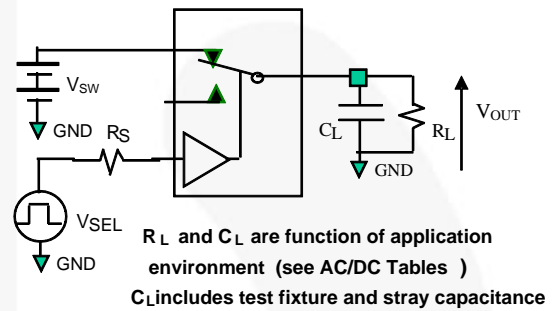


Figure 7. Test Circuit Load

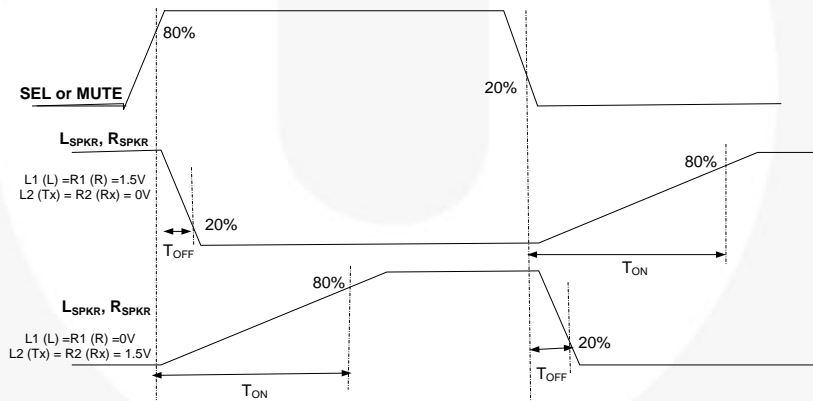


Figure 8. Turn On/Off Waveforms (SEL or MUTE to Output)

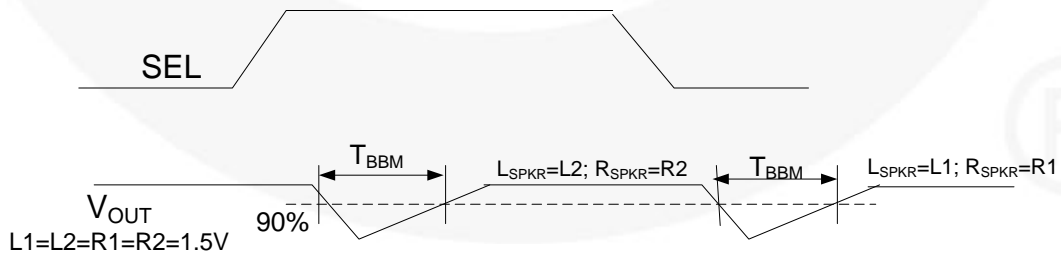


Figure 9. Break Before Make Interval Timing

Test Diagrams (Continued)

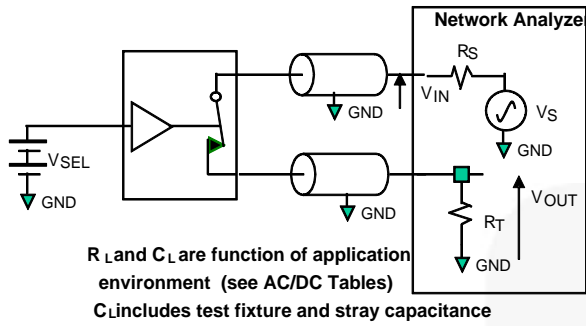


Figure 10. Bandwidth

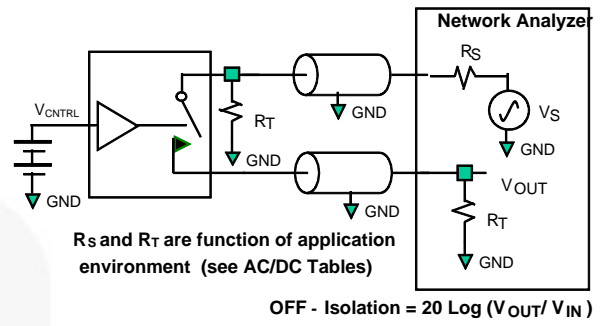


Figure 11. Channel Off Isolation

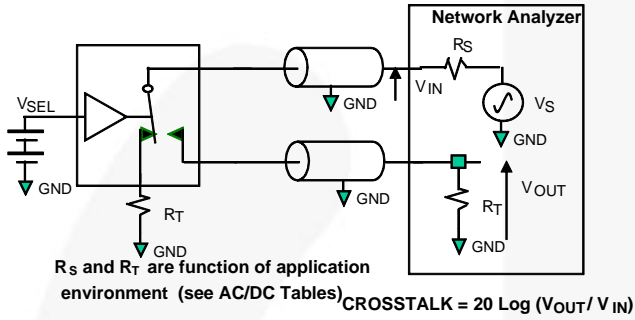


Figure 12. Adjacent Channel Crosstalk

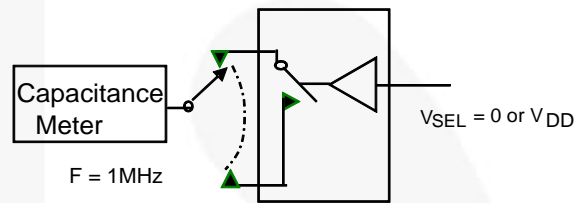


Figure 13. Channel Off Capacitance

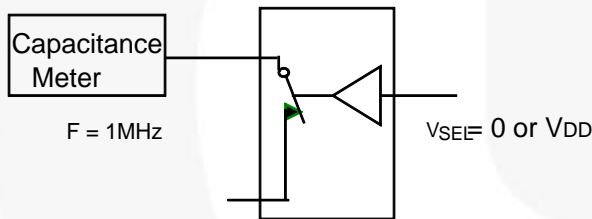


Figure 14. Channel On Capacitance

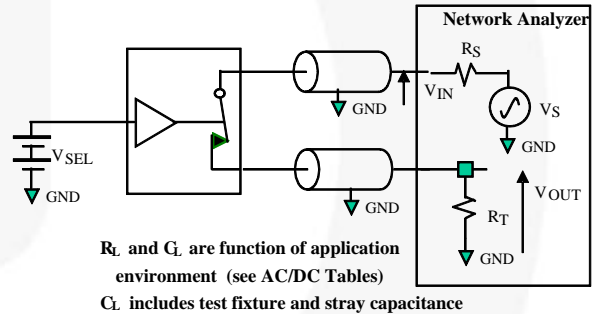
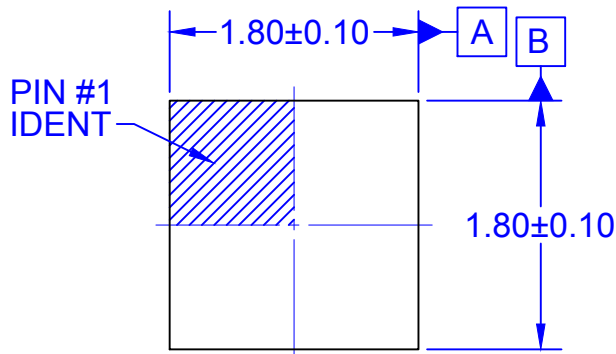
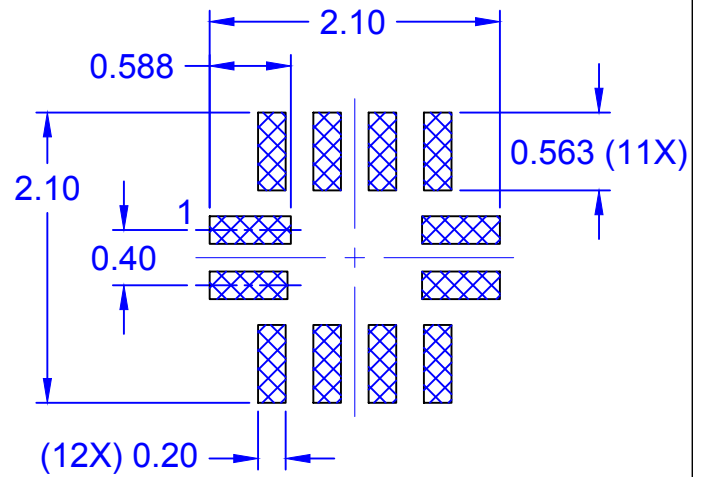


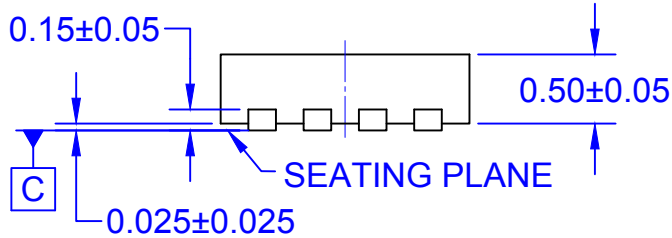
Figure 15. Total Harmonic Distortion (THD+N)



TOP VIEW



RECOMMENDED LAND PATTERN

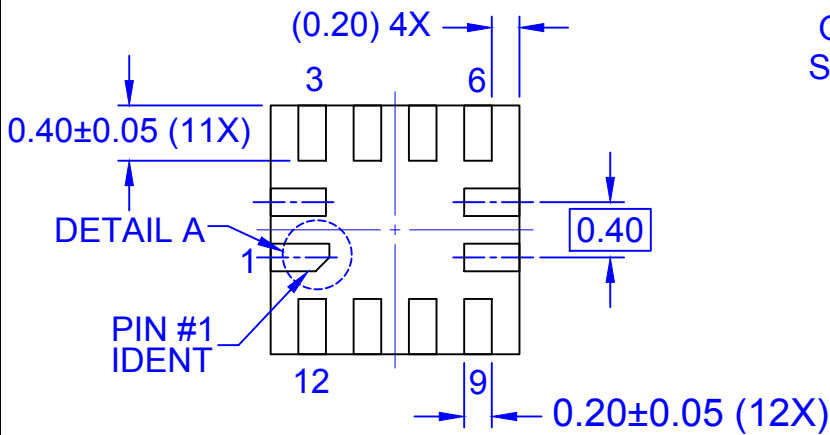


SIDE VIEW



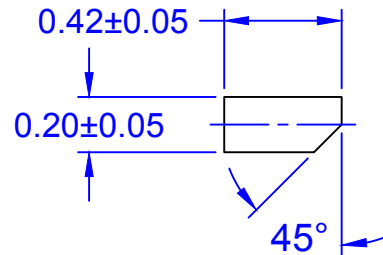
LEAD OPTION 1
SCALE 2:1

LEAD OPTION 2
SCALE 2:1



BOTTOM VIEW

⊕	0.10	C	A	B
	0.05	C		



DETAIL A
SCALE 2:1

NOTES:

- A. PACKAGE DOES NOT CONFORM TO ANY JEDEC STANDARD.
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