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March 2013

FSA2268 / FSA2268T 低电压及拥有高达 16kV ESD 的二通道 单刀双掷 (0.4Ω) 模拟开关

特点

- 0.4Ω 典型导通电阻 (+3.0V 供电电压)
- 0.25Ω 最大 R_{ON} 平坦度 (+3.0V 供电电压)
- -3db 带宽: > 50MHz
- 在扩展的控制信号电平范围内拥有低漏电流
- 无铅 10-管脚 µMLP (1.4 x 1.8mm) 的封装
- 共用端口的断电保护
- 宽广的Vcc 操作范围: 1.65 到 4.3V
- 人体电流模式 JEDEC: JESD22-A114
 - I/O 接地: 13.5kV
 - 电源接地:16.0kV
- 在 FSA2268T 中拥有噪音消除终端电阻

应用

- 手机, PDA (掌上电脑), 数码相机和笔记本电脑
- 液晶显示器, 电视及机顶盒

总述

FSA2268 是一种高性能,二通道单刀双掷模拟开关并拥有超低 R_{ON} 0.4Ω (典型值) 的特点。 FSA2268 可以在 V_{CC} 从 1.65V 到 4.3V 这么宽广的范围里工作,并被设计成先断后通的操作。它的选择输入端口是TTL兼容的。

即使在控制电压低于 V_{CC} 情况下 FSA2268 拥有非常低的静态电流,这一特性可以用最小的电池消耗来实现与基带处理器通用 I/O 之间的直接接口从而满足手机的应用。

FSA2268T 集成了终端电阻当信号有超调或串扰藕合时可以消除噪音,也就是说"爆音最小化"。

重要注解

欲知更多其它具体的操作信息,请联系 analogswitch @fairchildsemi.com.

订购信息

零件编号	表面标记	封装说明			
FSA2268UMX	GF	10-引脚, 方型超薄 (UMLP), 1.4 x 1.8mm, 0.4mm Pitch			
FSA2268TUMX	GH	10-引脚, 方型超薄 (UMLP), 1.4 x 1.8mm, 0.4mm Pitch			
FSA2268L10X	GH	10-引脚, MicroPak™, 1.6mm			

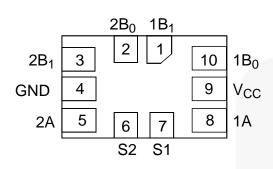
模拟符号



图 1. FSA2268

图 2. FSA2268T (含有抗扰终端电阻)

管脚分配图





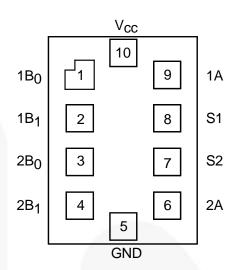


图 4. 10-管脚 Micropak™

管脚描述

管脚 号 UMLP	管脚号MicroPak™	名称	描述
1	2	1B ₁	数据端口
2	3	2B ₀	数据端口
3	4	2B ₁	数据端口
4	5	GND	接地
5	6	2A	数据端口
6	7	S2	开关选择脚
7	8	S1	开关选择脚
8	9	1A	数据端口
9	10	V _{CC}	供电电压
10	1	1B ₀	数据端口

真值表

控制输入, Sn 功能			
逻辑低	nB0 连接nA (FSA2268/2268T); nB1 接地 (FSA2268T)		
逻辑高	nB1 连接nA (FSA2268/2268T); nB0 接地 (FSA2268T)		

最大绝对额定值

超出绝对最大额定值会破坏设备,设备会不工作或者说不建议设备在和超过建议的工作条件下被操作. 另外,过长的暴露在超过建议工作条件下会影响设备的可靠性. 这种绝对最大额定值仅仅是极端额定值.

表达符号		参数	最小值	最大值	单位
Vcc	供电电压		-0.5	5.5	V
V	开关输入/输出电压 ⁽¹⁾	1B0, 1B1, 2B0, 2B1, 1A, 2A 管脚	-0.5	V _{CC} + 0.3	V
VSW	V _{sw} 开关输入/输出电压 ⁽¹⁾	T版本, nBn 管脚断开	0	1.4	V
V _{IN}	控制输入电压(1)	S1, S2	-0.5	5.5	V
I _{IK}	输入钳位二极管电流			-50	mA
I _{SW}	开关输入/输出电流 (连续)			350	mA
I _{SWPEAK}	峰值开关电流(脉冲持续时		500	mA	
T _{STG}	保存温度范围	-65	+150	°C	
TJ	最高结温			+150	°C
TL	引线温度 (焊接,10秒)			+260	°C
MSL	湿度敏感性			1	等级
/		I/O 接地	1	13.5	
	人体电流模式, JEDEC: JESD22-A114	电源接地	A.	16.0	\
ESD	OLDEO. GLODZZ-ATT4	其它各管脚		9.0	kV
	充放电模式, JEDEC: JESD22-C101		_	2.0	

注解:

1. 如输入及输出二极管电流额定值均到达时,则可能会超出输入及输出的负额定值.

建议工作条件

推荐工作条件指定用于保证实现数据表规范的最佳性能. Fairchild 建议不得超出以上值或设计至最大绝对额定值.

表达符号	参数	最小值	最大值	单位
V _{CC}	供电电压	1.65	4.30	V
V _{IN}	控制输入电压	0	V _{CC}	V
V_{SW}	开关I/O 电压	0	V _{CC}	V
T _A	工作温度	-40	+85	°C

DC电气特性

若无另外规定,所有数值均在25°C下测定。

	سد بد			T _A =+25°C			T _A =-40	to +85°C	36.05
表达符号	参数	条件	V _{CC} (V)	最小值	典型值	最大值	最小值	最大值	単位
			3.6 to 4.3				1.7		
.,	44 2 		2.7 to 3.6				1.5		٠,,
V_{IH}	输入高电平		2.3 to 2.7				1.4		V
			1.65 to 1.95				0.9		
			3.6 to 4.3					0.7	V
	松)似山亚		2.7 to 3.6					0.5	
V_{IL}	输入低电平		2.3 to 2.7					0.4	V
			1.65 to 1.95					0.4	
I _{IN}	控制输入漏电流 (S1,S2)	V _{IN} =0 to V _{CC}	1.65 to 4.3				-0.5	0.5	μΑ
I _{NO(0FF)} , I _{NC(0FF)} FSA2268	nB0 和 nB1端口断开 漏电流	nA=0.3V, V _{CC} - 0.3V nB0 or nB1=V _{CC} -0.3V, 0.3V, or Floating 图 6	1.95 to 4.3	-10		10	-50	50	nA
I _{NC(OFF)} FSA2268T	nB0 和 nB1端口断开 漏电流 (带有终端电阻)	nA=0.3V, nB0 or nB1=0V or Floating, 图 6	1.95 to 4.3	-10		10	-50	50	μΑ
I _{A(ON)}	nA导通漏电流	nA=0.3V, V _{CC} - 0.3V nB0 or nB1=V _{CC} -0.3V, 0.3V, or Floating, 图 7	1.95 to 4.3	-20		20	-100	100	nA
I _{OFF} FSA2268	断开漏电流 (1A, 2A共同端口)	Common Port (1A, 2A), V _{IN} =0V to 4.3V, V _{CC} =0V nB0, nB1=Floating	0V					±1	μΑ
I _{OFF} FSA2268T	断开漏电流 (1A, 2A共同端口)	Common Port (1A, 2A), $V_{\rm IN}$ =0V to 4.3V, $V_{\rm CC}$ =0V nB0, nB1=0V or Floating	oV					±40	μΑ
		I _{ON} =100mA, nB0 or nB1=0.7V, 3.6V, 图 5	4.30		0.30			0.50	
		I _{ON} =100mA, nB0 or nB1=0.7V, 2.3V, 图 5	3.00		0.40			0.55	
R _{ON}	开关导通电阻 ^{(2),(5)}	I _{ON} =100mA, nB0 or nB1=0V, 0.7V, 1.6V, 2.3V, 图 5	2.30		0.52			(P	Ω
		I _{ON} =100mA, nB0 or nB1=0V, 0.7V, 1.65V, 图 5	1.65		1.00			U	
			4.30		0.04			0.13	
4.5	Delta口导通电阻口	I _{oN} =100mA, nB0 or	3.00		0.06			0.13	_
ΔR_{ON}	(3),(5)	nB1=0.7V	2.30		0.12				Ω
			1.65		1.00				1

Continued on following page...

DC电气特性 (续)

若无另外规定,所有数值均在25°C下测定。

表达符号	参数	条件	V _{cc} (V)		T _A =+25°C	;	T _A =-46	- 单位														
12219 9	9 W	* 11	VCC (V)	最小值	典型值	最大值	最小值	最大值	十四													
			4.30					0.25														
		勺平坦 I _{OUT} =100mA, nB0 or nB1=0V to V _{CC}			I _{OUT} =100mA, nB0 or	3.00					0.25	Ω										
KFLAT(ON)					2.30		0.5				22											
			1.65		0.6																	
R _{TERM}	内部终端电阻(6)				200				Ω													
I _{CC}	静态工作电流	V _{IN} =0 or V _{CC} , I _{OUT} =0	4.30	-100		100	-500	500	nA													
1	控制输入时Icc 相	Input at 2.6V	4.30		3			7														
I _{CCT}	应的增加量	Input at 1.8V	4.30		7			15	μΑ													

注解:

- 2. 导通电阻由开关指定电流下A、B管脚之间的电压降决定.
- 3. $\Delta R_{ON} = R_{ON max} R_{ON min}$ 在相同 V_{CC} 、温度及电压下测得.
- 4. 平坦度定义为各种条件指定范围内on电阻最大值与最小值之间的差值.
- 5. 由特性保证而非产品试验, for V_{CC}=1.65-3.00.
- 6. 由特性保证而非产品试验.

AC电气特性

若无另外规定, 有数值均在 Vcc=3.3V 和 25°C下测定。

本 上	4 M	AT ALL	V 00		T _A =+25°C		T _A =-40°C	to +85°C	34 £3.	Del 다
表达符号	参数	条件	V _{CC} (V)	最小值	典型值	最大值	最小值	最大值	単位	图号
			3.6 to 4.3			55	15	60		
		nB0 or	2.7 to 3.6			60	15	65		
t _{ON}	开启时间	nB1=1.5V, R _L =50Ω,	2.3 to 2.7	1/		65	15	70	ns	
		C _L =35pF	1.65 to 1.95		70					图 8
			3.6 to 4.3			30	5	35		图 9
		nB0 or	2.7 to 3.6			35	5	40		
t _{OFF}	关闭时间	nB1=1.5V, R _L =50Ω,	2.3 to 2.7			40	5	45	ns	
		C _L =35pF	1.65 to 1.95		40					
	44	A.	3.6 to 4.3		15		2			
	先断后开 时间	nB0 or	2.7 to 3.6		15		2			
t _{BBM}		nB1=1.5V, R _L =50Ω,	2.3 to 2.7		15		2		ns	图 10
		C _L =35pF	1.65 to 1.95		16		2			
Q	电荷注入	$C_L=1.0nF, V_S=0V, R_S=0\Omega$	1.65 to 4.3		25				рС	图 14
OIRR	断开隔离	$\begin{array}{l} \text{f=100kHz,} \\ \text{R}_{\text{L}} = 50\Omega, \\ \text{C}_{\text{L}} = 0 \text{pF} \end{array}$	1.65 to 4.3		-70				dB	图 12
Xtalk	非相邻通 道串扰	$\begin{array}{l} \text{f=100kHz,} \\ \text{R}_{\text{L}} = 50\Omega, \\ \text{C}_{\text{L}} = 0 \text{pF} \end{array}$	1.65 to 4.3		-70				dB	图 13
BW	-3db 带宽	$R_L=50\Omega$, $C_L=0$ pF	1.65 to 4.3		>50				MHz	图 11
THD	总谐波失 真	$\begin{array}{l} \text{f=20Hz to} \\ \text{20kHz}, \\ \text{R}_{\text{L}}\text{=}32\Omega, \\ \text{V}_{\text{IN}}\text{=}2\text{V}_{\text{pp}} \end{array}$	1.65 to 4.3		.06				%	图 17

电容

丰 上	** ** ** ** ** ** ** **			T _A =+25°	单位	स्त्र 🗆		
表达符号	参数	条件	V _{CC} (V)	最小值	典型值	最大值	平 位	图号
C _{IN}	控制端输入电容	f=1MHz	0		1.5		pF	图 15
C _{OFF}	B 端断开电容	f=1MHz	3.3		30		pF	图 15
C _{ON}	A 端导通电容	f=1MHz	3.3		120		pF	图 16

测试框图

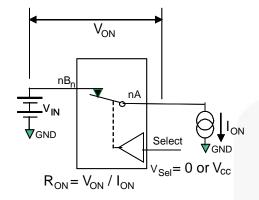
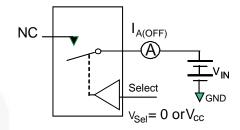


图 5. 导通电阻



**Each switch port is tested separately.

图 6. 断开漏电流(端口分开测试)

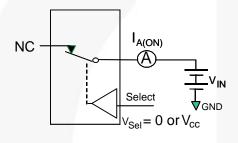


图 7. 导通漏电流

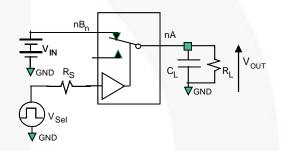


图 8. 测试电路负载

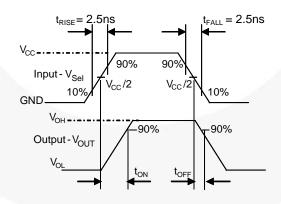


图 9. 开启/关闭波形

测试框图(续)

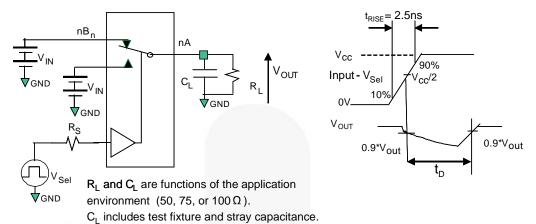


图 10. 先关后开间隔时间

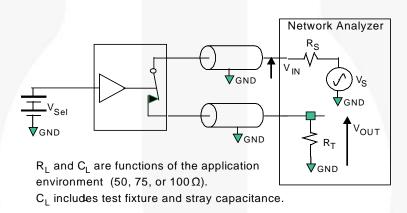


图 11. 带宽

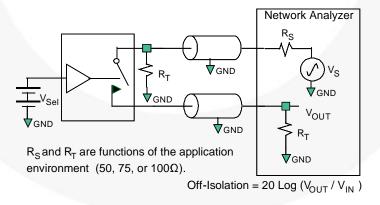
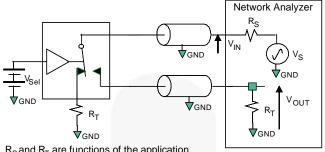


图 12. 线路断开Off 隔离

测试框图 (续)



 R_S and R_T are functions of the application environment (50, 75, or 100 Ω). CROSSTALK = 20 Log (V_{OUT}/V_{IN})

图 13. 相邻通道间的串扰

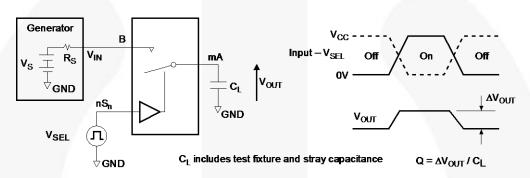


图 14. 电荷注入测试

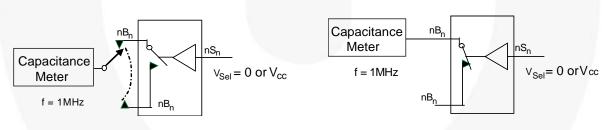
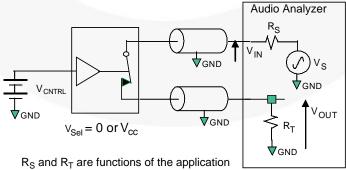


图 15. 通道断开电容

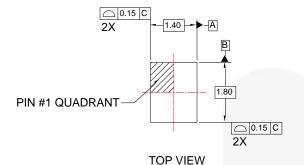
图 16. 通道导通电容

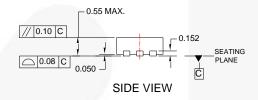


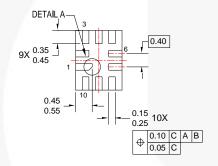
environment (see AC Tables for specific values).

图 17. 总谐波失真

物理尺寸



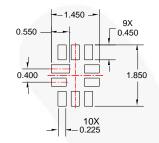




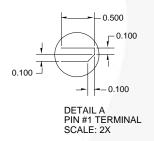
BOTTOM VIEW

0.663 9X 0.563 2.100 0.400 10X 0.225

RECOMMENDED LAND PATTERN



OPTIONAL MINIMIAL TOE LAND PATTERN



NOTES:

- A. DIMENSIONS ARE IN MILLIMETERS.
- B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M. 1994
- C. DRAWING FILENAME: UMLP10Arev2

图 18. 10-引脚方形超薄

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: http://www.fairchildsemi.com/packaging/.

For current tape and reel specifications, visit Fairchild Semiconductor's online packaging area: http://www.fairchildsemi.com/products/analog/pdf/UMLP10_TNR.pdf.

Physical Dimensions (Continued) 0.10 C 2.10 2X 1.62 В KEEPOUT ZONE, NO TRACES OR VIAS ALLOWED (0.11) -0.56 1.12 1.60 PIN1 IDENT IS □ 0.10 C (0.35) 10X 2X LONGER THAN OTHER LINES 2X 0.50 (0.25) 10X **TOP VIEW** RECOMMENDED LAND PATTERN 0.55 MAX // 0.05 C ○ 0.05 C (0.20) 0.05 C SIDE VIEW (0.15) b **DETAIL A** (0.36)0.65 0.55 0.35 0.25 DETAIL A 2X SCALE 0.56 NOTES: A. PACKAGE CONFORMS TO JEDEC REGISTRATION MO-255, VARIATION UABD. (0.29) B. DIMENSIONS ARE IN MILLIMETERS. 0.50 C. DIMENSIONS AND TOLERANCES PER 0.25 _{9X} 0.15 ASME Y14.5M, 1994. D. PRESENCE OF CENTER PAD IS PACKAGE 1.62

图 19. 10-引脚, MicroPak™, 1.6mm宽

0.10M C A B

⊕ 0.10 C

ALL FEATURES

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For current tape and reel specifications, visit Fairchild Semiconductor's online packaging area: http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf.

BOTTOM VIEW

SUPPLIER DEPENDENT. IF PRESENT IT

HAS A BLACK OXIDE FINISH.

E. DRAWING FILENAME: MKT-MAC10Arev5.

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