NB3N51054

3.3 V, Crystal to 100 MHz Quad HCSL/LVDS PCIe Clock Generator

The NB3N51054 is a precision, low phase noise clock generator that supports PCI Express requirements. The device accepts a 25 MHz fundamental mode parallel resonant crystal or a 25 MHz reference clock signal and generates four differential HCSL/LVDS outputs (See Figure 7 for LVDS interface) at 100 MHz clock frequency with maximum skew of 40 ps. Through I^2C interface, NB3N51054 provides selectable spread spectrum options of −0.35% and −0.5% for applications demanding low Electromagnetic Interface (EMI) as well as optimum performance with no spread option. The I^2C interface further enables control of each output and they can be enabled/disabled individually.

Features

- Uses 25 MHz Fundamental Crystal or Reference Clock Input
- Four Low Skew HCSL or LVDS Outputs
- I^2C Support with Read Back Capability
- Spread of −0.35%, −0.5% and No Spread
- Individual Output Enable/Disable Control through I^2C
- PCIe Gen 1, Gen 2, Gen 3, Gen 4 Compliant
- Typical Phase Jitter @ 100 MHz (Integrated 12 kHz to 20 MHz): 0.5 ps
- Typical Cycle−Cycle Jitter @ 100 MHz (10k cycles): 20 ps
- Phase Noise @ 100 MHz:

Offset	Noise Power
100 Hz	−104 dBc/Hz
1 kHz	−121 dBc/Hz
10 kHz	−131 dBc/Hz
100 kHz	−136 dBc/Hz
1 MHz	−140 dBc/Hz
10 MHz	−155 dBc/Hz

- Operating Power Supply: 3.3 V ± 5%
- Industrial Temperature Range: −40°C to 85°C
- Functionally Compatible with ICS841S104I with enhanced performance
- These are Pb−Free Devices

Application

- Networking
- Consumer
- Computing and Peripherals
- Industrial Equipment
- PCIe Clock Generation Gen 1, Gen 2, Gen 3 and Gen 4

End Products

- Switch and Router
- Set Top Box, LCD TV
- Servers, Desktop Computers
- Automated Test Equipment

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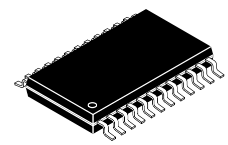
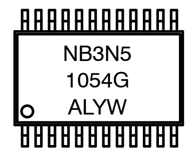


TSSOP−24
CASE 948H

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

BLOCK DIAGRAM

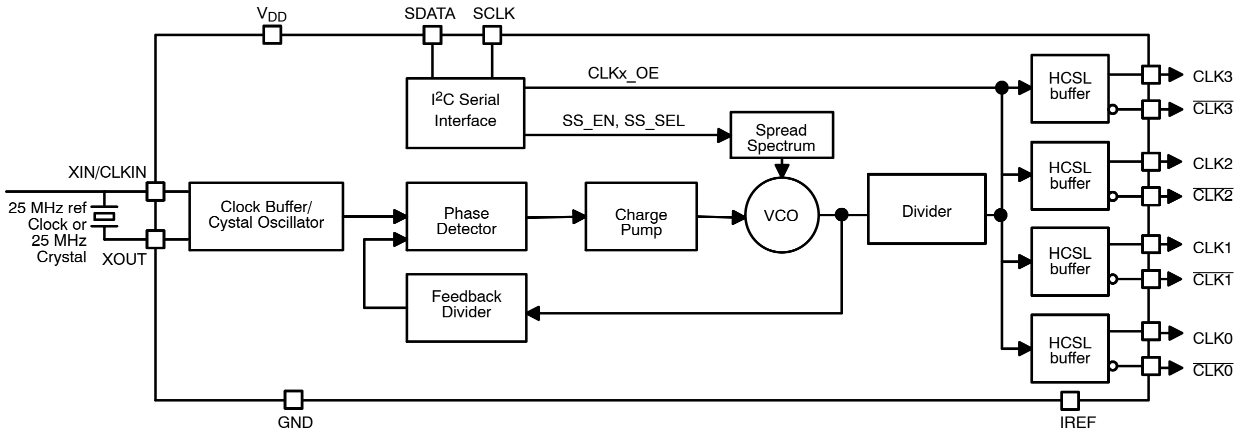


Figure 1. Block Diagram

PIN CONFIGURATION

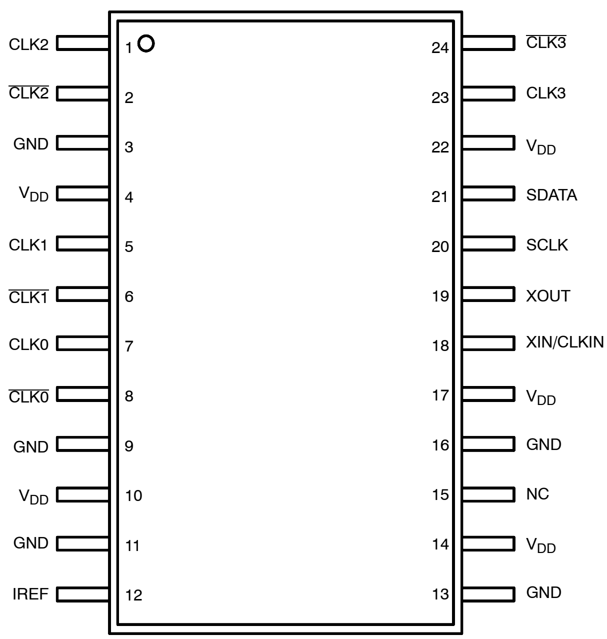


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	CLK2	HCSL or LVDS output	Noninverted clock output. (For LVDS levels see Figure 4)
2	$\overline{CLK2}$	HCSL or LVDS output	Inverted clock output. (For LVDS levels see Figure 4)
3	GND	Ground	Power supply ground 0 V. This pin provides GND return path for the device.
4	V_{DD}	Power	Positive supply voltage pin connected to +3.3 V typical supply voltage.
5	CLK1	HCSL or LVDS output	Noninverted clock output. (For LVDS levels see Figure 4)
6	$\overline{CLK1}$	HCSL or LVDS output	Inverted clock output. (For LVDS levels see Figure 4)
7	CLK0	HCSL or LVDS output	Noninverted clock output. (For LVDS levels see Figure 4)
8	$\overline{CLK0}$	HCSL or LVDS output	Inverted clock output. (For LVDS levels see Figure 4)
9	GND	Ground	Power supply ground 0 V. This pin provides GND return path for the device.
10	V_{DD}	Power	Positive supply voltage pin connected to +3.3 V typical supply voltage.
11	GND	Ground	Power supply ground 0 V. This pin provides GND return path for the device.
12	IREF	Output	Output current reference pin. Connect to precision resistor (typical 475 Ω) to set internal current reference
13	GND	Ground	Power supply ground 0 V. This pin provides GND return path for the device.
14	V_{DD}	Power	Positive supply voltage pin connected to +3.3 V typical supply voltage.
15	NC	NC	No Connect
16	GND	Ground	Power supply ground 0 V. This pin provides GND return path for the device.
17	V_{DD}	Power	Positive supply voltage pin connected to +3.3 V typical supply voltage.
18	XIN / CLKIN	Input	Crystal or Clock input. Connect to 25 MHz crystal OR 25 MHz single−ended reference clock input.
19	XOUT	Input	Crystal input. Connect to 25 MHz crystal or float this pin while using reference clock.
20	SDATA	Input/ Output	I^2C compatible data. Internal pull−up resistors
21	SCLK	Input	I^2C compatible clock. Internal pull−up resistors
22	V_{DD}	Power	Positive supply voltage pin connected to +3.3 V typical supply voltage.
23	CLK3	HCSL or LVDS output	Noninverted clock output. (For LVDS levels see Figure 4)
24	$\overline{CLK3}$	HCSL or LVDS output	Inverted clock output. (For LVDS levels see Figure 4)

Recommended Crystal Parameters

Crystal	Fundamental AT−Cut
Frequency	25 MHz
Load Capacitance	16−20 pF
Shunt Capacitance, C0	7 pF Max
Equivalent Series Resistance	50 Ω Max
Initial Accuracy at 25 °C	±20 ppm
Temperature Stability	±30 ppm
Aging	±20 ppm

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two−signal I^2C serial interface is provided. All the clock outputs can be individually enabled or disabled in a glitch free manner though this serial data interface. In addition, spread spectrum can be enabled for −0.35% or −0.5% down spread or no spread option can be selected though this interface. The registers associated with the serial interface initialize to their default settings upon power−up.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in Table 2 below.

Table 2. COMMAND CODE DEFINITION

Bit	Description
7	0 = Block read or Block write operation, 1= Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For Block read or Block write operations, these bits should be ‘0000000’.

The block write and block read protocol is outlined in Table 3, while Table 4 outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 3. BLOCK READ AND BLOCK WRITE PROTOCOL

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command code – 8 bit ‘00000000’ stands for block operation	11:18	Command code – 8 bit ‘00000000’ stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 0 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge from master
…	…………	39:46	Data byte from slave – 8 bits
…	Data byte (N−1) – 8 bits	47	Acknowledge from master
…	Acknowledge from slave	48:55	Data byte from slave – 8 bits
…	Data byte N – 8 bits	56	Acknowledge from master
	Acknowledge from slave	…	Data byte N from slave – 8 bits
…	Stop	…	Not Acknowledge from master
		…	Stop

Table 4. BYTE READ AND BYTE WRITE PROTOCOL

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave addresses – 7 bits	2:8	Slave addresses – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command code – 8 bit ‘10000000’ stands for byte operation, bits[1:0] command code represents the offset of the byte to be accessed	11:18	Command code – 8 bit ‘10000000’ stands for byte operation bits[1:0] command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29	Stop	28	Read = 1
		29	Acknowledge from slave
		30:37	Data byte from slave – 8 bits
		38 39	Not Acknowledge from master stop

CONTROL REGISTERS

Table 5. BYTE 0: CONTROL REGISTER 0

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	1	CLK3_OE	CLK3 Output Enable 0 = Disable (Hi–Z) 1 = Enable
5	1	CLK2_OE	CLK2 Output Enable 0 = Disable (Hi–Z) 1 = Enable
4	1	CLK1_OE	CLK1 Output Enable 0 = Disable (Hi–Z) 1 = Enable
3	1	CLK0_OE	CLK0 Output Enable 0 = Disable (Hi–Z) 1 = Enable
2	1	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Table 6. BYTE 1: CONTROLLER REGISTER 1

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Table 7. BYTE 2: CONTROLLER REGISTER 2

Bit	@Pup	Name	Description
7	1	SS_SEL	Spread Spectrum Selection 0 = −0.35%, 1 = −0.5%
6	1	Reserved	Reserved
5	1	Reserved	Reserved
4	0	Reserved	Reserved
3	1	Reserved	Reserved
2	0	SS_EN	Spread Spectrum Enable 0 = Spread Off, 1 = Spread On
1	1	Reserved	Reserved
0	0	Reserved	Reserved

Table 8. BYTE 3: CONTROLLER REGISTER 3

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Table 9. BYTE 4: CONTROLLER REGISTER 4

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Table 10. BYTE 5: CONTROLLER REGISTER 5

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Table 11. BYTE 6: CONTROLLER REGISTER 6

Bit	@Pup	Name	Description
7	0	TEST_SEL	Reserved
6	0	TEST_MODE	Reserved
5	0	Reserved	Reserved
4	1	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	1	Reserved	Reserved
0	1	Reserved	Reserved

Table 12. BYTE 7: CONTROLLER REGISTER 7

Bit	@Pup	Name	Description
7	0	Rev Code [3]	Revision Code (MSB)
6	0	Rev Code [2]	Revision Code
5	0	Rev Code [1]	Revision Code
4	1	Rev Code [0]	Revision Code (LSB)
3	1	Vendor ID [3]	Vendor ID (MSB)
2	1	Vendor ID [2]	Vendor ID
1	1	Vendor ID [1]	Vendor ID
0	1	Vendor ID [0]	Vendor ID (LSB)

Table 13. ATTRIBUTES

Characteristic		Value
Internal Pull−up Resistor (SCLK, SDATA)		50 kΩ
ESD Protection	Human Body Model	2 kV
Moisture Sensitivity, Indefinite Time Out of Dray Pack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		132,000
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 14. ABSOLUTE MAXIMUM RATING (Note 2)

Symbol	Parameter	Rating	Unit
V_{DD}	Positive power supply with respect to GND	+4.6	V
V_I	Input Voltage with respect to device GND	−0.5 V to V_{DD} + 0.5 V	V
T_A	Operating Temperature Range	−40 to +85	°C
T_{STG}	Storage temperature	−65 to +150	°C
T_{SOL}	Max. Soldering Temperature (10 sec)	265	°C
θ_{JA}	Thermal Resistance (Junction−to−ambient) 0 lfpm (Note 3) 500 lfpm	65 57	°C/W
θ_{JC}	Thermal Resistance (Junction−to−case)	50	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 15. DC ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3 V ± 5%, GND = 0 V, T_A = −40°C to 85°C, Note 4)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Power Supply Voltage	3.135	3.3	3.465	V
I_{DD}	Power Supply Current, spread OFF, all outputs ON		125	130	mA
I_{OFF}	Power Supply Current when all outputs are set OFF through I^2C, spread OFF			50	mA
V_{IH}	Input HIGH Voltage (XIN/CLKIN)	2.0		V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage (XIN/CLKIN)	GND − 0.3		0.8	V
I_{IH}	Input HIGH Current (SCLK/SDATA), V_{DD} = V_{IN} = 3.465 V			10	μA
I_{IL}	Input LOW Current (SCLK/SDATA), V_{DD} = 3.465 V, V_{IN} = 0 V	−150			μA
V_{OH}	Output HIGH Voltage for HCSL Output (Note 5)	660		850	mV
V_{OL}	Output LOW Voltage for HCSL Output (Note 5)	−150			mV
V_{CROSS}	Crossing Voltage Magnitude (Absolute) for HCSL Output (Notes 5, 6, 7)	250		550	mV
ΔV_{CROSS}	Change in Magnitude of V_{CROSS} for HCSL Output (Notes 5, 6, 8)			150	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. Measurement taken with outputs terminated with R_S = 33.2 Ω, R_L = 49.9 Ω, with test load capacitance of 2 pF and current biasing resistor set at R_{REF} = 475 Ω. See Figure 6. Guaranteed by characterization.
5. Measurement taken from single-ended waveform
6. Measured at crossing point where the instantaneous voltage value of the rising edge of CLKx+ equals the falling edge of CLKx-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltage of rising CLKx+ and falling CLKx-. This is maximum allowed variance in the V_{CROSS} for any particular system.

Table 16. AC ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3 V ± 5%, GND = 0 V, T_A = −40°C to 85°C, Note 9)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CLKIN}	Clock/ Crystal Input Frequency			25		MHz
f_{CLKOUT}	Output Frequency			100		MHz
Φ_{NOISE}	Phase Noise Performance	@ 100 Hz offset from carrier		−104		dBc/Hz
		@ 1 kHz offset from carrier		−121		
		@ 10 kHz offset from carrier		−131		
		@ 100 kHz offset from carrier		−136		
		@ 1 MHz offset from carrier		−140		
		@ 10 MHz offset from carrier		−155		
$t_{jit(\phi)}$	RMS Phase Jitter	RMS Phase Jitter, f_{CLKIN} = 25 MHz Crystal, f_{CLKOUT} = 100 MHz, Integration Range: 12 kHz − 20 MHz		0.5		ps
t_{JITTER}	Peak Cycle−to−Cycle Jitter	Measured over 10000 cycles		20		ps
t_F / t_R	Rise / Fall Time	Measured differentially between −150 mV to +150 mV	0.6		4.0	V/ns
Δt_F / t_R	Output Rise/ Fall Time Variation	Measured Single−ended			125	ps
f_{MOD}	Spread Spectrum Modulation Frequency		30	31.5	33.33	kHz
SSC_{RED}	Spectral Reduction, 3rd Harmonic	Measured with frequency spread of −0.5%		−10		dB
V_{MAX}	Absolute Maximum Voltage, measured single ended including undershoot				1150	mV
V_{MIN}	Absolute Minimum Voltage, measured single ended including undershoot		−300			mV
t_{SKEW}	Within device Output to Output Skew	All outputs			40	ps
t_{SPREAD}	Spread Spectrum Transition Time	Stabilization Time After Spread Spectrum Changes			50	μs
t_{DC}	Output Clock Duty Cycle	Measured at cross point	45	50	55	%
t_{PLL}	PLL Lock Time				50	ms
t_{PU}	Stabilization Time from Power−up	V_{DD} = 3.3 V		3.0		ms

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

9. Measurement taken from differential output on single−ended channel terminated with R_S = 33.2 Ω , R_L = 49.9 Ω , with test load capacitance of 2 pF and current biasing resistor set at R_{REF} = 475 Ω . See Figure 6. Guaranteed by characterization.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 17. AC ELECTRICAL CHARACTERISTICS – PCI EXPRESS JITTER SPECIFICATIONS
V_{DD} = 3.3 V ± 5%, T_A = −40°C to 85°C

Symbol	Parameter	Test Condition	Spread Condition	Min	Typ	Max	PCIe Industry Spec	Unit
tj (PCIe Gen 1)	Phase Jitter Peak−to−Peak (Notes 11 and 14)	f_{CLKIN} = 25 MHz Crystal, f_{CLKOUT} = 100 MHz Input Evaluation Band: 0 Hz − Nyquist (clock frequency/2)	SSOFF		10	20	86	ps
			SSON (−0.5%)		19	28		
tREFCLK_HF_RMS (PCIe Gen 2)	Phase Jitter RMS (Notes 12 and 14)	f_{CLKIN} = 25 MHz Crystal, f_{CLKOUT} = 100 MHz Input High Band: 1.5 MHz − Nyquist (clock frequency/2)	SSOFF		1.0	1.8	3.1	ps
			SSON (−0.5%)		1.1	1.9		
tREFCLK_LF_RMS (PCIe Gen 2)	Phase Jitter RMS (Notes 12 and 14)	f_{CLKIN} = 25 MHz Crystal, f_{CLKOUT} = 100 MHz Input Low Band: 10 kHz − 1.5 MHz	SSOFF		0.1	0.15	3.0	ps
			SSON (−0.5%)		0.8	1.1		
tREFCLK_RMS (PCIe Gen 3)	Phase Jitter RMS (Notes 13 and 14)	f_{CLKIN} = 25 MHz Crystal, f_{CLKOUT} = 100 MHz Input Evaluation Band: 0 Hz Nyquist (clock frequency/2)	SSOFF		0.35	0.7	1.0	ps
			SSON (−0.5%)		0.55	0.8		
tREFCLK_RMS (PCIe Gen 4)	Phase Jitter RMS (Notes 13 and 14)	f = 100 MHz, 25 MHz Crystal Input Evaluation Band: 0 Hz − Nyquist (clock frequency/2)	SSOFF		0.35	0.5	0.5	ps

10. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
11. Peak−to−Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86 ps peak−to−peak for a sample size of 10^6 clock periods.
12. RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1 ps RMS for tREFCLK_HF_RMS (High Band) and 3.0 ps RMS for tREFCLK_LF_RMS (Low Band).
13. RMS jitter after applying system transfer function for the common clock architecture.
14. Measurement taken from differential output on single−ended channel terminated with R_S = 33.2 Ω , R_L = 49.9 Ω , with test load capacitance of 2 pF and current biasing resistor set at R_{REF} = 475 Ω . See Figure 6. This parameter is guaranteed by characterization. Not tested in production

PHASE NOISE

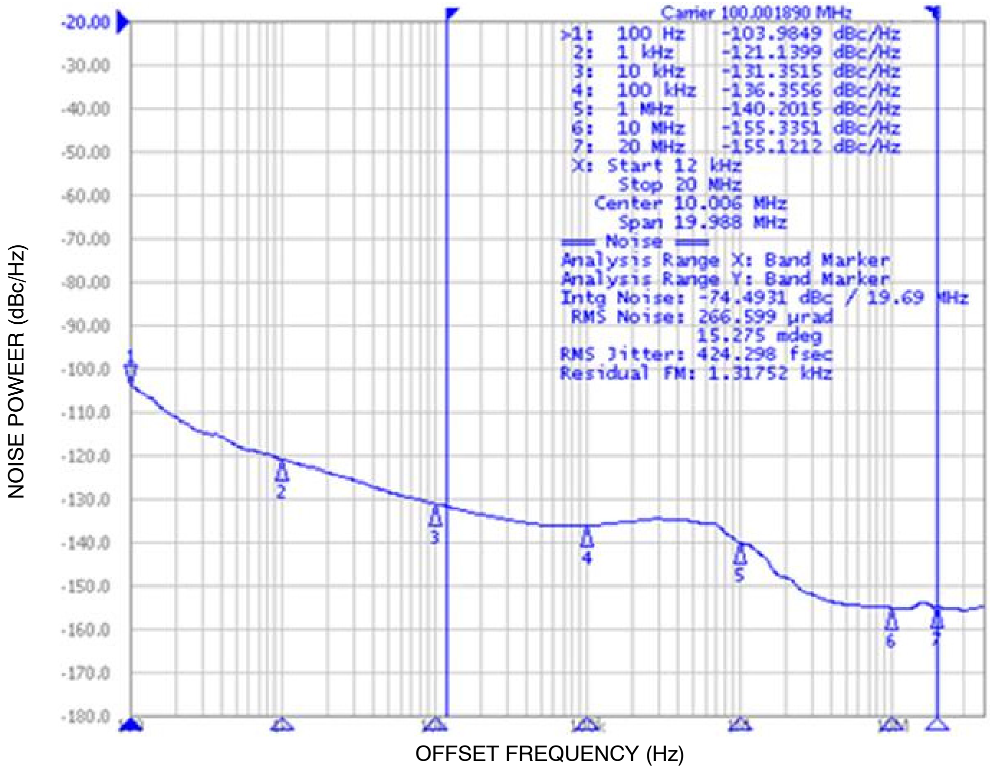


Figure 3. Typical Phase Noise Plot at 100 MHz (f_{CLKIN} = 25 MHz Crystal , f_{CLKOUT} = 100 MHz, RMS Phase Jitter = 424 fs for Integration Range of 12 kHz to 20 MHz, Output Termination = HCSL type)

APPLICATION INFORMATION

Crystal Input Interface

Figure 4 shows the NB3N51044 device crystal oscillator interface using a typical parallel resonant crystal. The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors, C_1 and C_2, need to consider the stray capacitances of the board and are used to match the nominally required crystal load capacitance C_L. A parallel crystal with loading capacitance C_L = 18 pF would use C_1 = 26 pF and C_2 = 26 pF as nominal values, assuming approximately 2 pF of stray capacitance per trace and approximately 8 pF of internal capacitance.

$C_L = (C_1 + C_{stray} + C_{in}) / 2; C_1 = C_2$

The frequency accuracy and duty cycle skew can be fine-tuned by adjusting the C_1 and C_2 values. For example, increasing the C_1 and C_2 values will reduce the operational frequency.

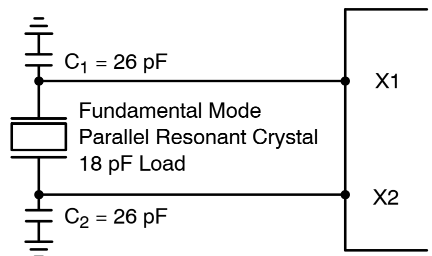


Figure 4. Crystal Interface Loading

Power Supply Filter

In order to isolate the NB3N51044 from system power supply, noise decoupling is required. The 10 μF and a 0.1 μF cap from supply pins to GND decoupling capacitor has to be connected between V_{DD} (pins 3, 9, 11, 13 and 16) and GND (pins 4, 10, 14, 17 and 22). It is recommended to place decoupling capacitors as close as possible to the device to minimize lead inductance.

Termination

The output buffer structure is shown in the Figure 5.

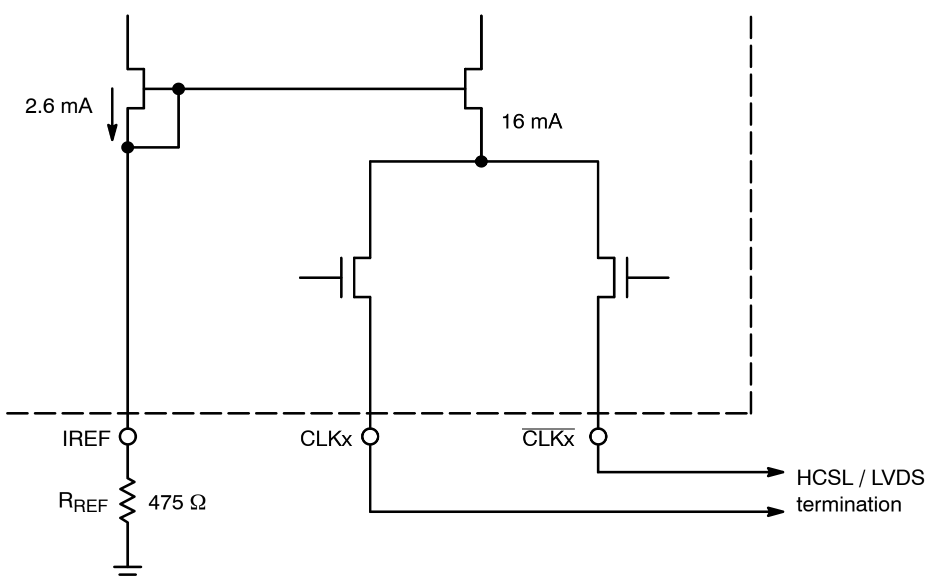


Figure 5. Simplified Output Structure

The outputs can be terminated to drive HCSL receiver (see Figure 6) or LVDS receiver (see Figure 7). HCSL output interface requires 49.9 Ω termination resistors to GND for generating the output levels. LVDS output interface may not require the 100 Ω near the LVDS receiver if the receiver has internal 100 Ω termination. An optional series resistor R_L may be connected to reduce the overshoots in case of impedance mismatch.

HCSL INTERFACE

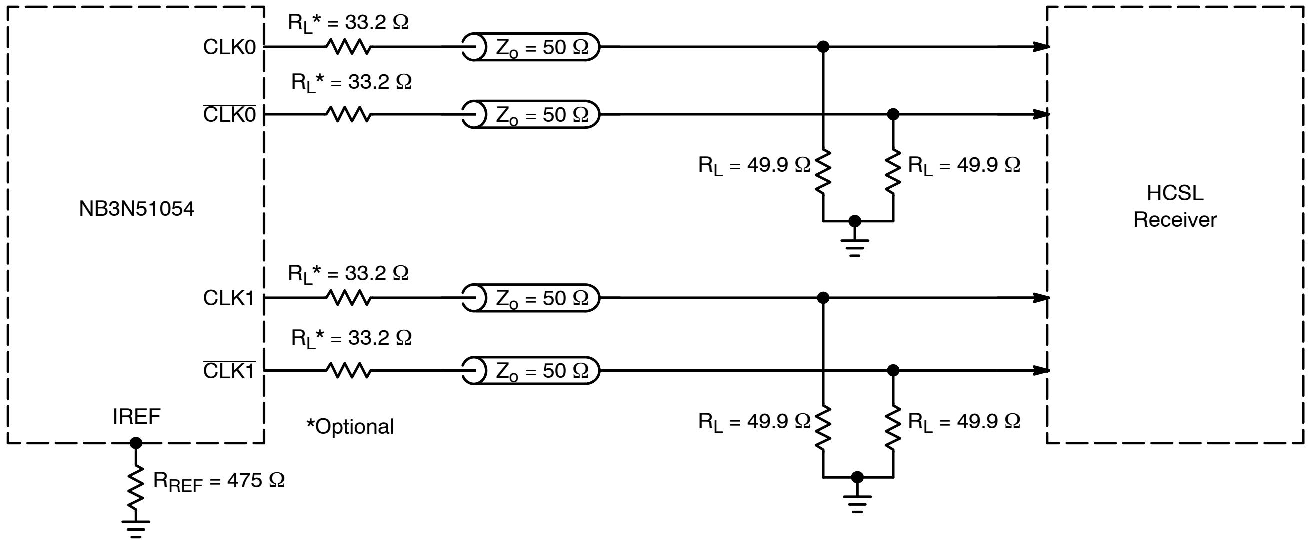


Figure 6. Typical Termination for HCSL Output Driver and Device Evaluation

LVDS COMPATIBLE INTERFACE

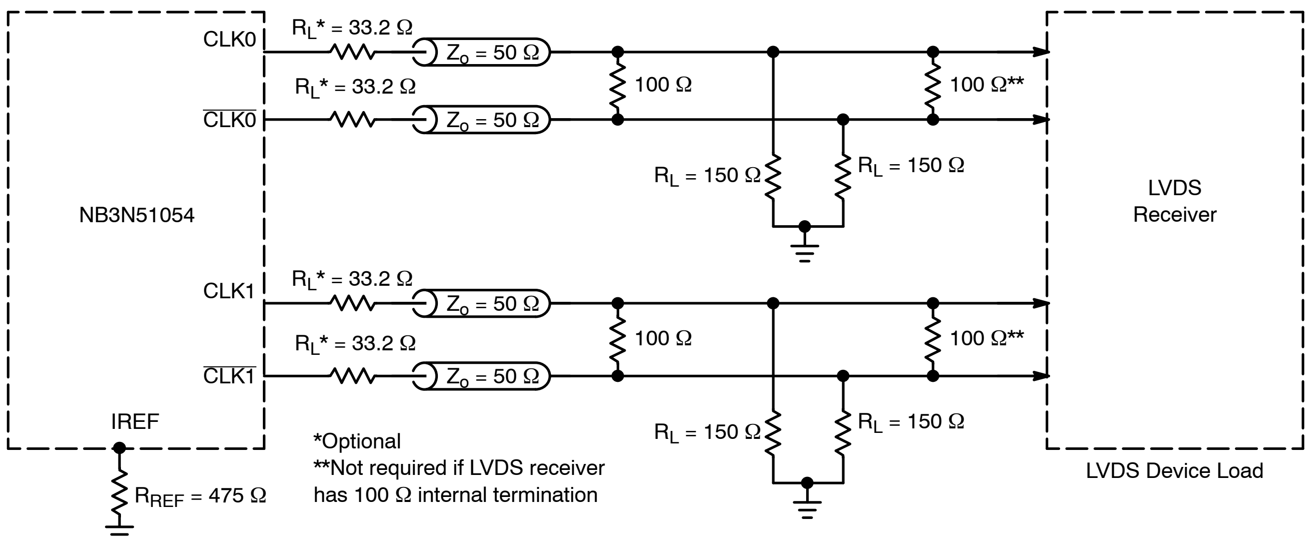


Figure 7. Typical Termination for LVDS Device Load

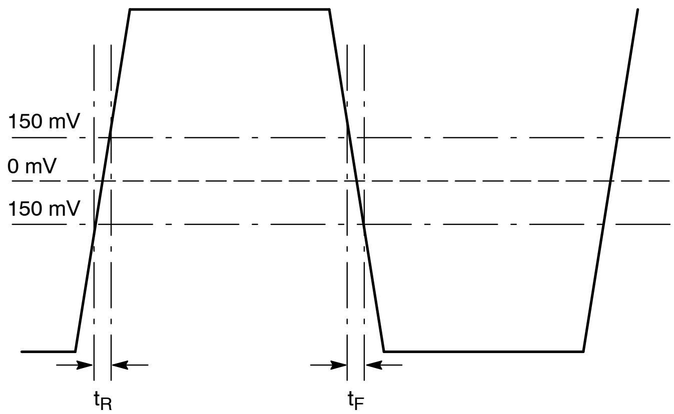


Figure 8. HCSL Differential Measurement of t_R/t_F

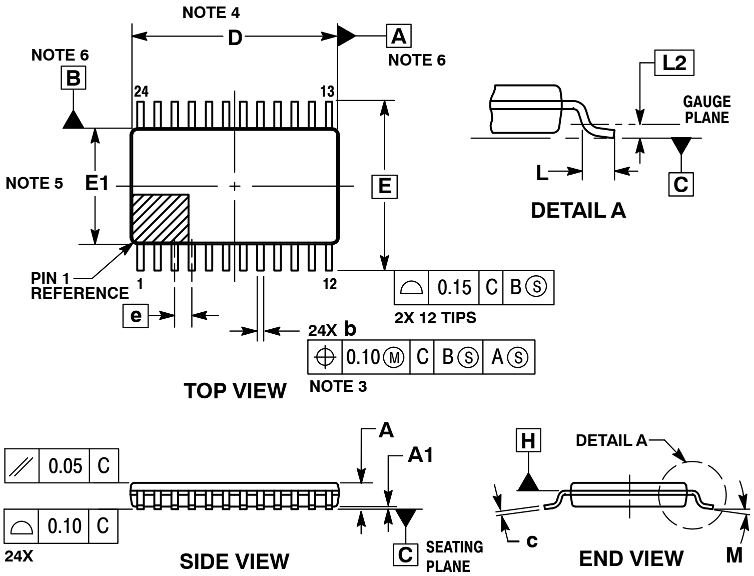
ORDERING INFORMATION

Device	Temperature	Package	Shipping†
NB3N51054DTG	−40°C to 85°C	TSSOP−24 (Pb−Free)	96 Units / Rail
NB3N51054DTR2G	−40°C to 85°C	TSSOP−24 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

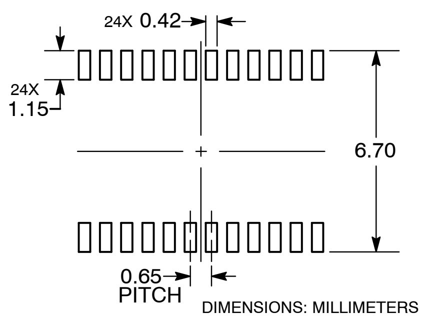
TSSOP24 7.8x4.4, 0.65P
CASE 948H
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BSC	
E1	4.30	4.50
e	0.65 BSC	
L	0.50	0.75
L2	0.25 BSC	
M	0°	8°

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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