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FPF2496

IntelliMAX™ 集成可调节限流控制，提供过压保护、过流保护的 28 V 负载开关

特性

- V_{IN} : 3.5 V~5.5 V
- 28 V 绝对额定值 (在 V_{IN} 时)
- 电流能力: 2.5 A
- 可调节限流: (典型值) 0.1 A~2.5 A, 10% 的精度
- R_{ON} : 最大值: 100 m Ω (5 V_{IN} 和1A I_{OUT})
- 输入 OVP: 最小值 = 5.6 V, 典型值 = 5.8 V, 最大值 = 6 V
- 断开 (Off) 状态期间无输出放电
- FLAGB 上的漏极开路过压保护 (OVP)
- 热关断
- 欠压锁定 (UVLO)
- 精确反向电流阻隔 (TRCB)
- 逻辑 CMOS IO 符合 GPIO 接口的 JESD76 标准以及相关的电源要求
- 静电放电保护:
 - 人体模型: >5.0 kV
 - 元件充电模型: >2.5 kV
 - IEC 61000-4-2 空气放电: >15 kV
 - IEC 61000-4-2 接触放电: >8 kV

说明

FPF2496 先进负载管理开关的目标应用要求高度集成的解决方案。它将断开通过 DC 电源 (< 6 V) 供电且具有严格关断状态电流目标和高负载电容 (< 100 μ F) 的负载。FPF2496 由压摆率控制的低阻抗 MOSFET 开关 (最大值 100 m Ω) 和集成式模拟功能组成。压摆率控制的打开特性可防止电源轨上产生浪涌电流及过大的电压降。FPF2496 具有过压保护和过温保护。

FPF2496 具有精确反向电流阻隔 (TRCB) 功能, 可阻止导通和关断状态期间从 V_{OUT} 到 V_{IN} 的不需要的反向电流。极低的关断状态漏电流 (< 2 μ A 最大值) 有助于符合待机功率要求。输入工作电压范围为 3.5 V 至 5.5 V_{DC} , 可满足消费电子、光学、医疗、存储、便携式和工业器件电源管理等广泛应用的需求。开关控制是通过能够直接连接低压控制信号/通用输入/输出 (GPIO) 的逻辑输入 (高电平有效) 来管理的, 无需外部下拉电阻。

该器件采用先进的、完全符合“绿色”标准的 1.25 mm x 1.25 mm 晶圆级芯片尺寸封装 (WLCSP)。

应用

- 智能手机、平板电脑
- 存储、数码单反相机和便携式设备

订购信息

器件编号	工作温度范围	封装	顶标
FPF2496UCX	-40 至 85°C	1.25 mm x 1.25 mm, 晶圆级芯片尺寸封装 (WLCSP)	TJ

应用框图

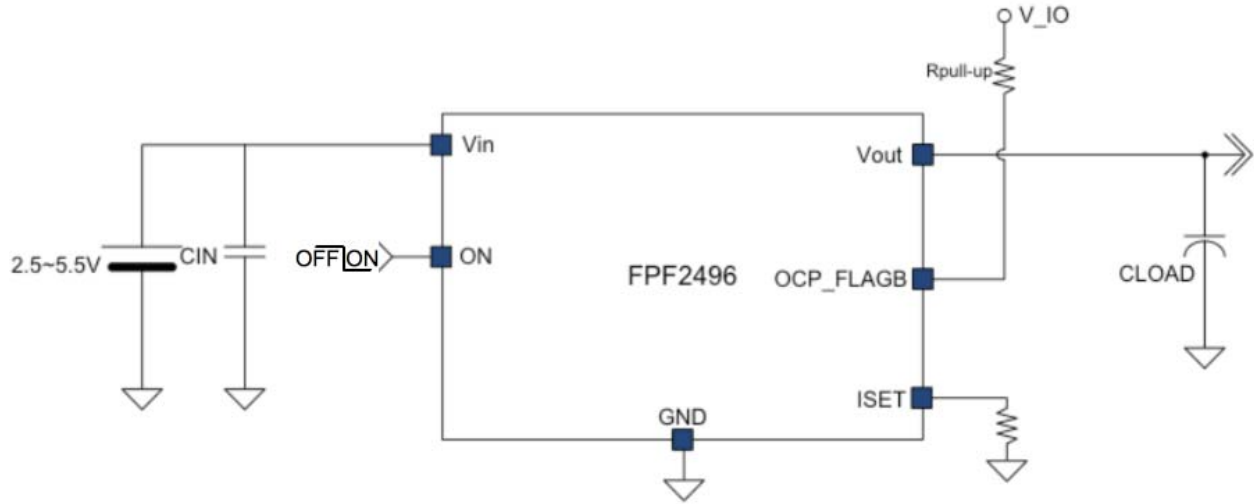


图 1. 典型应用

注意:

1. 推荐使用 C_{IN} 和 C_{OUT} 电容以提高器件稳定性。

框图

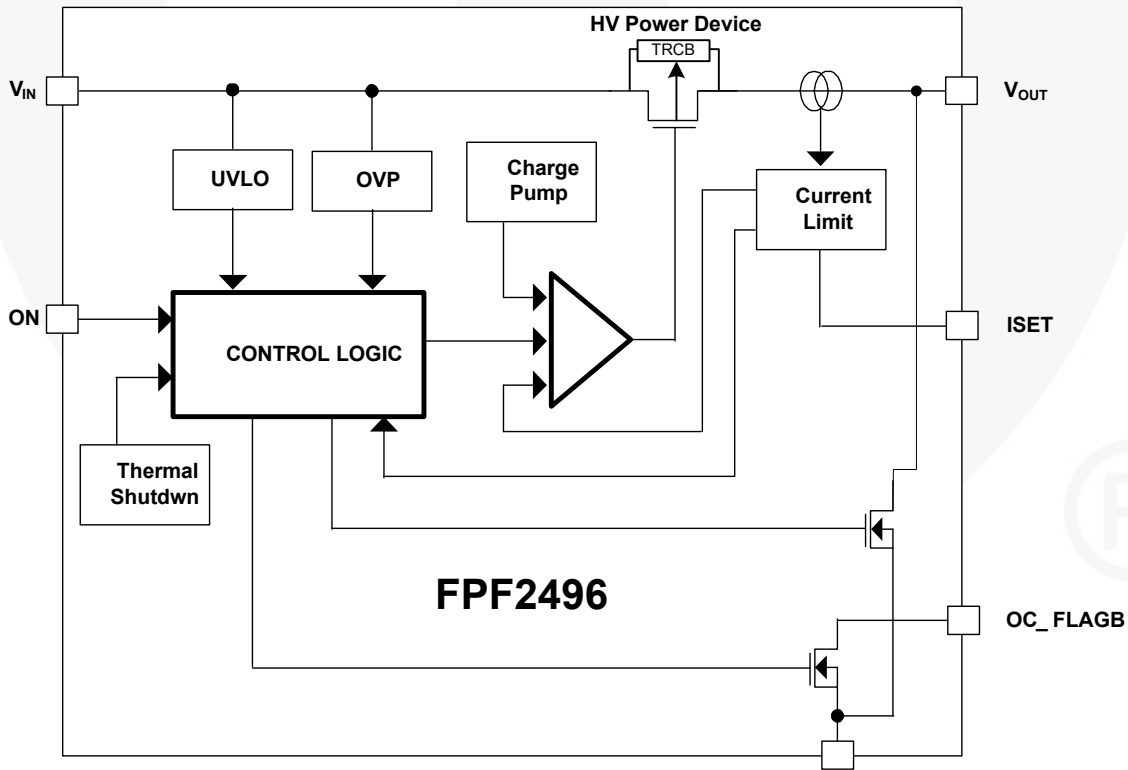


图 2. 功能框图

引脚布局

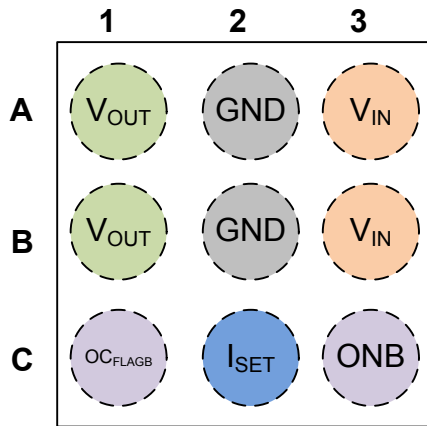


图 3. 引脚分配 (顶视图/俯视图)

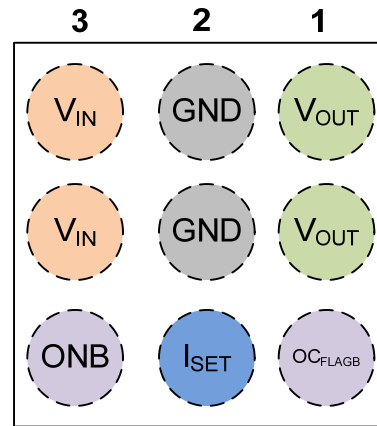


图 4. 引脚布局 (底视图)

引脚描述

引脚号	名称	说明		
A1, B1	V _{OUT}	开关输出		
A3, B3	V _{IN}	电源输入：电源开关的输出		
A2	GND	接地（设备接地）		
B2				
C3	ONB	导通/判断控制输入：低电平有效；GPIO 兼容	逻辑高电平	禁用开关
			逻辑低电平	启用开关
C1	OC _{FLAGB}	故障输出：低电平有效，表示输入过流的开漏输出。需要外部上拉电阻至 V _{CC} 。		
C2	I _{SET}	电流限值设置输入：I _{SET} 与地之间的电阻设置开关的限流值。		

绝对最大额定值

应力超过绝对最大额定值，可能会损坏器件。在超出推荐的工作条件的情况下，该器件可能无法正常工作，所以不建议让器件在这些条件下长期工作。此外，长期在高于推荐的工作条件下工作，会影响器件的可靠性。绝对最大额定值仅是应力规格值。

符号	参数		最小值	最大值	单位
V _{PIN}	V _{IN} 至 GND 接地, V _{IN} 至 V _{OUT}		-0.3	28.0	V
	ONB、V _{OUT} 、FLAGB、I _{SET} 至 GND		-0.3	6.0	
I _{SW}	连续开关电流最大值			2.75	A
t _{PD}	总功率损耗（在 T _A =25°C 时）			1.0	W
T _J	工作结温		-40	+150	°C
T _{STG}	存储结温		-65	+150	°C
Θ _{JA}	结至环境热阻（每平方英寸焊盘为 2 oz 铜片）			95 ⁽²⁾	°C/W
				110 ⁽³⁾	
ESD	静电放电能力	人体模型, ANSI/ESDA/JEDEC JS-001-2012	5.0		kV
		元件充电模型, JESD22-C101	2.5		
	IEC61000-4-2 系统级	空气放电 (V _{IN} 、V _{ON} 、V _{OUT} 到 GND)	15		
		接触放电 (V _{IN} 、V _{ON} 、V _{OUT} 到 GND)	8		

注意：

2. 采用 2S2P JEDEC 标准测量。PCB。
3. 使用 2S2P JEDEC PCB 冷板方法测得。

推荐工作条件

推荐的操作条件表明了器件的真实工作条件。指定推荐的工作条件，以确保器件的最佳性能达到数据表中的规格。飞兆半导体建议不要超过推荐工作条件，也不能按照绝对最大额定值进行设计。

符号	参数	最小值	最大值	单位
V _{IN}	电源电压	3.5	5.5	V
T _A	工作环境温度	-40	85	°C

电气特性

$V_{IN}=3.5$ 至 5.5 V, $T_A=-40$ 至 $+85^\circ\text{C}$; 在 $V_{IN}=5$ V 和 $T_A=25^\circ\text{C}$ 时的典型值, 除非另有说明。

符号	参数	条件	最小值	典型值	最大值	单位
基本工作						
V_{IN}	输入电压		3.5		5.5	V
$I_{Q(OFF)}$	关断电源电流	$V_{ON}=\text{接地}, V_{OUT}=\text{开路}$		1	2	μA
$I_{SD(OFF)}$	关断电流	$V_{IN}=5.5$ V, $V_{OUT}=0$ V, $V_{ON}=\text{接地}$		0.1	4.0	μA
I_Q	静态电流	$I_{OUT}=0$ mA		65	100	μA
R_{ON}	导通电阻	$V_{IN}=5.0$ V, $I_{OUT}=1$ A		70	100	m Ω
		$V_{IN}=3.7$ V, $I_{OUT}=1$ A		75	105	
V_{IH}	ONB 输入逻辑高电压	$V_{IN}=3.5$ V 至 5.5 V	1.15			V
V_{IL}	ONB 输入逻辑低电平	$V_{IN}=3.5$ V 至 5.5 V			0.65	V
V_{IL_FLAG}	FLAGB 输出逻辑低电压	$V_{IN}=5$ V, $I_{SINK}=10$ mA		0.1	0.2	V
		$V_{IN}=3.5$ V, $I_{SINK}=10$ mA		0.15	0.30	
I_{FLAGB_LK}	FLAGB 输出高漏电流	$V_{IN}=5$ V, 开关导通			1	μA
I_{ON}	ONB 输入漏电流	0 V 至 V_{IN}			1.0	μA
R_{ON_PD}	ONB 引脚上的下拉电阻	$V_{IN}=3.5\sim 5.5$ V, $V_{ON}=\text{HIGH}$, $T_A=-40$ 至 85°C		14		M Ω
RPD	输出放电 R_{PULL_DOWN}	$V_{IN}=3.5$ V, $V_{ON}=0$ V, $I_{FORCE}=20$ mA, $T_A=-40$ 至 85°C		100		Ω
过压保护						
V_{OVP_TRIP}	输入 OVP 锁定	V_{IN} 上升阈值	5.60	5.80	6.00	V
		V_{IN} 下降阈值		5.50		
V_{OVP_HYS}	输入 OVP 滞回			0.3		V
t_{OVP}	响应时间	$I_{OUT}=0.5$ A, $C_L=1$ μF , $T_A=25^\circ\text{C}$, $V_{IN}=5.5$ V 至 6.0 V	1			μs
过流保护						
I_{LIM}	限流	$V_{IN}=5$ V, $R_{SET}=2100$ Ω , $V_{OUT}>1.68$ V, 精度为 10%	450	500	550	mA
		$V_{IN}=5$ V, $R_{SET}=1070$ Ω , $V_{OUT}>1.68$ V, 精度为 10%	900	1000	1100	
V_{UVLO}	欠压锁定	V_{IN} 升高		3.2		V
		V_{IN} 降低		3.0		
V_{UVLO_HYS}	UVLO 滞环			200		mV
V_{T_RCB}	RCB 保护跳闸点	$V_{OUT} - V_{IN}$		50		mV
V_{R_RCB}	RCB 保护脱扣点	$V_{IN} - V_{OUT}$		50		mV

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电气特性 (续)

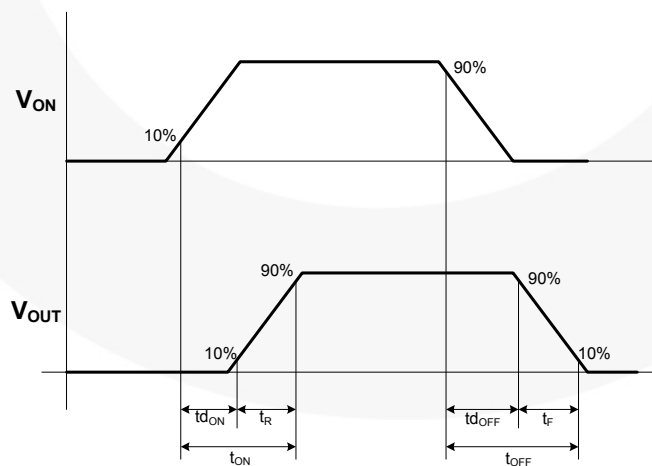
$V_{IN}=3.5$ 至 5.5 V, $T_A=-40$ 至 $+85^\circ\text{C}$; 在 $V_{IN}=5$ V 和 $T_A=25^\circ\text{C}$ 时的典型值, 除非另有说明。

符号	参数	工作条件	最小值	典型值	最大值	单位
V_{RCB_HYS}	RCB 滞环			100		mV
t_{RCB}	默认 RCB 响应时间	$V_{IN}=5$ V, V_{ON} =高电平/低电平		2		μs
I_{RCB}	RCB 电流	$V_{ON}=0$ V, $V_{OUT}=5.5$ V		14		μA
t_{HOCP}	硬过流响应时间	中度过流条件, $I_{OUT} \geq I_{LIM}$, $V_{OUT} \leq 0$ V		6		μs
t_{OCP}	过流响应时间	中度过流条件, $I_{OUT} \geq I_{LIM}$, $V_{OUT} \leq V_{IN}$		7		μs
t_{OC_FLAG}	过流标志响应时间	当标志下拉低电平出现过流时		8		ms
TSD	热关断	关断阈值		150		$^\circ\text{C}$
		从关闭中恢复		130		
		滞回		20		
动态特性						
t_{DON}	导通延迟 ^(4,5)	$V_{IN}=5$ V, $R_L=100$ Ω , $C_L=1$ μF , $T_A=25^\circ\text{C}$		4.39		ms
t_R	V_{OUT} 上升时间 ^(4,5)			7.26		ms
t_{ON}	导通时间 ^(4,7)			11.65		ms
t_{DOFF}	关断延时 ⁽⁵⁾			1.85		ms
t_F	V_{OUT} 下降时间 ⁽⁵⁾			37.60		ms
t_{OFF}	关断时间 ⁽⁷⁾			39.45		ms

注意:

- 该参数通过设计和特性得到保证, 无需生产测试。
- $t_{DON}/t_{DOFF}/t_R/t_F$ 在下列中进行定义图 5。
- $t_{ON}=t_R + t_{DON}$ 。
- $t_{OFF}=t_F + t_{DOFF}$ 。

时序图



其中:

- t_{DON} = 延迟导通时间
- t_R = V_{OUT} 上升时间
- t_{ON} = 导通时间
- t_{DOFF} = 延迟关断时间
- t_F = V_{OUT} 下降时间
- t_{OFF} = 关断时间

图 5. 时序图

操作和应用描述

输入电容

当开关打开变成放电负载电容时，为防止因瞬时浪涌电流造成输入电源电压下降，必须在 V_{IN} 与 GND 引脚之间放置一个电容。可使用较高值的电容 C_{IN} 来降低高电流应用中的电压降。

输出电容

输出电容应放置在 V_{OUT} 和 GND 引脚之间。开关打开时，该电容可防止电路板寄生电感强制将 V_{OUT} 拉到比 GND 低。该电容还可以防止反向浪涌电流产生电压尖峰，在 V_{OUT} 短路的情况下这可能会损坏器件。

故障报告

一旦检测到过流，OC_FLAGB 将被拉到低电平发送故障信号。

电流限制

电流限值可确保通过开关的电流不会超过最大设定值，而对最小值不做限制。通过选择与 ISET 连接的外接电阻，可以调节电流限值。关于选择电阻的更多信息，可在以下章节查询。当负载大于器件设定的最大值时，器件将作为一个恒定电流源，直到热关断。当裸片温度降至阈值温度以下时，器件恢复。

欠压锁定 (UVLO)

当输入电压降至锁定阈值以下时，欠压锁定功能将关闭开关。当 ONB 引脚有效时，输入电压将超过 UVLO 阈值，解除闭锁并打开开关。

反向电流阻断

无论负载开关处于导通还是关断状态，真正的反向电流阻断功能均可阻止输入源电流从输出端流到输入端。

热关断

热关断可防止晶圆内部或外部产生过高温度。过温状态下，开关关闭。当裸片温度降至阈值温度以下时，开关将再次自动打开。

设置电流限制

通过在 ISET 和 GND 引脚之间连接一个外部电阻来设置电流限值。使用表 1 选择电阻。建议电阻容差为 1% 或更低

表 1. 通过 RSET⁽⁸⁾ 设置限流

R _{SET} Ω	最小值 电流 限值 (mA)	典型值 电流 限值 (mA)	电流限值最 大值 (mA)
420	2250	2500	2750
469	2020	2250	2407
528	1800	2000	2200
604	1570	1750	1920
680	1350	1500	1650
866	1125	1250	1375
1070	900	1000	1100
1200	810	900	990
1330	720	800	880
1500	630	700	770
1740	540	600	660
2100	450	500	550
2320	405	450	495
2550	360	400	440
2940	315	350	385
3400	370	300	330
4020	225	250	275
4990	180	200	220
6490	135	150	165
9530	90	100	110

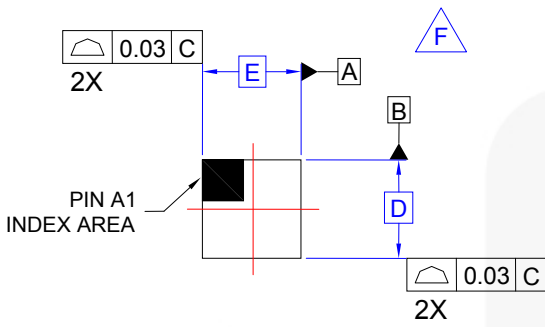
注意：

8. 表值基于 1% 的电阻容差。

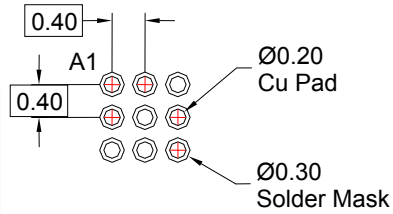
线路板布局

若要实现最佳效果，所有的线路应尽量短。输入和输出电容应尽可能靠近器件放置，从而尽量降低正常和短路工作时的寄生走线电感。 V_{IN} 、 V_{OUT} 和 GND 引脚使用较宽走线，有助于最大限度地降低寄生电效应，以及壳至环境的热阻。

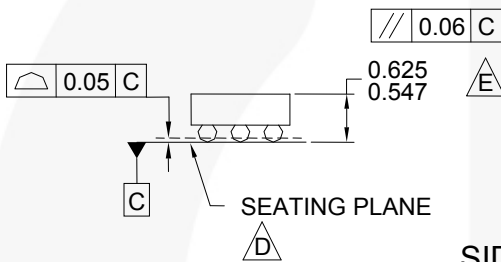
物理尺寸



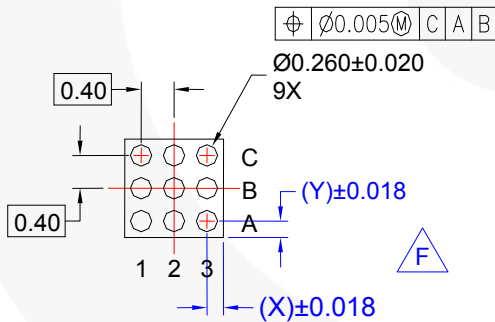
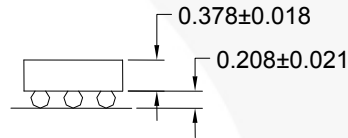
TOP VIEW



LAND PATTERN RECOMMENDATION (NSMD PAD TYPE)



SIDE VIEWS



BOTTOM VIEW

NOTES:

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
- G. DRAWING FILNAME: MKT-UC009ABrev2

产品规格尺寸

产品	D	E	X	Y
FPF2496	1210 μm ±30 μm	1210 μm ±30 μm	205 μm	205 μm

封装图纸作为一项服务，提供给考虑飞兆半导体元件的客户。具体参数可能会有变化，且不会做出相应通知。请注意图纸上的版本和/或日期，并联系飞兆半导体代表核实或获得最新版本。封装规格并不扩大飞兆公司全球范围内的条款与条件，尤其是其中涉及飞兆公司产品保修的部分。

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