NCV7608

Octal Configurable Low/High Side Driver

The NCV7608 integrates 8 output drivers configurable in any combination of high−side, low−side, or H−Bridge configurations. The integrated standard Serial Peripheral Interface (SPI) allows digital control of all output stages and provides diagnostic fault information. In addition, four channels (#5−8) can be PWM controlled via external control input pins.

Integrated clamping circuits (both in high and low−side operational modes), waveshaping, positive and negative transient protection, and dedicated channel pair overtemperature shutdown circuits provide for a wide range of automotive and industrial applications.

Features

- Eight Independent Configurable Drivers
- $R_{DS(on)}$ = 1.2 Ω (typ @25°C)
- SPI Interface for Data Communication
  - 16 Bit Frame Length, Daisy Chain Compatible
  - 3.3 V/5 V Compatible
  - Frame Detection
- PWM Inputs for 4 Outputs
- Ultra−low Standby Current
- Over Current Protection
  - Characterized to AEC Q10X−12−REV A
- High−Side and Low−Side Flyback Protection
- Fault Reporting
- Undervoltage Lockout (VS and V_{CC})
- Overvoltage Shutdown (VS)
- Supports LED Loads
- Supports Cold Cranking Operation Down to 3 V
- Overtemperature Protection
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

Typical Applications

- Automotive
- Industrial
- Relay Drive
- DC Motor Drive
- LED Drive

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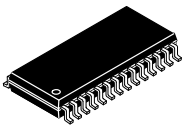
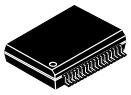
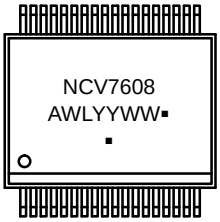
MARKING DIAGRAMs



SOIC−28
DW SUFFIX
CASE 751F



SSOP36 EP
DQ SUFFIX
CASE 940AB



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 25 of this data sheet.

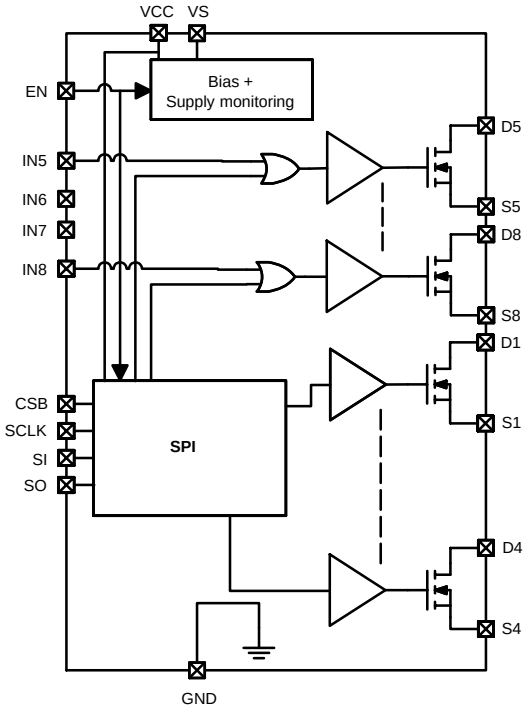


Figure 1. Block Diagram (See Figure 2 for detailed diagram)

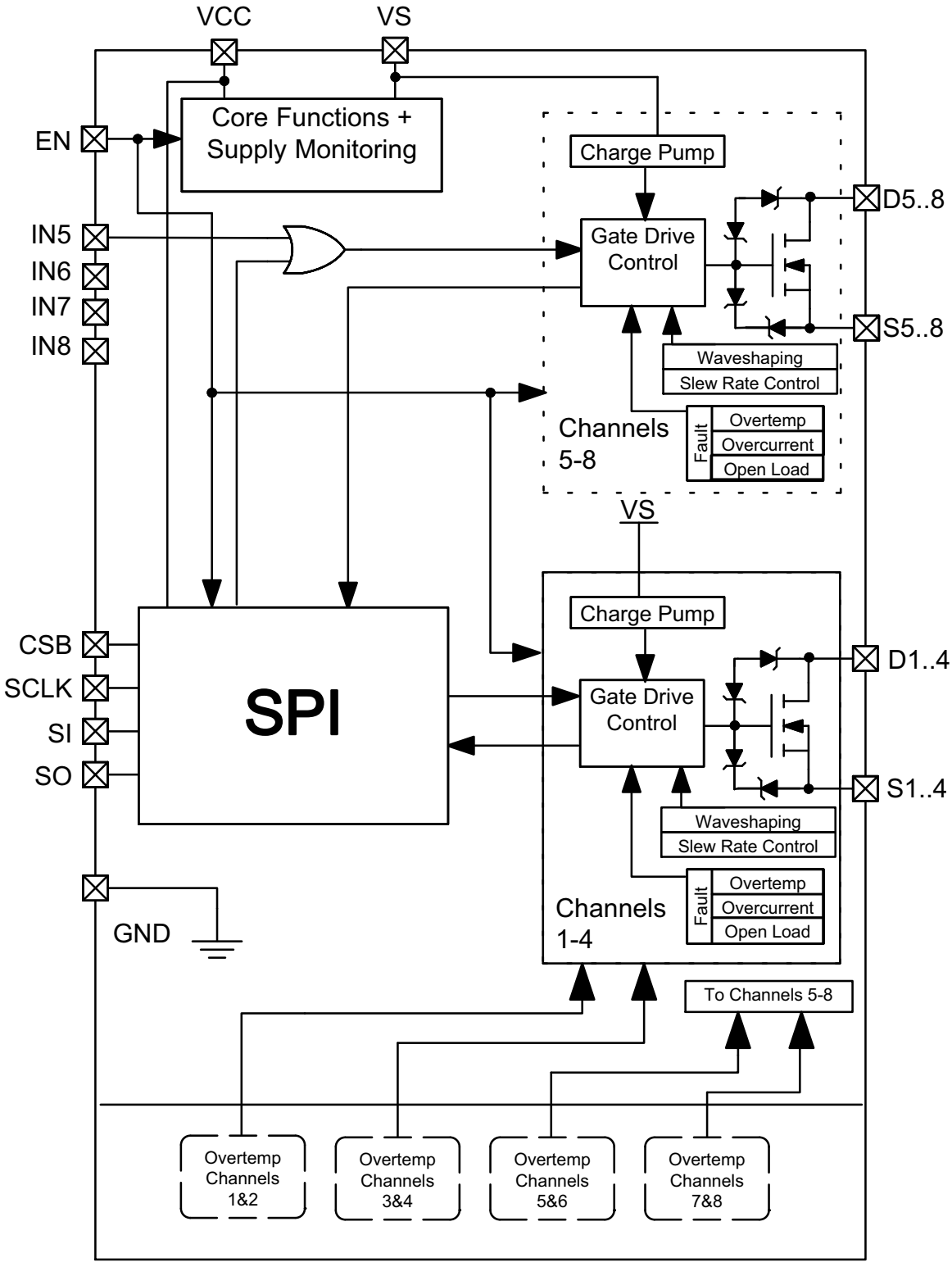


Figure 2. Detailed Block Diagram

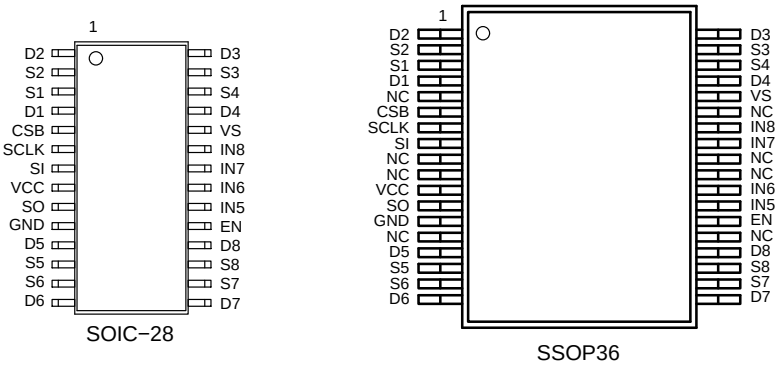


Figure 3. Pin Connections

SOIC−28 PACKAGE PIN DESCRIPTION

Pin #	Symbol	Description
1	D2	Drain of configurable driver #2
2	S2	Source of configurable driver #2
3	S1	Source of configurable driver #1
4	D1	Drain of configurable driver #1
5	CSB	SPI Chip Select “Bar” (100 kΩ pullup resistor to V_{CC})
6	SCLK	SPI clock (100 kΩ pulldown resistor)
7	SI	SPI serial data input (100 kΩ pulldown resistor)
8	VCC	Logic Supply Input Voltage
9	SO	SPI serial data output
10	GND	Ground – Device substrate
11	D5	Drain of configurable driver #5
12	S5	Source of configurable driver #5
13	S6	Source of configurable driver #6
14	D6	Drain of configurable driver #6
15	D7	Drain of configurable driver #7
16	S7	Source of configurable driver #7
17	S8	Source of configurable driver #8
18	D8	Drain of configurable driver #8
19	EN	Global Enable (active high) (100 kΩ pulldown resistor)
20	IN5	PWM control input for driver #5, (active high) (100 kΩ pulldown resistor) Ground if not used.
21	IN6	PWM control input for driver #6, (active high) (100 kΩ pulldown resistor) Ground if not used.
22	IN7	PWM control input for driver #7, (active high) (100 kΩ pulldown resistor) Ground if not used.
23	IN8	PWM control input for driver #8, (active high) (100 kΩ pulldown resistor) Ground if not used.
24	VS	Battery Supply Input Voltage.
25	D4	Drain of configurable driver #4
26	S4	Source of configurable driver #4
27	S3	Source of configurable driver #3
28	D3	Drain of configurable driver #3

SSOP36EP PACKAGE PIN DESCRIPTION

Pin #	Symbol	Description
1	D2	Drain of configurable driver #2
2	S2	Source of configurable driver #2
3	S1	Source of configurable driver #1
4	D1	Drain of configurable driver #1
5	NC	No Connection. This pin should be isolated from any traces or via on the PCB board.
6	CSB	SPI Chip Select “Bar” (100KΩ pullup resistor to VCC)
7	SCLK	SPI clock (100kΩ pulldown resistor)
8	SI	SPI serial data input (100kΩ pulldown resistor)
9	NC	No Connection. This pin should be isolated from any traces or via on the PCB board.
10	NC	No Connection. This pin should be isolated from any traces or via on the PCB board.
11	VCC	Logic Supply Input Voltage
12	SO	SPI serial data output
13	GND	Ground – Device substrate
14	NC	No Connection. This pin should be isolated from any traces or via on the PCB board.
15	D5	Drain of configurable driver #5
16	S5	Source of configurable driver #5
17	S6	Source of configurable driver #6
18	D6	Drain of configurable driver #6
19	D7	Drain of configurable driver #7
20	S7	Source of configurable driver #7
21	S8	Source of configurable driver #8
22	D8	Drain of configurable driver #8
23	NC	No Connection. This pin should be isolated from any traces or via on the PCB board.
24	EN	Global Enable (active high) (100kΩ pulldown resistor)
25	IN5	PWM control input for driver #5, (active high) (100kΩ pulldown resistor) Ground if not used.
26	IN6	PWM control input for driver #6, (active high) (100kΩ pulldown resistor) Ground if not used.
27	NC	No Connection. This pin should be isolated from any traces or via on the PCB board.
28	NC	No Connection. This pin should be isolated from any traces or via on the PCB board.
29	IN7	PWM control input for driver #7, (active high) (100kΩ pulldown resistor) Ground if not used.
30	IN8	PWM control input for driver #8, (active high) (100kΩ pulldown resistor) Ground if not used.
31	NC	No Connection. This pin should be isolated from any traces or via on the PCB board.
32	VS	Battery Supply Input Voltage.
33	D4	Drain of configurable driver #4
34	S4	Source of configurable driver #4
35	S3	Source of configurable driver #3
36	D3	Drain of configurable driver #3
EPAD	Exposed Pad	Connect to Ground

MAXIMUM RATINGS (Voltages are with respect to device substrate)

Rating	Symbol	Value	Unit
Digital supply input voltage (V_{CC})	VCCmax	−0.3 to 7	V
Battery supply input voltage (VS) DC input supply voltage Transient input supply voltage	 VSDCmax VSACmax	 −0.3 to 34 −0.3 to 40	 V V
Digital I/O pin voltage (IN5, IN6, IN7, IN8, SI, SO, CSB, SCLK, EN)	VIOmax	−0.3 to 7	V
Configured for High−Side Operation Drain = VS Source Output DC Voltage (S1−S8) Transient Source Output voltage (S1−S8)	 VSHSXDCmax VSHSXACmax	 −1 to 34 −29 to 34	 V V
Configured for Low−Side Operation Source = GND Drain Output DC Voltage (D1−D8) Transient Drain Output Voltage (D1−D8)	 VDLSXDCmax VDLSXACmax	 −1 to 34 (Note 1) −1 to 48 (Note 2)	 V V
Clamping energy Maximum (single pulse) Repetitive (multiple pulse) (Note)3	 Wmax Wrep	 100 20	 mJ mJ
Electrostatic Discharge (VS, D1−D8, S1−S8) Human Body Model (100 pF, 1.5 kΩ) Machine Model (200 pF) Charged Device	ESD4	 −4000 to 4000 −200 to 200 −1000 to 1000	V
Electrostatic Discharge (All Other Pins) Human Body Model (100 pF, 1.5 kΩ) Machine Model (200pF) Charged Device	ESD2	 −2000 to 2000 −200 to 200 −1000 to 1000	V
AECQ10x−12−REVA SHORT−CIRCUIT RELIABILITY CHARACTERIZATION	 AECsc	 Grade B	
Storage Temperature Range	Tstr	−55 to 150	°C
Moisture Sensitivity Level SO28 SSOP36−EPAD	MSLso MSLssop	MSL3 MSL2	−

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. In this configuration lower voltage limit is due to drain−gate clamp.
2. Internally limited.
3. 1638000 pulses (triangular), 350 mA peak, VS = 18 V, 47 Ω, 410 mH, T_A = 85°C.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value		Unit
		Min	Max	
Digital supply input voltage (V_{CC})	VCCop	3.15	5.25	V
Battery supply input voltage (VS)	Vsop	5.5	28	V
DC Output current (Sx,Dx)	Ixop	−	350	mA
Junction temperature	T_J	−40	150	°C

THERMAL CONDITIONS

Thermal Parameter (Note 4)		Value	Unit
Junction−to−Lead (Ψ_{JL})	SO28 SSOP36−EP	34 37	°C/W
Junction−to−Ambient ($R_{\theta JA}$)	SO28 SSOP36−EP	64.6 55.8	°C/W
Junction−to−Exposed−Pad (Ψ_{JPAD})	SSOP36−EP	7.3	°C/W

4. PCB 50x50x1.2 mm FR4, 2s0p, 2 oz copper, 650 sq mm heater spreader area with no vias. All 8 channels are dissipating 0.147 watts of power each.

ELECTRICAL CHARACTERISTICS (−40°C < T_J < 150°C, 5.5 V < VS < 28 V, 3.15 V < V_{CC} < 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
GENERAL PARAMETERS						
VS Supply Current Standby (Note 5) Run (Note 6)	 IQVS85 IVSop	En = 0 V, 0 V ≤ V_{CC} ≤ 5.25 V, Dx = VS = 13.2 V, Sx = 0 V, −40°C < T_J < 85°C All channels Active	 0 –	 1 –	 5 12	 μA mA
VCC Supply Current Standby (Note 7) Run	 IQVCC IVCCop	EN = 0 V, CSB = V_{CC}, −40°C < T_J < 85°C all channels active, $I_{(SO)}$ = 0	 0 –	 1 –	 5 3	 μA mA
VCC Power−on reset Threshold	VCCPOR	V_{CC} increasing	2.6	2.8	3.0	V
VCC Power−on reset Hysteresis	VCChys		100	200	–	mV
VS Undervoltage Threshold	VSUV	VS increasing	2.5	2.8	3.0	V
VS Undervoltage Hysteresis	VSUhys		100	200	–	mV
VS Overvoltage Threshold	VSOV	VS increasing	32	36	40	V
VS Overvoltage Hysteresis	VSOhys		1.0	2.5	4.0	V
THERMAL RESPONSE						
Thermal Warning	TW	Not ATE tested	120	145	170	°C
Thermal Warning Hysteresis	TWH	Not ATE tested	–	30	–	°C
Overtemperature Shutdown	TLIM	Not ATE tested	155	175	195	°C
Overtemperature Shutdown hysteresis	TLIMHY	Not ATE tested	–	30	–	°C
Ratio of Overtemperature Shutdown to Thermal Warning	TSTOTW	Not ATE tested	1.05	1.20	–	°C/°C
POWER OUTPUTS, DC CHARACTERISTICS						
Output Transistor $R_{DS(on)}$ (Note 8)	RonOPx RonVSminx RonVS3	VS = 8 V, I(Dx) = 200 mA VS = 5.5 V, I(Dx) = 200 mA VS = 3 V, I(Dx) = 200 mA	– – –	1.2 1.4 1.6	2.8 5.6 9.9	Ω
Output Leakage Current (Note 9)	Ilkgx	VS = Dx = 16 V, Sx = 0 V	–	–	5	μA
Open Load Diagnostic Sink Current Low Side	IdiagLSx	Dx = 2.6 V, Sx = 0 V, Output disabled	100	215	350	μA
Open Load Diagnostic Source Current High Side (Note 10)	IdiagHSx	Dx = VS, Sx = VS − 2.6 V, Output disabled −40°C < T_J < 125°C	 −500	 −330	 −150	μA
Open load detection threshold voltage, VD (LS)	VOLDx		1.0	2.0	3.0	V
Open load detection threshold voltage, VS (HS)	VOLSx		VS−3	VS−2	VS−1	V
Over Current (Note 11) High−Side Low−Side	 IlimHS IlimLS	 VS = 16 V VS = 16 V	 −1.90 0.80	 −1.35 1.35	 −0.80 1.90	A
Output fault filter time Over Current Open Load	 TFOC TFOL		 50 50	 100 100	 200 200	μs

5. Refer to Figures 13 and 18 for the VS standby current behavior.
6. Refer to Figure 11. I(VS) versus Temperature.
7. Refer to Figure 17 for the V_{CC} standby current behavior.
8. Refer to Figures 12 and 15 for $R_{DS(on)}$ behavior.
9. Refer to Figure 16 for output leakage current behavior.
10. Refer to Figures 19 and 20 for open load diagnostic current behavior.
11. Refer to Figure 14 for current limit behavior.

ELECTRICAL CHARACTERISTICS (−40°C < T_J < 150°C, 5.5 V < VS < 28 V, 3.15 V < V_{CC} < 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT CLAMPS						
Output clamp Voltage Drain with respect to Source	VOCLS	I(Dx) = 50 mA Source = GND	34	−	48	V
Output clamp Voltage Source with respect to GND	VOCHS	I(Sx) = −50 mA, VS = 14 V	−29	−22	−16	V
POWER OUTPUTS, AC CHARACTERISTICS						
Low Side Rise Time	T_LSr	8 V < VS < 16 V R_{load} = 70 Ω 10/90% criteria, Figure 5	−	12	50	μs
Low Side Fall Time	T_LSf	8 V < VS < 16 V R_{load} = 70 Ω 10/90% criteria, Figure 4	−	12	50	μs
High side Rise Time	T_HSr	8 V < VS < 16 V R_{load} = 70 Ω 10/90% criteria, Figure 4	−	12	50	μs
High side Fall Time	T_HSf	8 V < VS < 16 V R_{load} = 70 Ω 10/90% criteria, Figure 5	−	12	50	μs
Serial Control Output turn−on time (High side and Low−side configuration)	TDONs	8 V < VS < 16 V CSB going high (at 90%) to V_{final} going high (at 10%) or V_{final} going low (at 90%) R_{load} = 70 Ω, Figure 4	1	−	50	μs
Serial Control Output turn−off time (High side and Low−side configuration)	TDOFFs	8 V < VS < 16 V CSB going high (at 90%) to V_{final} going low (at 90%) or V_{final} going high (at 10%) R_{load} = 70 Ω, Figure 5	1	−	100	μs
Parallel Control Output turn−on time (High side and Low−side configuration)	TDONp	8 V < VS < 16 V Inx going high (at 90%) to V_{final} going high (at 10%) or V_{final} going low (at 90%) R_{load} = 70 Ω, Figure 6	1	−	50	μs
Parallel Control Output turn−off time (High side and Low−side configuration)	TDOFFp	8 V < VS < 16 V Inx going low (at 10%) to V_{final} going low (at 90%) or V_{final} going high (at 10%) R_{load} = 70 Ω, Figure 7	1	−	100	μs

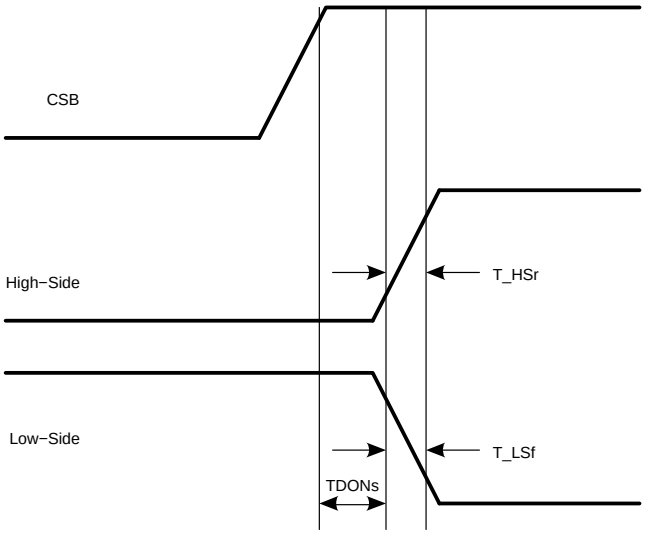


Figure 4. Serial Turn On

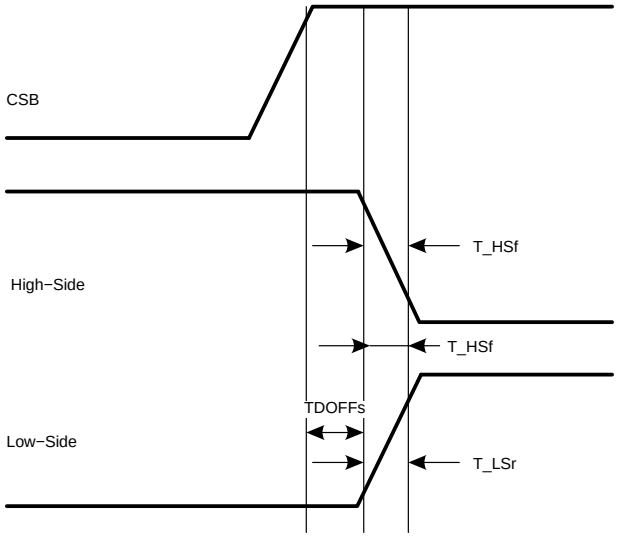


Figure 5. Serial Turn Off

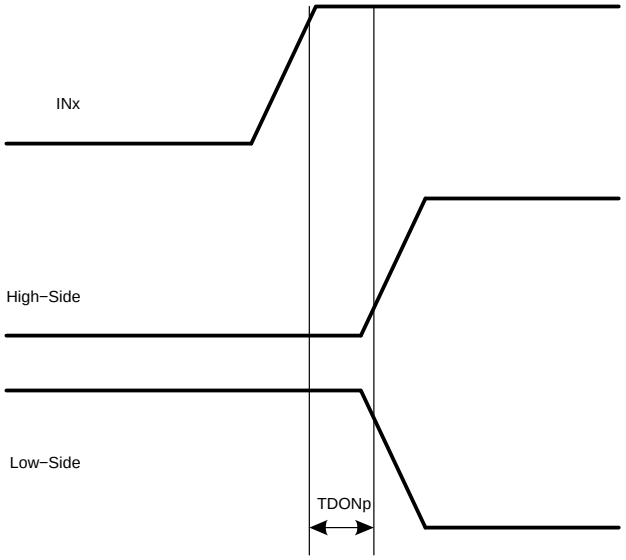


Figure 6. Parallel Turn On

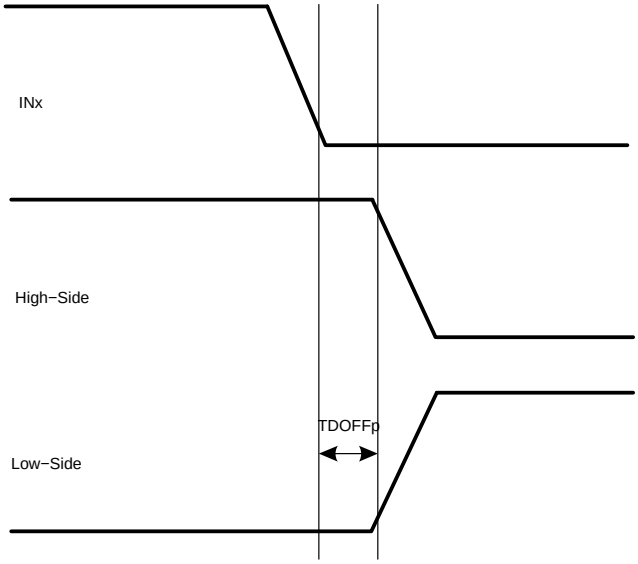


Figure 7. Parallel Turn Off

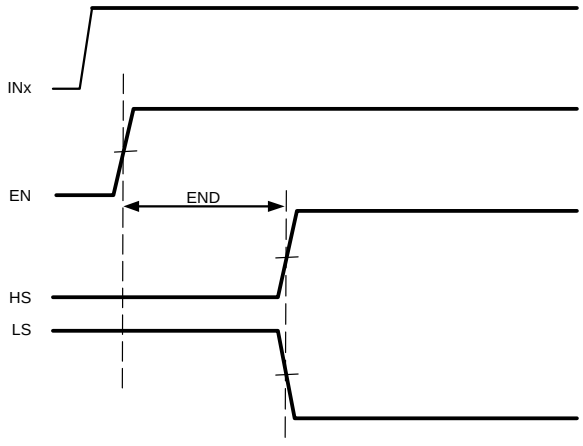


Figure 8. EN Delay Time

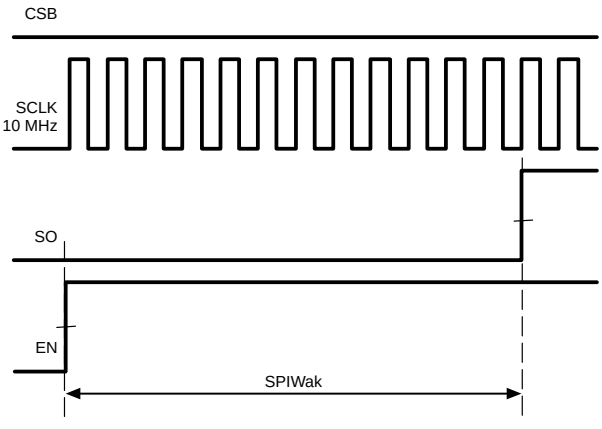


Figure 9. SPI Wake Up

Table 1. DIGITAL INTERFACE CHARACTERISTICS

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Digital Input High Threshold	VINH		2.0	−	−	V
Digital Input Low Threshold	VINL		−	−	0.6	V
Input Pulldown Resistance (EN, SI, SCLK, IN5, IN6, IN7, IN8)	RPDx	EN = SI = SCLK = V_{CC}, IN5 = IN6 = IN7 = IN8 = V_{CC}	50	100	200	kΩ
Input Pullup Resistance (CSB)	IPUCSB	CSB = 0 V	50	100	200	kΩ
CSB Leakage to V_{CC}	ILCSx	CSB = 5 V, V_{CC} = 0 V	−	−	10	μA
Input Capacitance (Note 12)	CINx	Not ATE Tested	−	−	15	pF
SO – Output High	VOUTH	I(out) = −1 mA	V_{CC} − 1.0	−	−	V
SO – Output Low	VOUTL	I(out) = 1.6 mA	−	−	0.4	V
SO Tristate Leakage	ILSOx	CSB = V_{CC}	−10	−	10	μA
SO Tristate Input Capacitance (Note 12)	CSOx	Not ATE Tested	−	−	15	pF
SCLK Frequency	CLKf	V_{CC} = 5 V V_{CC} = 3.3 V	− −	− −	5 2	MHz
SCLK Clock Period	CLKper	V_{CC} = 5 V V_{CC} = 3.3 V	200 500	− −	− −	ns ns
SCLK High Time	CLKH	V_{CC} = 5 V, Figure 10	85	−	−	ns
SCLK Low Time	CLKL	V_{CC} = 5 V, Figure 10	85	−	−	ns
SCLK Setup Time	CLKsup	V_{CC} = 5 V, Figure 10	85	−	−	ns
SI Setup Time	Sisup	V_{CC} = 5 V, Figure 10	50	−	−	ns
SI Hold Time	SIH	V_{CC} = 5 V, Figure 10	50	−	−	ns
CSB Setup Time	Cssup	V_{CC} = 5 V, Figure 10	100	−	−	ns
CSB High Time	CSH	V_{CC} = 5 V, Figure 10	200	−	−	ns
SO enable after CSB falling edge (Note 12)	CStSOf	V_{CC} = 5 V, Figure 10	−	−	50	ns
SO disable after CSB rising edge (Note 12)	CStSOr	V_{CC} = 5 V, Figure 10	−	−	50	ns
SO Rise Time	SOR	V_{CC} = 5 V, C_{load} = 40 pF	−	−	25	ns
SO Fall Time	SOF	V_{CC} = 5 V, C_{load} = 40 pF	−	−	25	ns
SO Valid Time (Note 12)	SOV	V_{CC} = 5 V, C_{load} = 40 pF, Figure 10	−	−	50	ns
EN Low Valid Time	ENL		10	−	−	μs
EN Delay Time	END	V_{CC} = INx = 5 V EN going high 50% to OUT5 − OUT8 turning on 50%.	−	−	100	μs
SPI wake up after EN rising edge	SPIWak	SI = 5 V, CSB = 0 V, SCLK = 10 MHz, EN going high 50% to SO going high 50%, Figure 9	−	−	200	μs

12. Not subject to production testing.

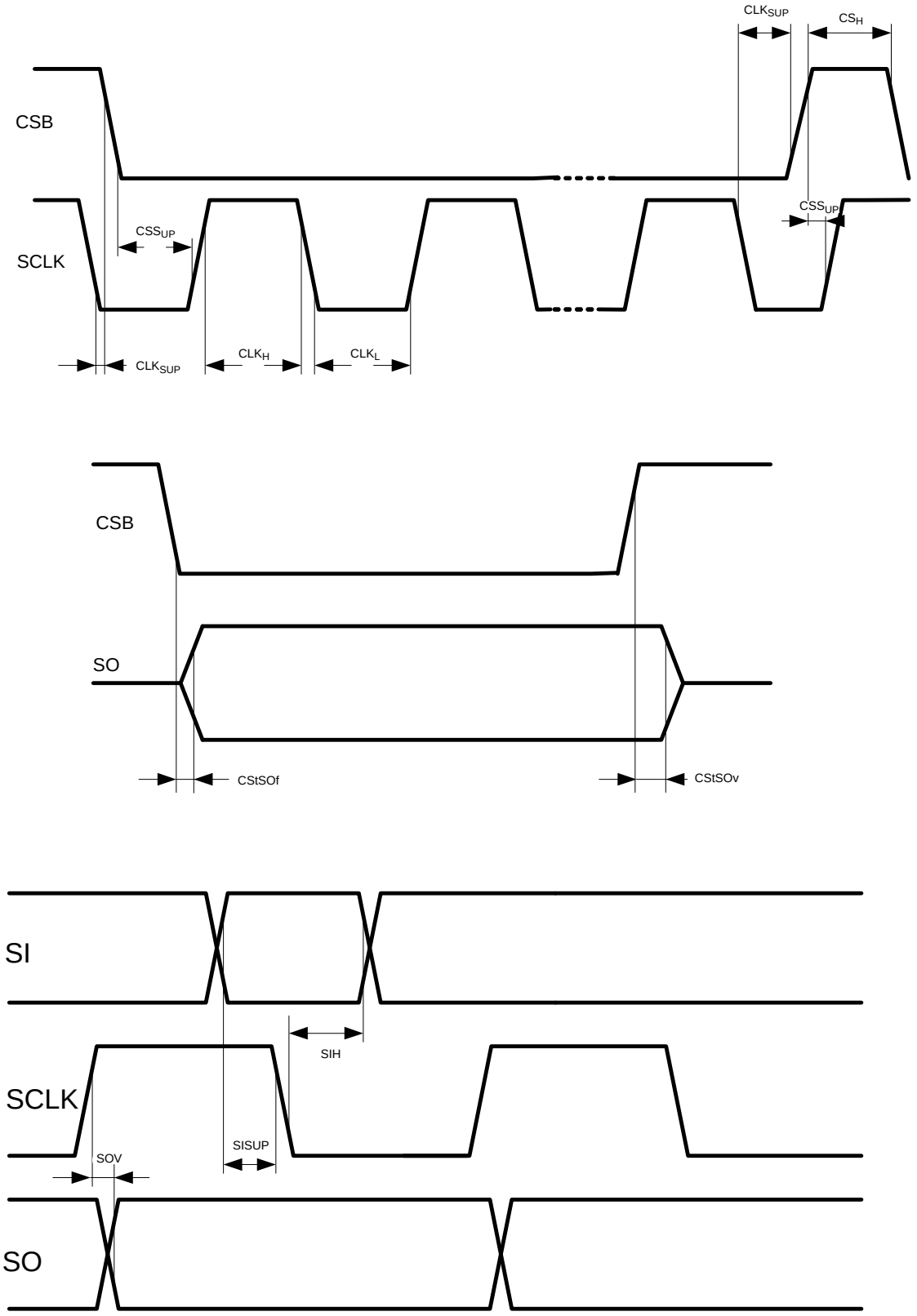


Figure 10. Detailed SPI Timing

TYPICAL PERFORMANCE CHARACTERISTICS

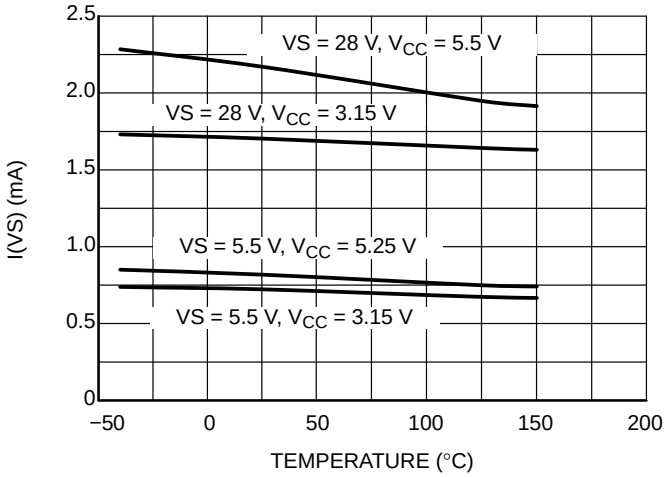


Figure 11. I(VS) vs. Temperature

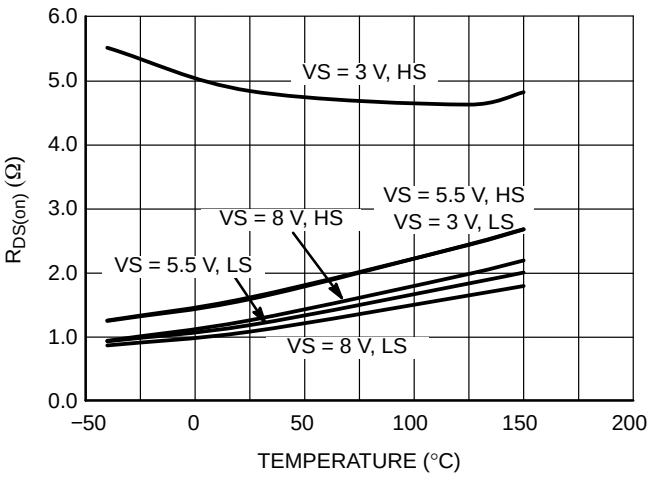


Figure 12. $R_{DS(on)}$ vs. Temperature

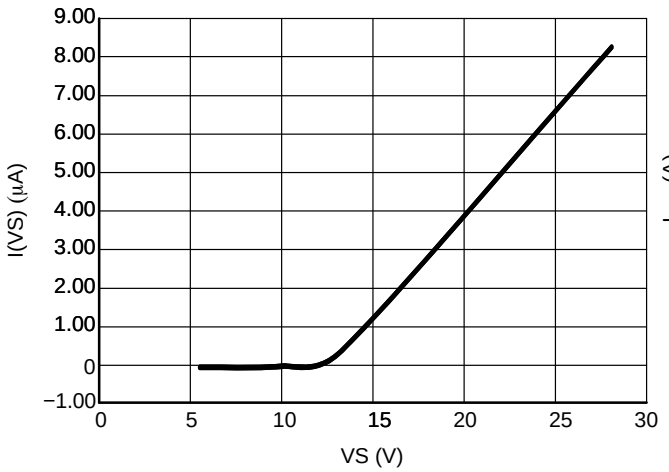


Figure 13. I(VS) Standby Current vs. VS at 25°C

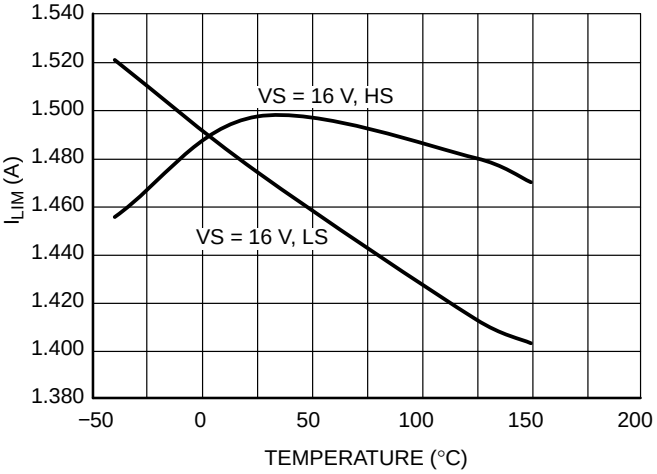


Figure 14. Output Over Current vs. Temperature

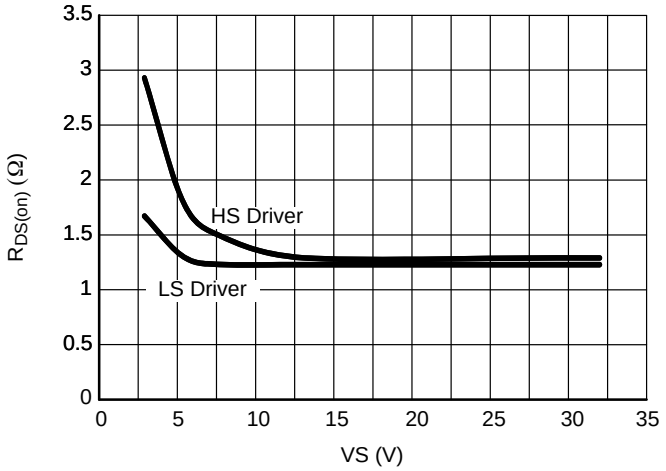


Figure 15. $R_{DS(on)}$ vs. VS

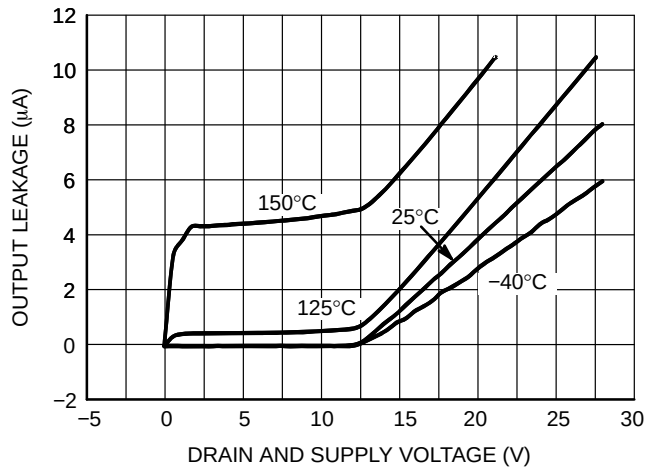


Figure 16. Standby Output Leakage vs. VS

TYPICAL PERFORMANCE CHARACTERISTICS

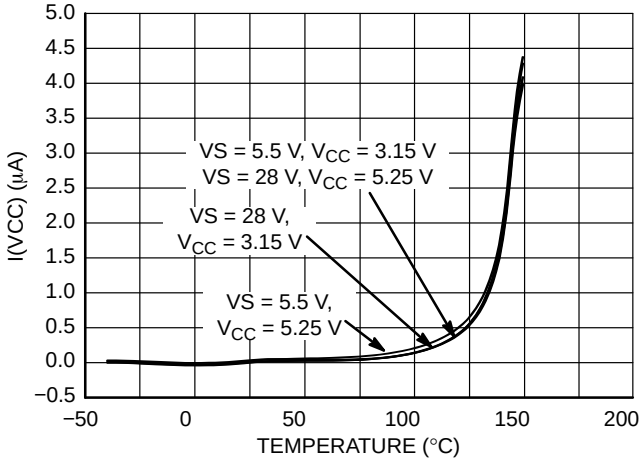


Figure 17. I(VCC) vs. Temperature

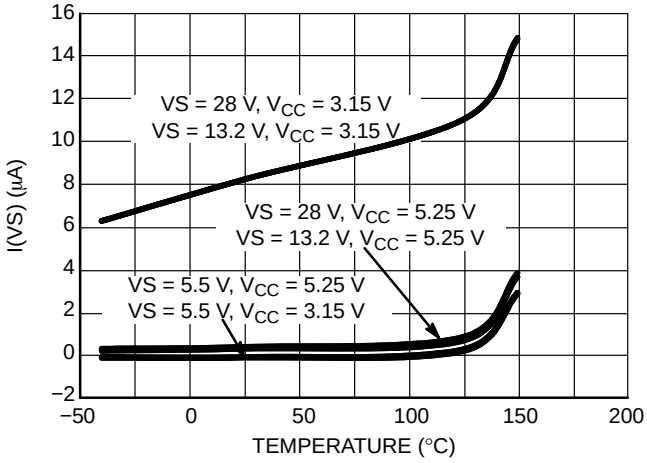


Figure 18. VS Standby Current vs. Temperature

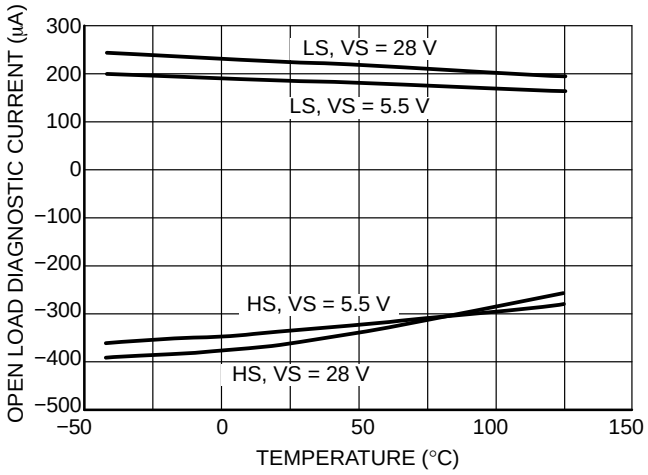


Figure 19. Open Load Detect Current vs. Temperature

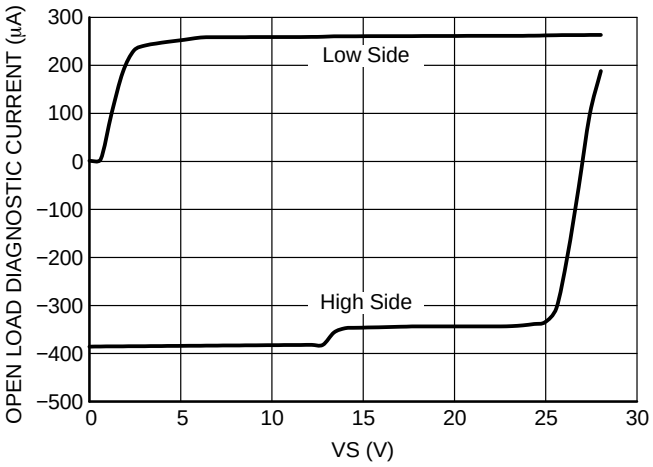


Figure 20. Open Load Detect Current vs. VS @ 25°C

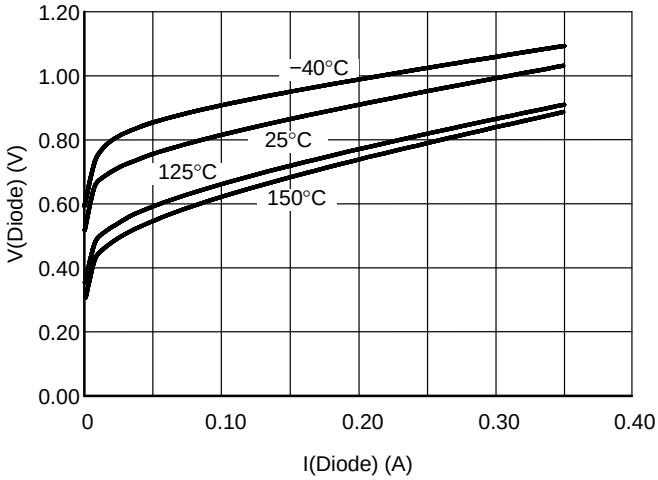


Figure 21. Source−to−Drain Voltage Body Diode

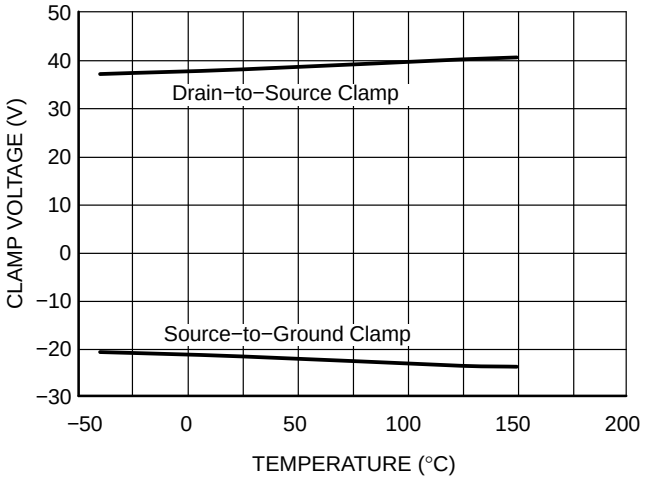


Figure 22. Output Clamp vs. Temperature

DETAILED OPERATING DESCRIPTION

Normal Operation

Power Outputs

The NCV7608 provides eight independent power transistors with pins D1−D8, and S1−S8 as drain and source outputs respectively. For High−side Drive configurations (sourcing), the drain pins are connected to the battery supply. In Low−Side configurations (sinking), the drain pins are connected to the load. All outputs may be configured as high−side, low−side, half−bridge, or H−bridge. Internal clamping structures are provided to limit transient voltages when switching inductive loads.

SPI−Interface

The device provides a 16 bit SPI−interface. Data is imported into the NCV7608 through the SI (serial input) pin. Data is exported out of the NCV7608 through the SO (serial output) pin. The input−frame (SI) is used to command the output stages and program individual channel open load diagnostics. The response frame (SO) provides channel−specific (1bit / channel) status information and fault information. See Table 1 for channel status decoding. Words should be composed of 16 bits LSB (least significant bit) transmitted first.

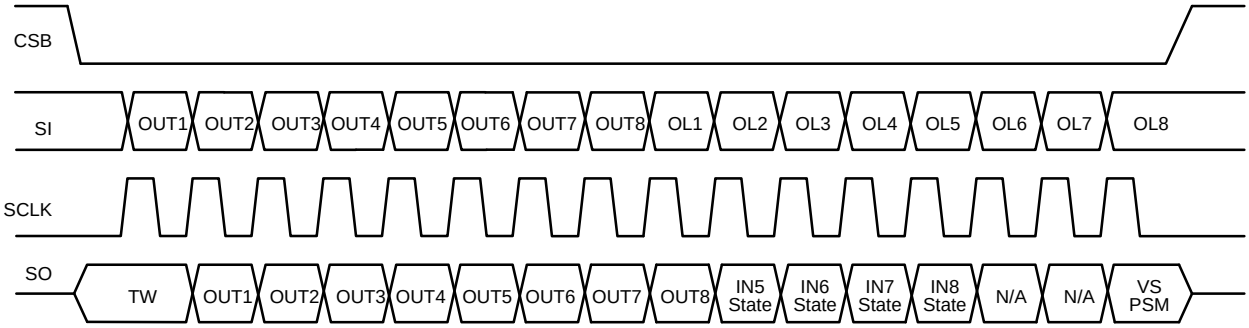


Figure 23. SPI Frame

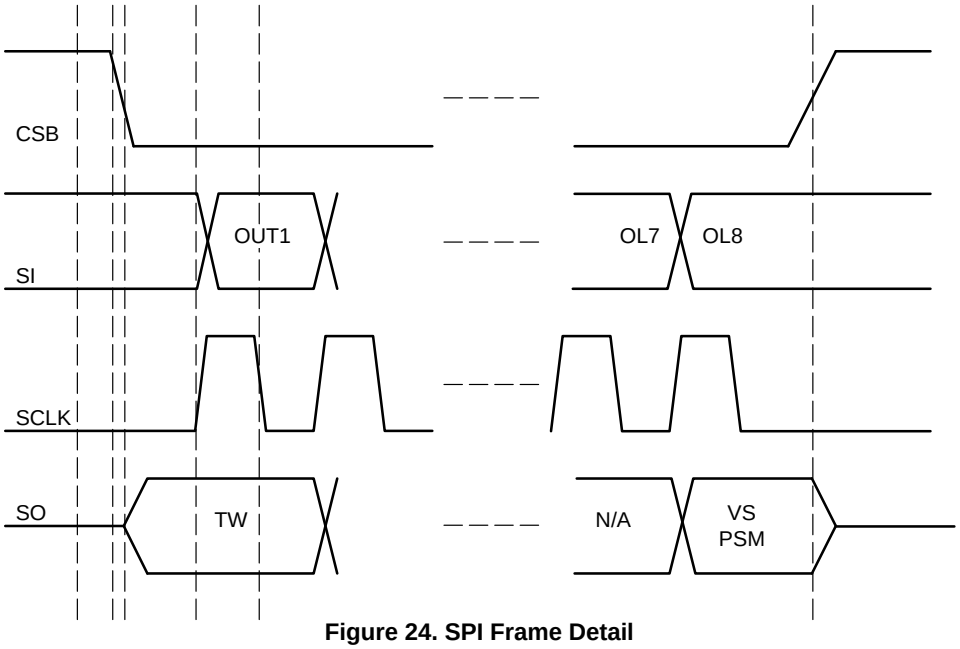


Figure 24. SPI Frame Detail

Table 2. SPI INPUT / OUTPUT

Input Data			Output Data		
Bit Number	**Bit Description**	**Bit Status**	**Bit Number**	**Bit Description**	**Bit Status**
15	Driver 8 Open Diagnostic Enable	0 = Disable 1 = Enable	15	VS Power Supply Monitoring	0 = No Fault 1 = Fault
14	Driver 7 Open Diagnostic Enable	0 = Disable 1 = Enable	14	N/A	0
13	Driver 6 Open Diagnostic Enable Driver 6 Open Diagnostic Enable	0 = Disable 1 = Enable	13	N/A	0
12	Driver 5 Open Diagnostic Enable	0 = Disable 1 = Enable	12	IN8 State (Note 13)	0 = (IN8 = 0) 1 = (IN8 = 1)
11	Driver 4 Open Diagnostic Enable	0 = Disable 1 = Enable	11	IN7 State (Note 13)	0 = (IN7 = 0) 1 = (IN7 = 1)
10	Driver 3 Open Diagnostic Enable	0 = Disable 1 = Enable	10	IN6 State (Note 13)	0 = (IN6 = 0) 1 = (IN6 = 1)
9	Driver 2 Open Diagnostic Enable	0 = Disable 1 = Enable	9	IN5 State (Note 13)	0 = (IN5 = 0) 1 = (IN5 = 1)
8	Driver 1 Open Diagnostic Enable	0 = Disable 1 = Enable	8	Driver 8 Status	0 = No Fault 1 = Fault
7	Driver 8 Enable	0 = Disable 1 = Enable	7	Driver 7 Status	0 = No Fault 1 = Fault
6	Driver 7 Enable	0 = Disable 1 = Enable	6	Driver 6 Status	0 = No Fault 1 = Fault
5	Driver 6 Enable	0 = Disable 1 = Enable	5	Driver 5 Status	0 = No Fault 1 = Fault
4	Driver 5 Enable	0 = Disable 1 = Enable	4	Driver 4 Status	0 = No Fault 1 = Fault
3	Driver 4 Enable	0 = Disable 1 = Enable	3	Driver 3 Status	0 = No Fault 1 = Fault
2	Driver 3 Enable	0 = Disable 1 = Enable	2	Driver 2 Status	0 = No Fault 1 = Fault
1	Driver 2 Enable	0 = Disable 1 = Enable	1	Driver 1 Status	0 = No Fault 1 = Fault
0	Driver 1 Enable	0 = Disable 1 = Enable	0	Thermal Warning (TW)	0 = No Fault 1 = Fault

An output driver (Driver Status) fault is either open load, over current, or over temperature.

13. When over current or thermal shutdown fault occurs, bits 9 through 12 records the state of INx.

SPI Input

Driver Enable (bits 0−7)

A zero turns the driver off.

A one turns the driver on.

Open Load Diagnostic (bits 8−15)

A zero programming bit disables the detection of an open load condition.

A one programming bit enables the detection of an open load condition.

Parallel Input (INx) State (bits 9−12)

The state of the parallel (PWM) input pins (Inx) are mirrored to SPI output bits #9−12. When overcurrent or thermal shutdown fault occurs, bits 9 through 12 record the state of INx. This enables the user to distinguish an open load fault from an over current fault when the NCV7608 is operated from two isolated controllers for the SPI input and the Parallel input.

SPI Output

Table 3. SO DRIVER STATUS INFORMATION SUMMARY (Bits 0−8, 15)

Driver Enable	Open Load Diagnostic enable	SO Feedback	Status Information Reset Requirement
Disabled	Disabled	0	N/A
Disabled	Enabled	0 (No Open Load)	N/A
		1 (Open Load Detected)	N/A
Enabled	X	0 (No Fault)	N/A
		1 (Over Current)	A valid SPI command with the offending Driver DISABLED is received.
		1 (VS Power supply fail)	Any valid SPI command **AND** VS within limits
		1 (Thermal Warning)	N/A
		1 (Thermal Shutdown)	The over temperature goes away **AND** a valid SPI frame with the offending driver pair DISABLED is received.

X=Don't Care

Frame Detection

Input word integrity (SI) is evaluated by the use of a frame consistency check. The word frame length is compared to an n * 16 bit (where n is an integer) acceptable word length before the data is latched into the input register. This guarantees the proper word length has been imported and allows for daisy chain operation applications.

The frame length detector is enabled with the CSB falling edge and the SCLK rising edge.

SCLK must be low during the CSB rising edge.

Reference the valid SPI frame shown below.

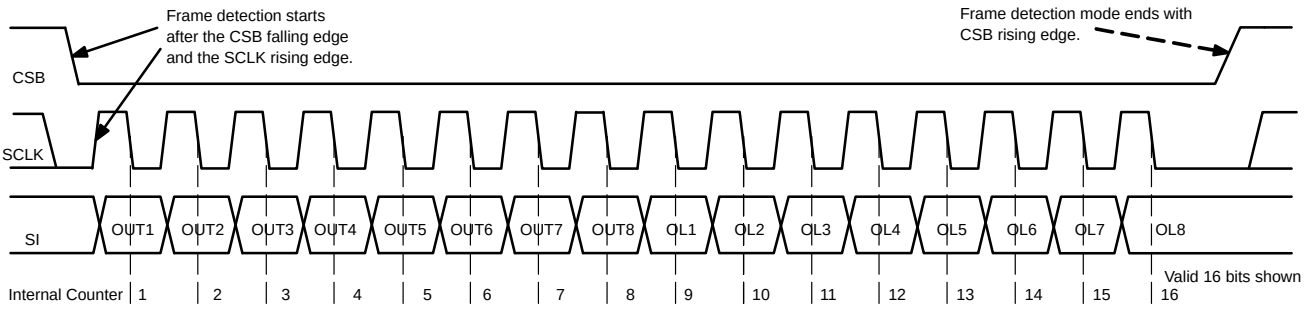


Figure 25. Frame Detection

PWM Operation

Channels 5, 6, 7, and 8 can be controlled via the serial port (SPI) or via the respective parallel port input pins (IN5−IN8).

The SPI information is OR'd with the respective Parallel input control pins (INx).

INx = 1 activates the output stage.

INx = 0 deactivates the output stage.

Special attention should be paid to detection of over current and open load conditions when operated in a pwm mode. These faults are detected in a 100 μs (typ) time window. Faults will not be detected at higher frequencies if the time period of the input signal does not allow for 100 μs detection time.

Handling of Fault Conditions

Table 4. FAULT SUMMARY TABLE

Fault	Fault Memory	Driver Condition	Output Register Clear Requirement
Open Load	None	Allowed to turn on	N/A
Over Current	Latched	Latched Off	A valid SPI command is received with the offending driver disabled
Thermal Warning	None	Allowed to turn/ remain on as long as the device is not in thermal shutdown	N/A
Thermal Shutdown	Latched (Note 14)	Latched Off	The over temperature goes away **AND** a valid SPI frame with the offending driver pair DISABLED is received.
VS Power Supply Fail	Latched (Note 14)	Allowed to turn on while the Voltage is within operating range	After ANY valid SPI frame & voltage within operating range

14. Latched conditions are cleared in the same manner (via the SPI port) during normal operation regardless of the driver turn on command path (via a SPI command or via a parallel input command). Latches are also cleared by cycling the EN pin or with a power−on reset of V_{CC}.

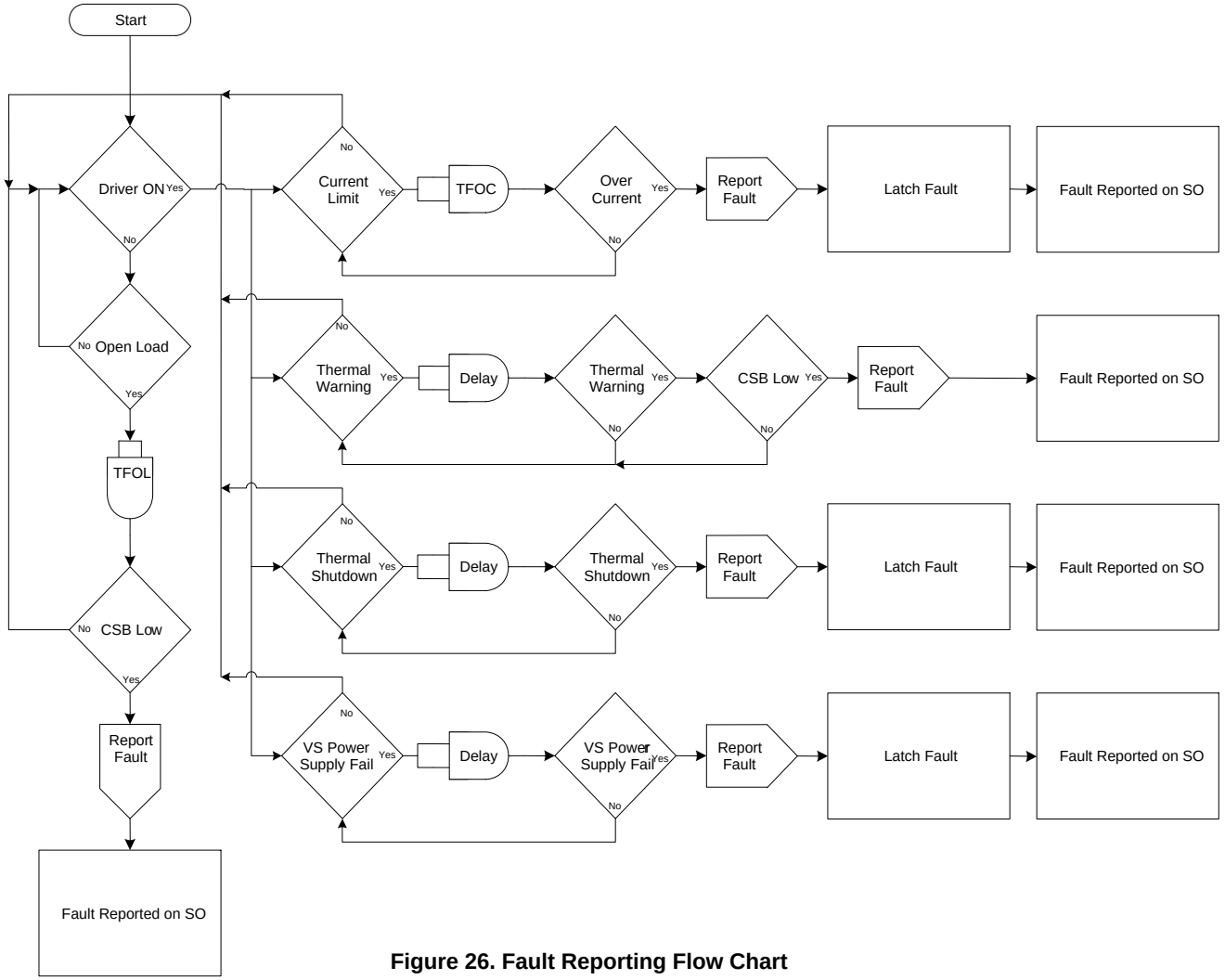


Figure 26. Fault Reporting Flow Chart

Fault Filters

The NCV7608 detects overtemperature, over current, VS Power Supply and open load faults. Faults are reported in the Output Data fault register. The fault filter timer for over current or open load is 100 μs (typ). An over current or open load event must exist for this period of time to be recognized. There are eight fault timers, one dedicated to each driver for use for both over current and open load. Thermal Warning, Thermal Shutdown and VS Power Supply Fail each have there own dedicated timers.

Open Load

Open Load conditions are detected in the off mode. See “OFF−Mode Open Load Diagnostics” for details.

Over Current

The output current is limited in both high−side and low−side configuration. Over Current is detected in the turn on mode. High power dissipation during over current can cause overtemperature shutdown. Over Current is a latched off event. Latching off a driver in over current is especially useful in systems utilizing a hierarchical software architecture whereby the microprocessor sends a command (such as turning a device on when a short circuit exists) and then proceeds to other focused microprocessor activity. Eliminating an auto retry upon over current fault detection scheme reduces IC stress by reducing the frequency of attempts to turn back on.

Thermal Warning & Overtemperature Shutdown

Four independent Overtemperature shutdown circuits are featured (one common sensor for each drive pair). Channels are sequentially paired together with its own thermal detection circuit as Channels 1 and 2, Channels 3 and 4, Channels 5 and 6, and Channels 7 and 8. Each thermal detection circuit senses two temperature levels, one to give a Thermal Warning (145°C typ) (TW, bit = 0), and one to shut the driver pair off (Overtemperature) at a higher temperature 30°C above TW (175°C typ). When the thermal detection circuit reaches the temperature point of Thermal Warning, the output data bit 0 (TW) will be set to a 1, and the outputs will remain on. Overtemperature events will be recorded as faults to the offending Output Driver pair

independently of the input state (serial or parallel). Overtemperature shutdown is a latched event.

Since thermal warning precedes an overtemperature shutdown, software polling of this bit will allow for load control and possible prevention of overtemperature shutdown conditions.

Thermal Warning Retrieval

Thermal warning information can be retrieved immediately without performing a complete SPI access cycle. Figure 27 below displays how this is accomplished. Bringing the CSB pin from a 1 to a 0 condition immediately displays the information on the output data bit 0, thermal warning, even in the absence of a SCLK signal. As the temperature of the NCV7608 changes from a condition from below the thermal warning threshold to above the thermal warning threshold, the state of the SO pin changes and this level is available immediately when the CSB goes to 0. A 0 on SO indicates there is no thermal warning, while a 1 indicates the IC is above the thermal warning threshold.

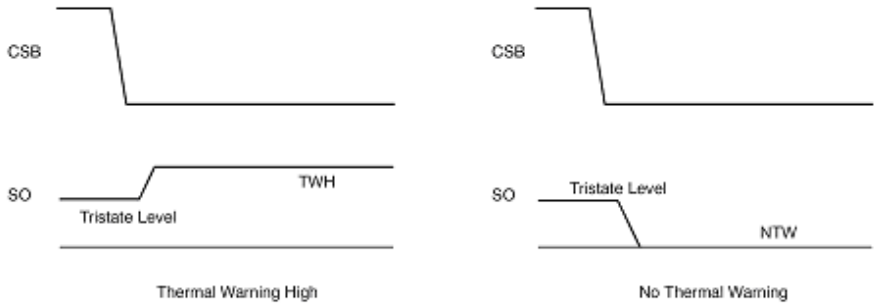


Figure 27. Accessing Thermal Warning Bit

Power Supply Monitoring

Undervoltage shutdown

Both supply voltages (V_{CC} and VS) are monitored for undervoltage. When V_{CC} goes below the threshold, all outputs are turned OFF and the input and output registers are cleared. An undervoltage condition on VS will cause all channels to shut down. The fault bit (Bit #15) is latched in the Output Data Register. The channels will return to the commanded status after reaching operational VS levels provided V_{CC} UVLO is not breached. The SPI port remains active during VS undervoltage within a valid VCC voltage. Drivers are guaranteed to operate with automotive cranking voltages down to 3 V on VS per the undervoltage shutdown thresholds. Bit# 15 is cleared with a valid SPI frame and VS within the operating limits.

Overvoltage shutdown

VS is continuously monitored for overvoltage conditions. The threshold is set above automotive jump start conditions allowing operation of the IC during jump start. The minimum overvoltage threshold is 32 V. When VS goes above the overvoltage threshold voltage, all outputs are turned OFF. The fault bit (Bit #15) is latched in the Output Data Register. Input and output registers maintain all information. The channels will return to the commanded status after reaching operational VS levels provided V_{CC} UVLO is not breached. The SPI port remains active during VS overvoltage within a valid VCC voltage. Bit #15 is cleared with any valid SPI frame and VS within the operating limits.

OFF−Mode Open Load Diagnostics

Open load diagnostics are performed when the drivers are off (provided the channel is programmed to perform the operation via Bits #8 through #15). Open load diagnostics are performed by connecting two tracking current sources (IDIAGHSx and IDIAGLSx) to the corresponding outputs. To support both operation modes (high−side and low−side) and provide minimum delay due to external capacitances, both Drain and Source pin voltages of the device are monitored to generate the diagnostic information. Channel diagnostic information is directed to the output data register. Open load diagnostics are disabled during VS undervoltage or overvoltage events or when EN is low.

Figure 28 shows the NCV7608 open load diagnostics principles.

Figure 29 shows the internal circuitry used with the device set up as a low−side driver.

Figure 30 shows the internal circuitry used with the device set up as a high−side driver.

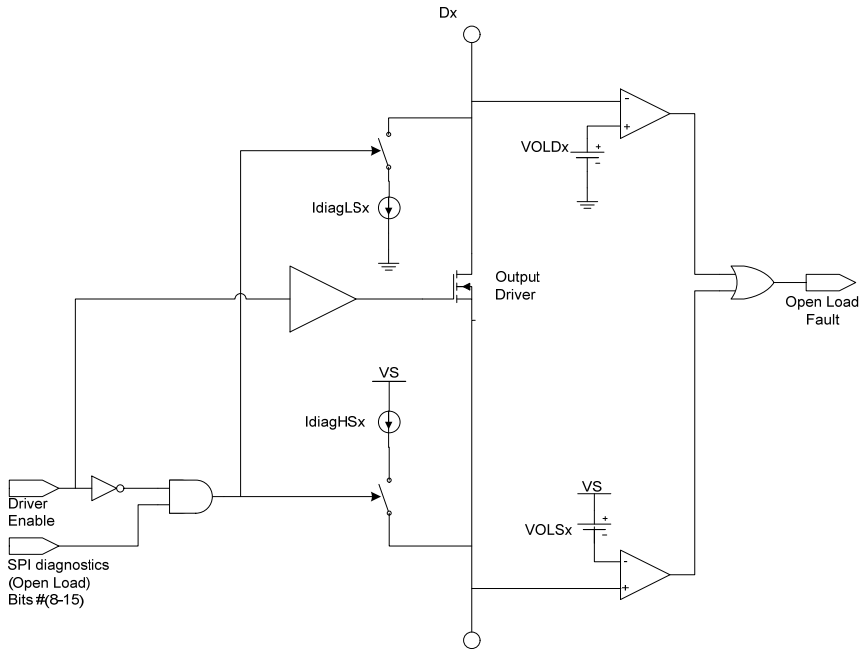


Figure 28. Open Load Diagnostic Principle

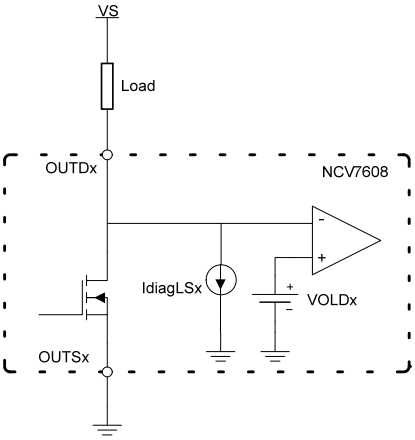


Figure 29. Open Load Circuitry as Low Side Driver

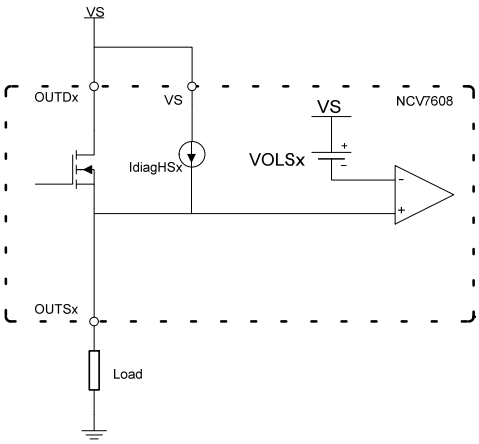


Figure 30. Open Load Circuitry as High Side Driver

Open Load Diagnostic Performance

System design sometimes requires open load diagnostics to be turned off to prevent unintended operation. Input Bits 8−15 control this function.

One application example would be driving LED's. Leaving the diagnostic circuitry turned on would result in visible illumination of the LED's because of the currents used in open load detection. Open load detection may still be utilized by testing at low time intervals.

Miscellaneous

Enable

A logic low on EN puts the device in a current saving mode. Quiescent current (V_{CC}) with EN low is less than 5 μA. A logic high on EN powers up the device allowing operation through the parallel inputs (IN5...IN8). An internal pulldown resistor is provided to ensure device turn−off in the event the enable signal is lost.

A low on EN will result in a power−on−reset to the logic. All outputs will be shut off and all registers reset.

Loss of Ground

The NCV7608 output drivers will not be active during a loss of ground condition. No damage to the device will occur during this condition for VS less than or equal to 16 V.

Diagnostic Implementation

To provide maximum flexibility in using the device as an H−Bridge driver, a current ratio between the HS and LS diagnostic currents is implemented (the diagnostic source current is always higher in magnitude than the diagnostic

sink current). Equal diagnostic currents would result in unpredictable results due to process variation.

Timing Information

Open Load

Open Load is reported if open load is enabled and an open load fault exists.

Open Load is not a latched condition and is not reported when drivers are on.

To be captured, Open Load must be present when CSB goes low.

* SPI Driver Enable bit = 0 and associated INx = 0

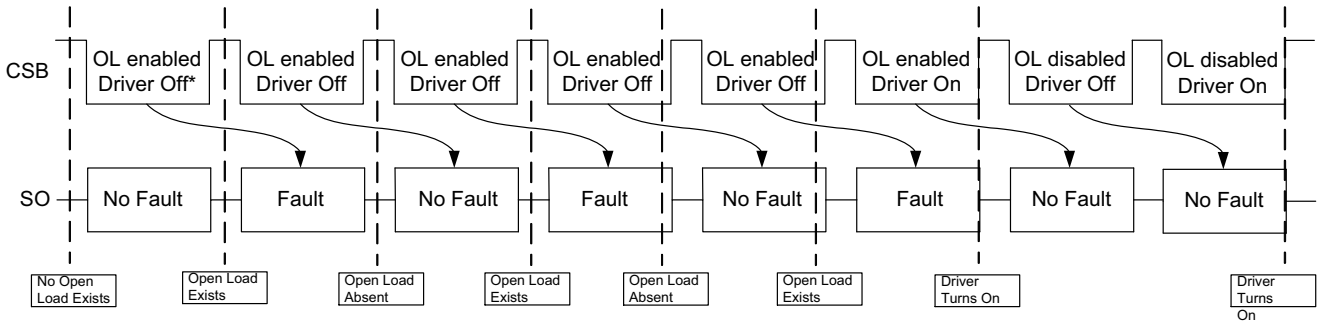


Figure 31. Open Load Timing Diagram

Over Current

Over current is reported if the drivers' over current detection threshold is breached.

The driver is latched off after 100 μs from the over current detection.

To reset the driver status bit for over current, a valid SPI frame with ENx = 0 is required. This will reset the driver status bit and the driver can be turned back on in the next valid SPI frame.

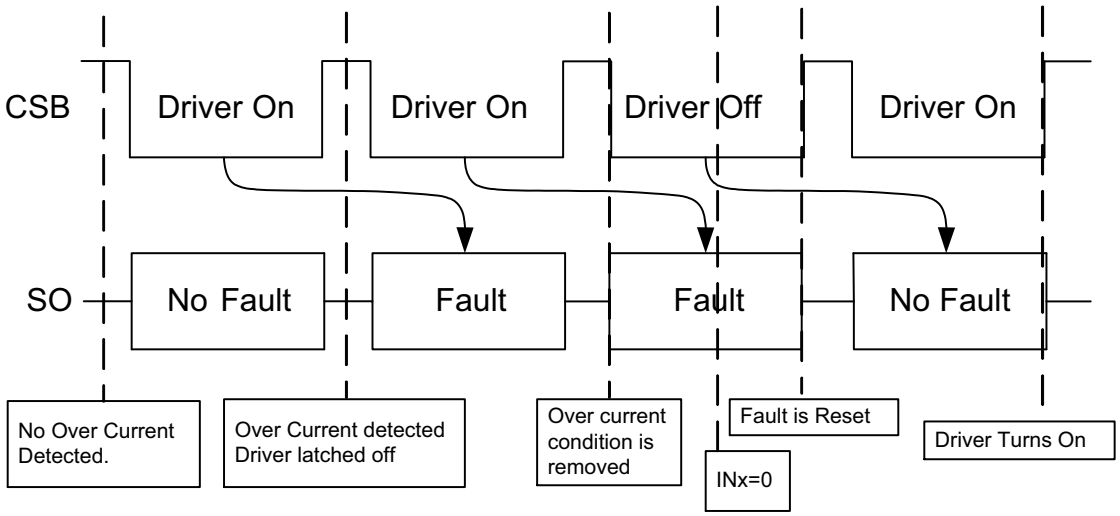


Figure 32. Over Current Timing Diagram

Thermal Warning and Thermal Shutdown

Thermal Warning is reported in bit #0 when the die temperature goes above 145°C (typ)

and does not fall below 145°C (typ) – 30°C hysteresis (typ). Thermal Warning is only sampled and reported when CSB is low.

Thermal Shutdown will turn off the two drivers associated with the thermal sensor when the die temperature is above 175°C (typ). The driver status bit will be latched.

The driver status is reset if the die temperature falls below 175°C (typ) – 30°C (typ) and a valid SPI frame with the Driver(s) x Enable bit = 0. The driver(s) can then be turned on in the next valid SPI frame with the Driver x Enable(s) = 1.

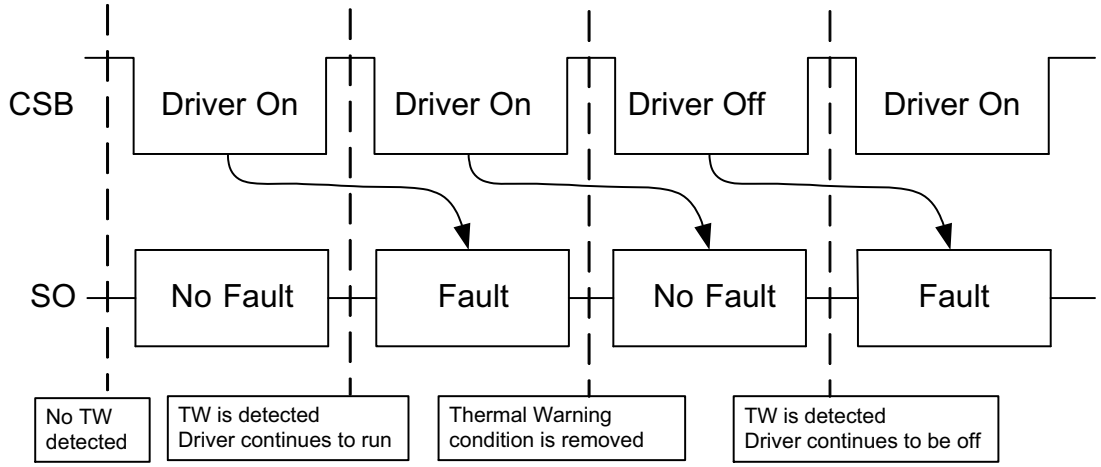


Figure 33. Thermal Warning Timing Diagram

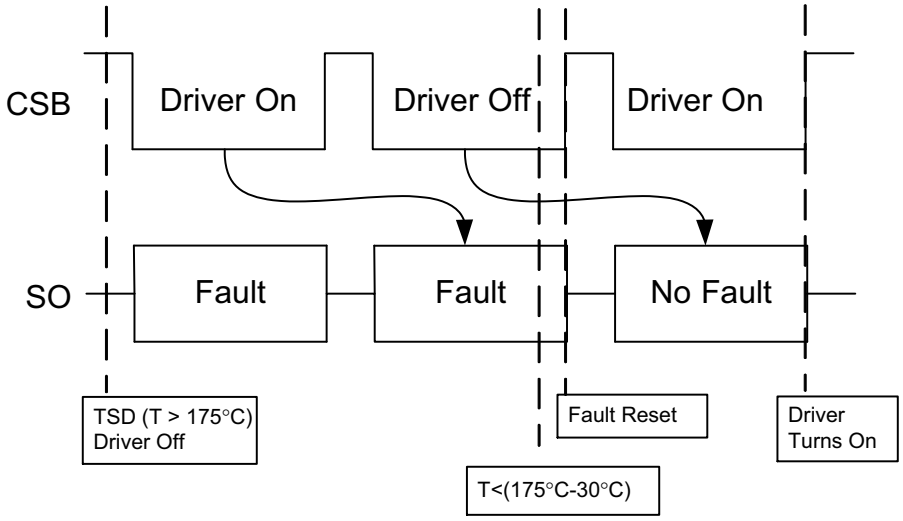


Figure 34. Thermal Shutdown Timing Diagram

Power Supply Fail

VS Overvoltage (OV) or undervoltage (UV) is reported using bit #15 (PSM) in the SO output data register. This is a latched event.

Drivers will shut off during VS OV or UV.

When coming out of VS OV or UV, the drivers will take on the state determined by the last valid SPI frame.

The VS Power Supply Monitoring bit (bit #15) will be reset by any valid SPI frame.

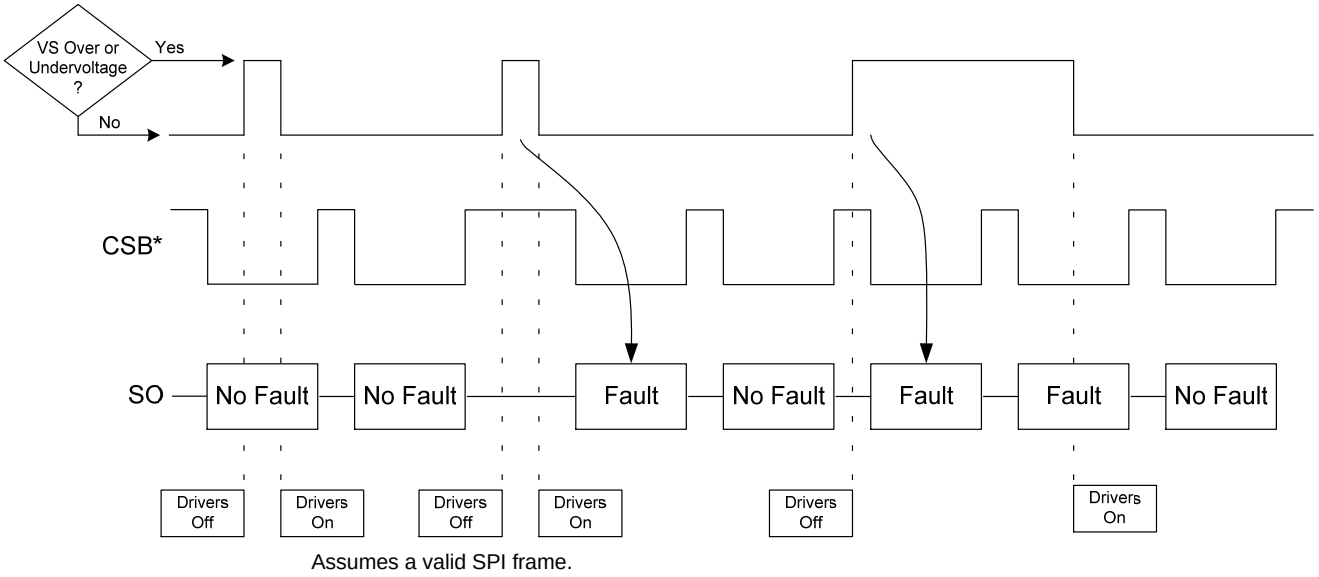


Figure 35. Power Supply Fail Timing Diagram

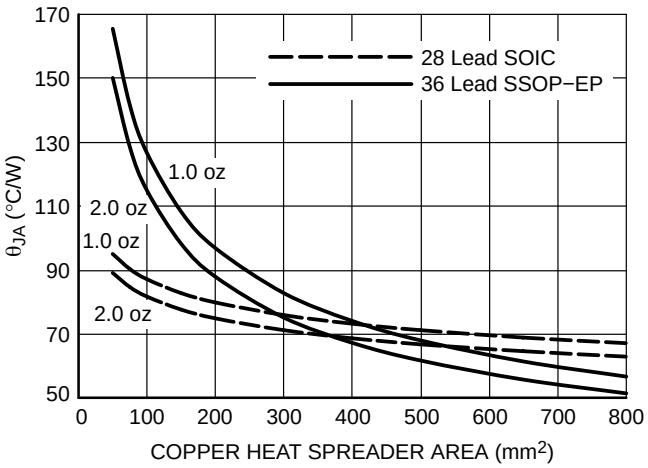


Figure 36. θ_{JA} vs. Copper Heat Spreader

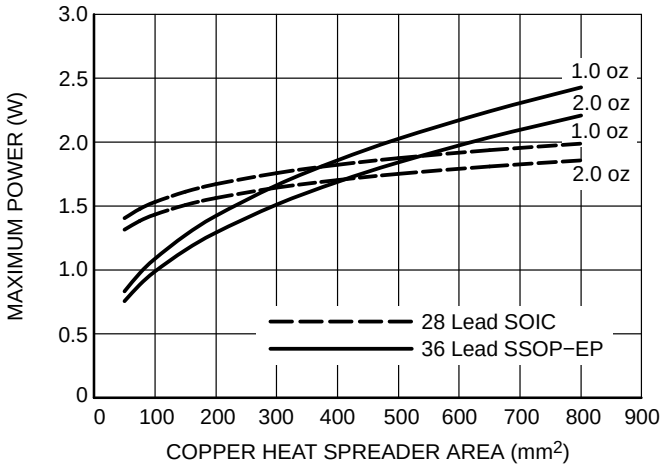


Figure 37. Maximum Power vs. Copper Heat Spreader

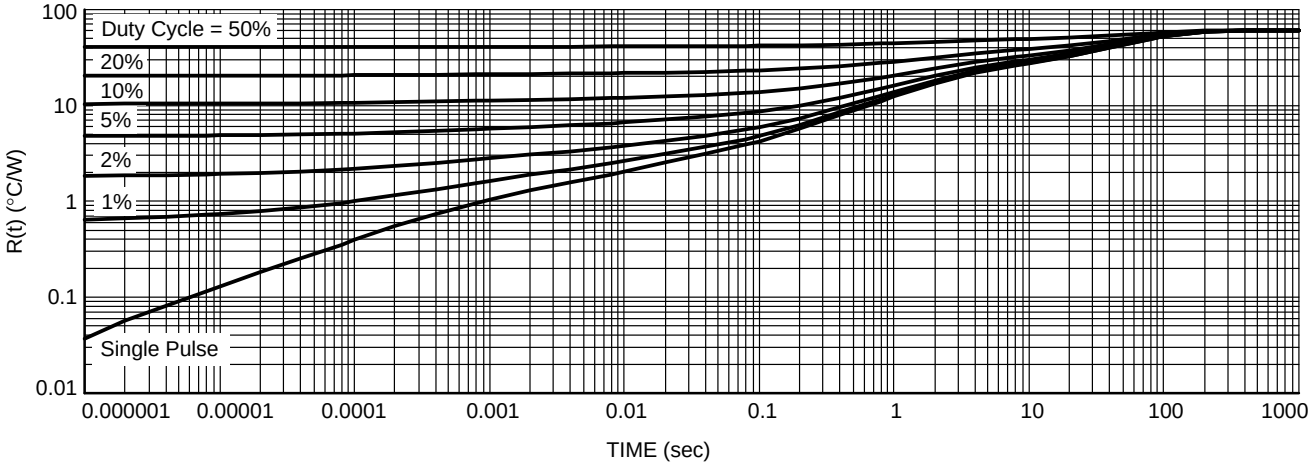


Figure 38. NCV7608−28 Lead SOIC (body 18x7.55x2.55 mm) PCB Cu Area 650 sq mm PCB thk 2 oz All Outputs On

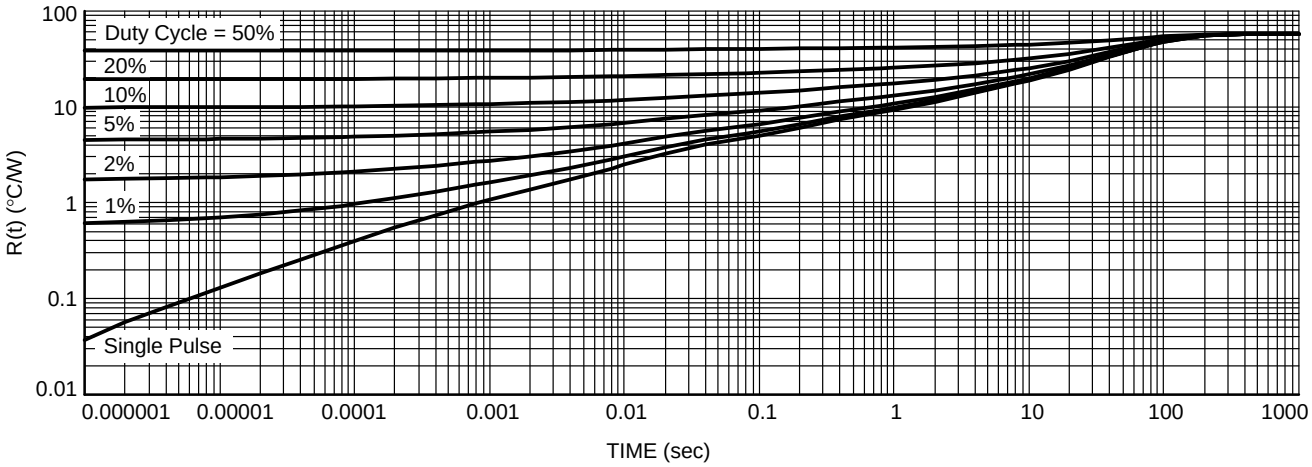
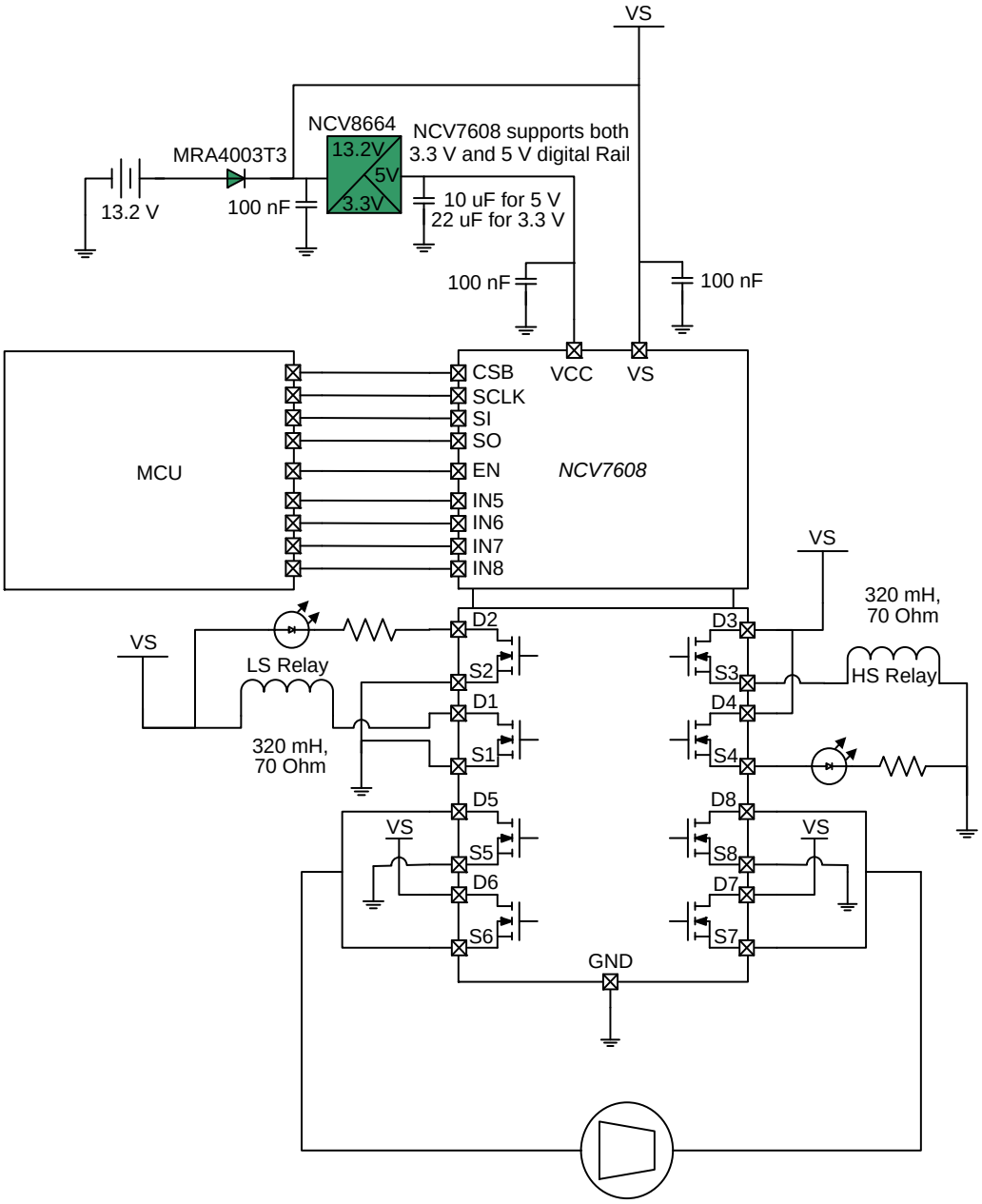


Figure 39. 4.2x5.8x0.25 mm−36 Lead SSOP−EP PCB Cu Area 650 sq mm PCB thk 2 oz All Outputs On

Typical Application

The drawing below demonstrates the versatility of the NCV7608 in a typical application.



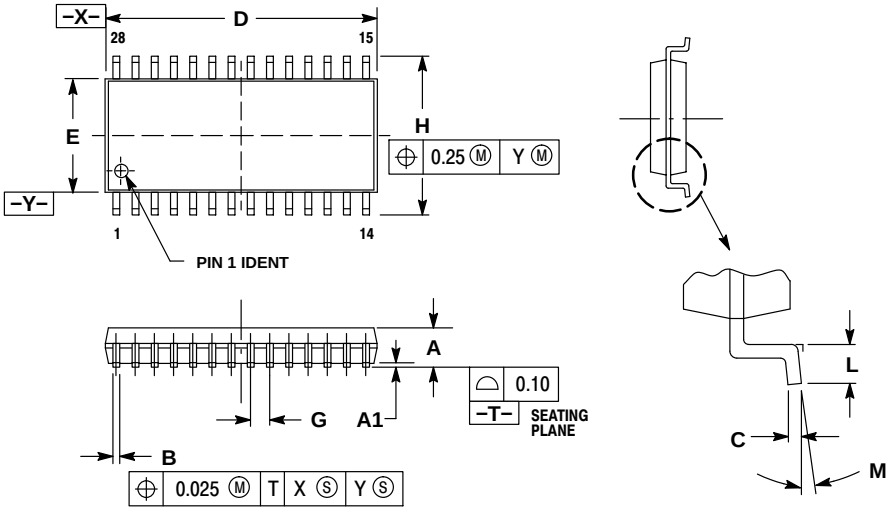
ORDERING INFORMATION

Device	Package	Shipping†
NCV7608DWR2G	SOIC−28 WB (Pb−Free)	1000 / Tape & Reel
NCV7608DQR2G	SSOP36−EP (Pb−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

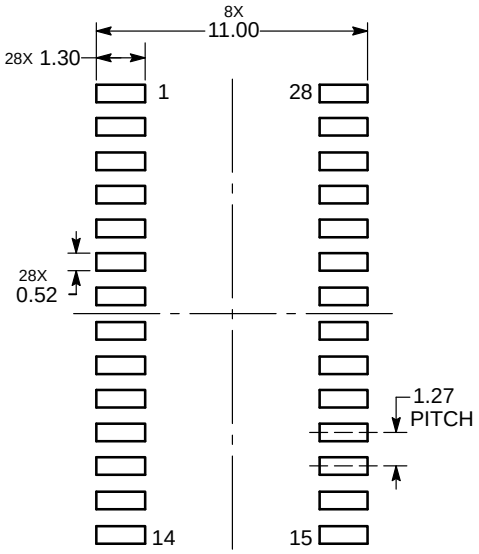
SOIC−28 WB
CASE 751F
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBER PR5OTRUSION SHALL NOT BE 0.13 TOTATL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
G	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
M	0 °	8 °

SOLDERING FOOTPRINT*

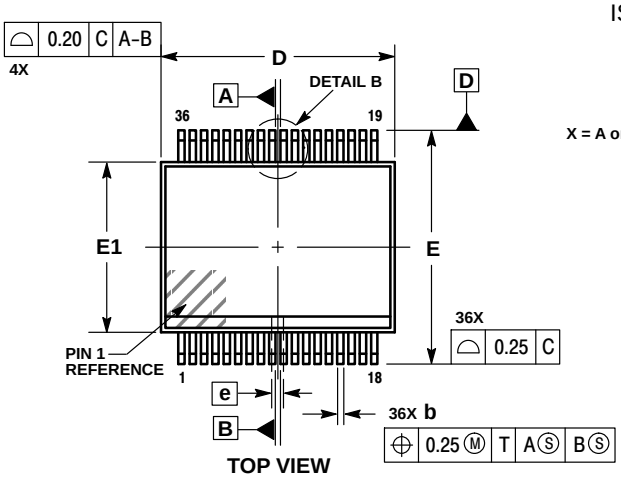


DIMENSIONS: MILLIMETERS

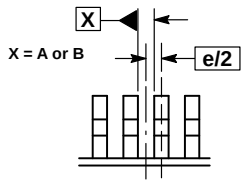
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

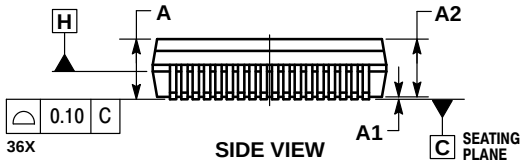
SSOP36 EP
CASE 940AB
ISSUE A



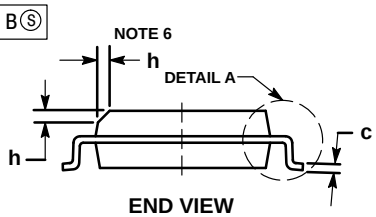
TOP VIEW



DETAIL B



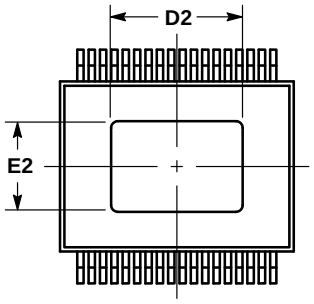
SIDE VIEW



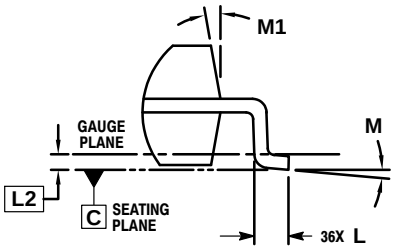
END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE b DIMENSION AT MMC.
4. DIMENSION b SHALL BE MEASURED BETWEEN 0.10 AND 0.25 FROM THE TIP.
5. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. DIMENSIONS D AND E1 SHALL BE DETERMINED AT DATUM H.
6. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, A PIN ONE IDENTIFIER MUST BE LOACATED WITHIN THE INDICATED AREA.

	MILLIMETERS	
DIM	MIN	MAX
A	---	2.65
A1	---	0.10
A2	2.15	2.60
b	0.18	0.30
c	0.23	0.32
D	10.30 BSC	
D2	5.70	5.90
E	10.30 BSC	
E1	7.50 BSC	
E2	3.90	4.10
e	0.50 BSC	
h	0.25	0.75
L	0.50	0.90
L2	0.25 BSC	
M	0°	8°
M1	5°	15°

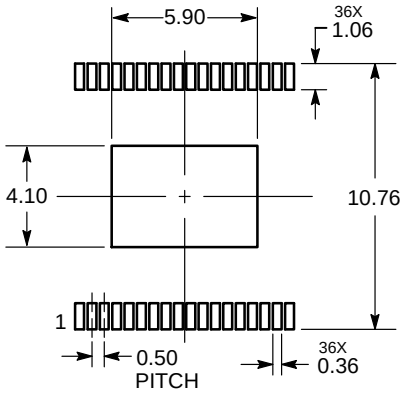


BOTTOM VIEW



DETAIL A

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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