NCP4060

High Voltage Synchronous Buck Converter

The NCP4060 is a high performance, high voltage, high efficiency, fully integrated, voltage−mode synchronous buck converter with constant frequency voltage mode control with input feedforward architecture. It operates from input voltages ranging from 16 V to 80 V and it is capable of generating output voltages down to 1.25 V at 6 A DC loads and up to 10 A peak load currents, across a wide range of ambient temperatures. The NCP4060 exhibits protection features that protect the load from faults like over−voltage, over−current and over−temperature. The NCP4060 adopts a ±1% accurate reference voltage to maintain a tight−regulated output voltage. It has a programmable switching frequency that can be set from 100 to 500 kHz.

Features

- Wide Input Voltage Range from 16 V to 80 V
- Output Current Handling: 6 A
- 1.25 V Internal Reference Voltage Accurate to within ±1% over the Entire Temperature Range
- Programmable Switching Frequency from 100 to 500 kHz
- Externally Programmable Soft−start
- Auxiliary Bootstrap LDO from Output to Reduce Powerloss
- External Error Amplifier Compensation
- Lossless High−side and Low−side FET Current Sensing
- Over−current Protection
- Voltage Mode Control with Input Voltage Feed−forward
- Power Good Output
- Programmable VIN UVLO
- Supports Prebias Start−ups
- Over and Under−voltage Protection
- Internal Over−temperature Protection
- Hiccup Mode Operation for All Faults
- 20 Pin 6 mm x 6 mm QFN Package

Typical Application

- Remote Radio Unit (RRU)
- Telecom and Datacom Applications
- High Voltage Point of Load

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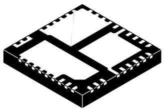


QFN20
CASE 485FC

MARKING DIAGRAM

A = Assembly Lot
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP4060MNTXG	QFN20 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

September, 2017 − Rev. 2

Publication Order Number:
NCP4060/D

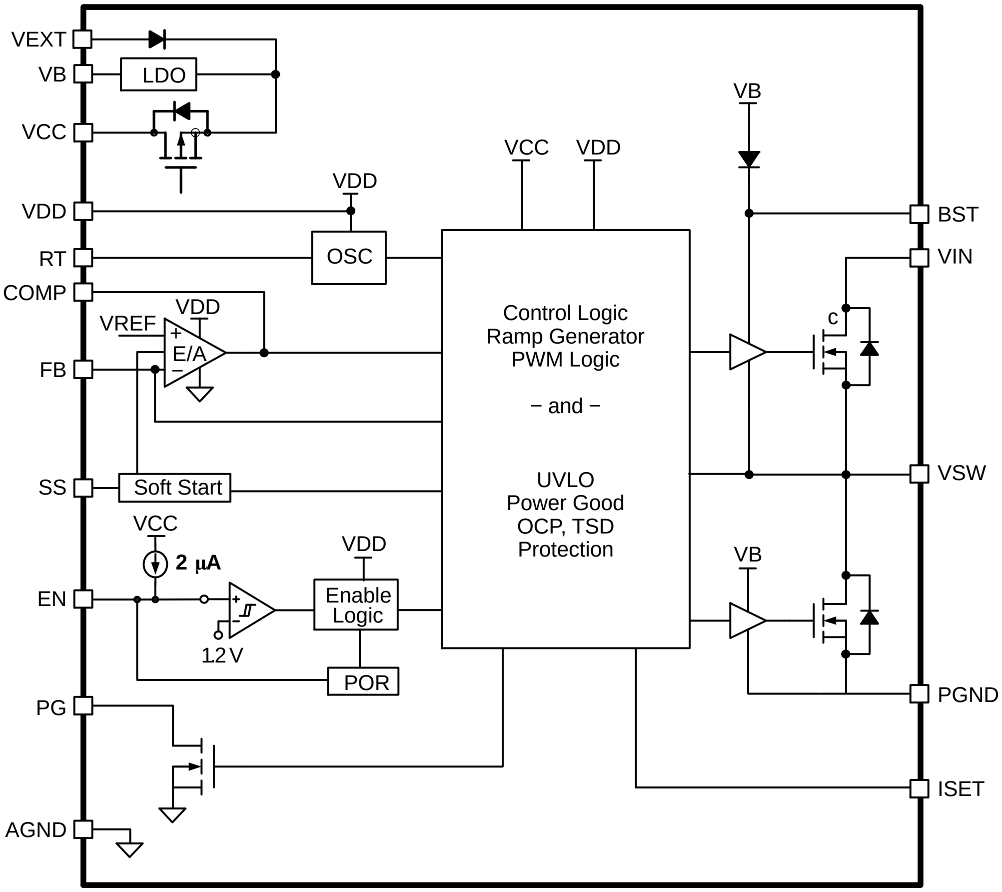


Figure 1. Internal Block Diagram

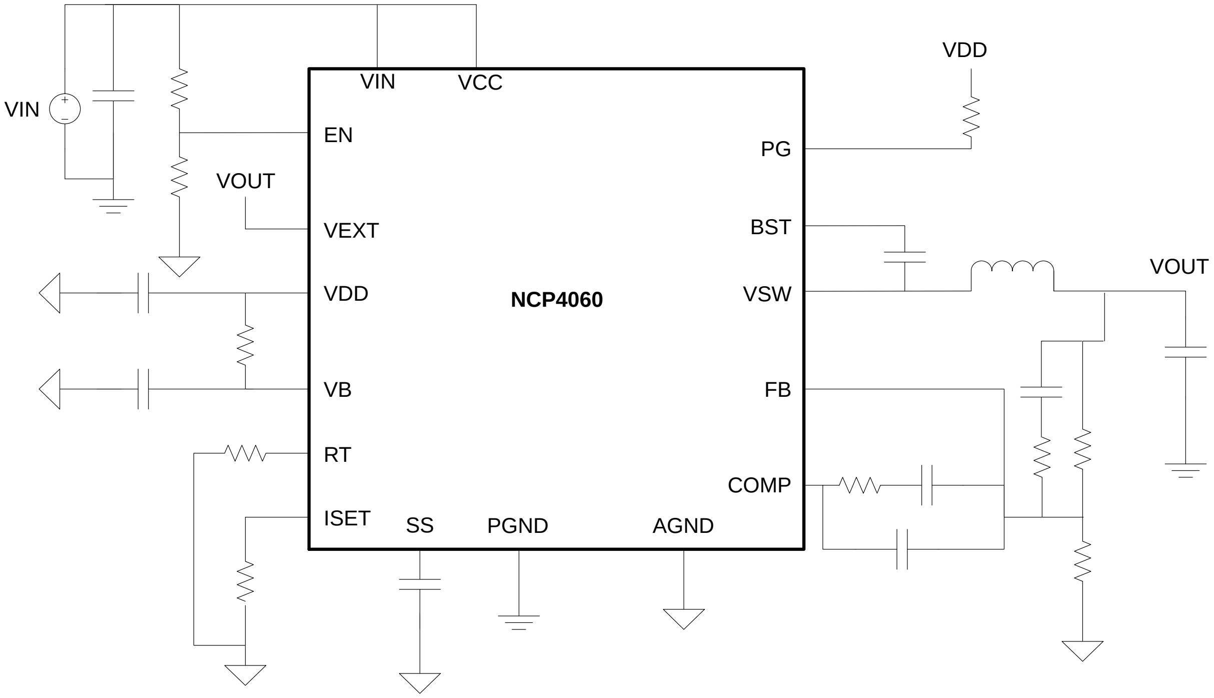


Figure 2. Typical Application Circuit

PIN CONNECTIONS

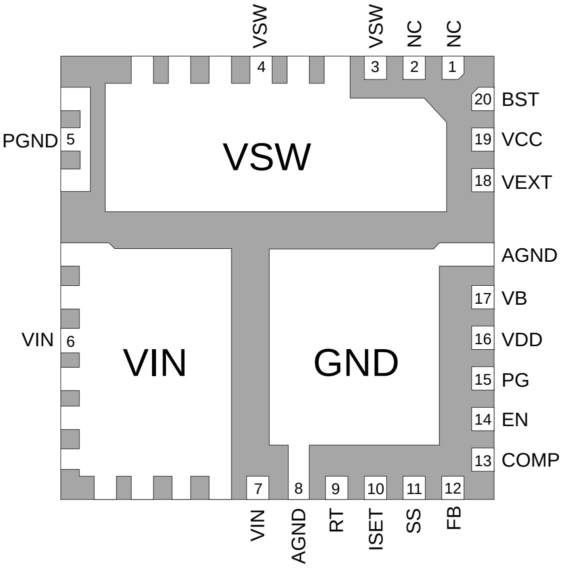


Table 1. PIN DESCRIPTION

Pin No.	Symbol	Description
1	NC	No Connect
2	NC	No Connect
3−4	VSW	The VSW pin is connected to the drain of the low−side MOSFET and the source of the high−side MOSFET.
5	PGND	Power ground reference
6−7	VIN	The VIN pin is connected to the drain of high−side MOSFET. Decouple this pin to PGND by placing decoupling capacitors close to the IC
8	AGND	Analog ground
9	RT	A resistor from RT to AGND sets the switching frequency
10	ISET	A resistor from ISET pin to AGND sets the over−current protection (OCP) threshold
11	SS	A capacitor from SS pin to AGND allows the user to adjust the soft−start ramp time
12	FB	Connect FB to the center tap of external resistor divider to set the output voltage
13	COMP	Error Amplifier Output
14	EN	When used as EN pin, float or drive this pin to > 1.2 V to enable the part; pull to ground to disable; for standby mode, drive this pin to a voltage between 0.8 V & 1 V. To implement VIN UVLO, and set the input voltage at which the part turns on, add a resistor divider from VIN to PGND, and connect the center−tap to EN.
15	PG	Power good indicator of the output voltage. Open−drain output. Connect PG to VDD with an external resistor
16	VDD	Analog input bias voltage. Connect to VB. Connect a 4.7 μF ceramic capacitor from VDD to AGND
17	VB	5.25 V LDO output and MOSFETs driver supply pin for NCP4060. Bypass VB by 4.7 μF ceramic capacitor to AGND.
18	VEXT	Output voltage is connected to this pin to enable LDO switch−over scheme to reduce power consumption. If LDO switch−over scheme is not needed, tie VEXT to AGND.
19	VCC	VCC input voltage for the LDO. Connect to VIN.
20	BST	High−side MOSFET driver input supply, a bootstrap capacitor connection between the switch node and this pin

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Power Supply to PGND		V_{IN}, V_{CC}	−0.3 to 100	V
V_{SW} to PGND	DC	V_{SW}	−1 to 100	V
	Repetitive pulse < 100 ns		−10 to 100	
BST to SW		BST	−0.3 to 6	V
VEXT to PGND		VEXT	−0.3 to 80	V
All other pins			−0.3 to 6.0	V
AGND to PGND		AGND, PGND	−0.3 to 0.3	V
Electrostatic Discharge Human body model		HBM	2000	V
Electrostatic Discharge Charge device model		CDM	1500	V
Operating Ambient Temperature Range		T_A	−40 to +125	°C
Operating Junction Temperature Range		T_J	−40 to +125	°C
Maximum Junction Temperature		$T_{J(MAX)}$	+150	°C
Storage Temperature Range		T_{stg}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. THERMAL INFORMATION

HS FET Junction−to−case thermal resistance (Note 1)	$R_{\theta JA-HS}$	25	°C/W
LS FET Junction−to−case thermal resistance (Note 1)	$R_{\theta JA-LS}$	26	
μC Junction−to−Ambient thermal resistance (Note 1)	$R_{\theta JA-Controller}$	27	
Junction−to−case characterization parameter	Ψ_{JC}	0.5	

1. $R_{\theta JC}$ thermal resistance is obtained by simulating a cold plate test on the exposed power pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30−88.

Table 4. RECOMMENDED OPERATING CONDITIONS (over operating free−air, unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply to PGND	V_{IN}, V_{CC}	−0.3 to 80	V
VSW to PGND	VSW	−1 to 80	V
BST to SW	BST	−0.6 to 5.5	V
VEXT to PGND	VEXT	−0.3 to 60	V
AGND to PGND	AGND	0	V
All other pins		−0.3 to 5.5	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS (−40°C < T_J = T_A < +125°C, V_{IN} = V_{CC} = 48 V, for min/max values unless otherwise noted, T_A = T_J = +25°C for typical values, VB = VDD, VEXT = 0 V)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V_{IN} Operation Voltage	V_{IN}		16		80	V
V_{CC} Operation Voltage	V_{CC}		16		80	V
VB Output Voltage	VB		5.0	5.25	5.6	V
VB Dropout voltage		IB = 5 mA		0.6	1.8	V
VB Current Limit		V_{CC} = 48 V		117		mA
VDD UVLO Threshold (Rising)			4.3	4.6	4.8	V
VDD UVLO Hysteresis				0.4		V
V_{CC} Quiescent Current		EN = H, COMP = L, PG open; VIN = VCC = 48 V, Fsw = 300 kHz		5.5	10	mA
Shutdown Supply Current		EN = 1 V; VIN = VCC = 48 V; PG open		700		µA
		EN = 0 V; VIN = VCC = 48 V; PG open		160		µA
FEEDBACK VOLTAGE						
FB input voltage	VFB	T_J = 25°C, 16 V ≤ V_{CC} ≤ 80 V	1.24	1.25	1.26	V
		−40°C ≤ T_J ≤ 125°C; 16 V ≤ V_{CC} ≤ 80 V	1.237	1.25	1.262	
Feedback Input Bias Current	IFB	VFB = 1.25 V		100	120	nA
ERROR AMPLIFIER						
Open Loop DC Gain (GBD)			60	85		dB
Open Loop Unity Gain Bandwidth	F0dB, EA			24		MHz
Open Loop Phase Margin				60		deg
Slew Rate		COMP pin to GND = 10 pF		2.5		V/µs
COMP Clamp Voltage, High				3.4		V
Output Source Current		VFB = 0 V	6			mA
Output Sink Current		VFB = 1.5 V	17			mA
CURRENT LIMIT						
Low−side $R_{DS(on)}$/ISET	$R_{DS(on)}$/ISET	Guaranteed by characterization, T_A = 25°C		440		Ω/A
Low−side ISET Current Source Temperature Coefficient	TC_LS_ISET			+0.36		%/°C
Low−side OCP switch−over threshold		Guaranteed by design		0.6		V
Low−side Fixed OCP threshold	LS_OCPth	Guaranteed by design		150		mV
Low−side programmable OCP range	LS_OCPth	Guaranteed by design			<600	mV
LS OCP Blanking time	LS_Tblnk	Guaranteed by design		150		ns
High−side OCP	HS_OCP	Guaranteed by characterization		2xLS_OCP		A
PWM						
Minimum OFF−Time				330		ns
Minimum duty cycle		VCOMP < PWM Ramp Offset Voltage		8		%
Minimum ON−Time				50		ns
PWM Ramp Amplitude		16 V ≤ V_{IN} ≤ 80 V		V_{IN}/30		V
PWM Ramp Offset				0.18		V

Table 5. ELECTRICAL CHARACTERISTICS (−40°C < T_J = T_A < +125°C, V_{IN} = V_{CC} = 48 V, for min/max values unless otherwise noted, T_A = T_J = +25°C for typical values, VB = VDD, VEXT = 0 V)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
OSCILLATOR						
Programmable Switching frequency range		16 V < V_{CC} < 80 V	100		500	kHz
Switching frequency	f_{sw}	RT = 120 KΩ, 16 V < V_{CC} < 80 V		100		kHz
		RT = 40 KΩ, 16 V < V_{CC} < 80 V	270	300	330	kHz
		RT = 23 KΩ, 16 V < V_{CC} < 80 V		500		kHz
Hiccup Timer	t_{hiccup}	fsw = 500 kHz		4 x tss		ms
LDO SWITCHOVER						
LDO switch−over threshold		V_{OUT} = V_{EXT}	>7.2			V
LDO switch−over threshold hysteresis				0.90		V
ENABLE INPUT (EN)						
Enable Threshold Voltage	V_EN	VEN rising	1.13	1.2	1.27	V
Enable Hysteresis		VEN falling		190		mV
Deep Disable Threshold				0.82	1.1	V
Enable Pull−up Current				2.5		μA
SOFTSTART INPUT (SS)						
SS Startup Delay	t_{SSD}	Time from EN going high to time before SS starts to ramp		1.52		ms
SS End Threshold	SSEND			1.3		V
SS Source Current	ISS		2	3	4	μA
VOLTAGE MONITOR						
Power Good Sink Current		PG = 0.15 V	5.0	9.2		mA
Output Over-voltage Trip Threshold			1.575	1.625		V
Overvoltage Fault Blanking Time				4		μs
Output Under−Voltage Trip Threshold				0.875	0.925	V
Under−voltage Protection Blanking Time				20		μs
POWER STAGE						
High−side On Resistance	RDSONH	I_D = 2 A		20	38	mΩ
Low−side On Resistance	RDSONL	I_D = 2 A		22	38	mΩ
VFBOOT		I_{BOOT} = 2 mA		60		mV
THERMAL SHUTDOWN						
Thermal Shutdown Threshold		Guaranteed by Characterization		150		°C
Thermal Shutdown Hysteresis		Guaranteed by Characterization		25		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. The LDO, VIN And Oscillator Frequency Blocks are tested at 48 V. All other blocks tested at 12 V.

TYPICAL CHARACTERISTICS

V_{IN} = 48 V, V_{OUT} = 5 V, C_{OUT} = 5 x 10 μF, L = 15 μH, F_{SW} = 300 kHz, T_A = +25°C, unless otherwise noted.

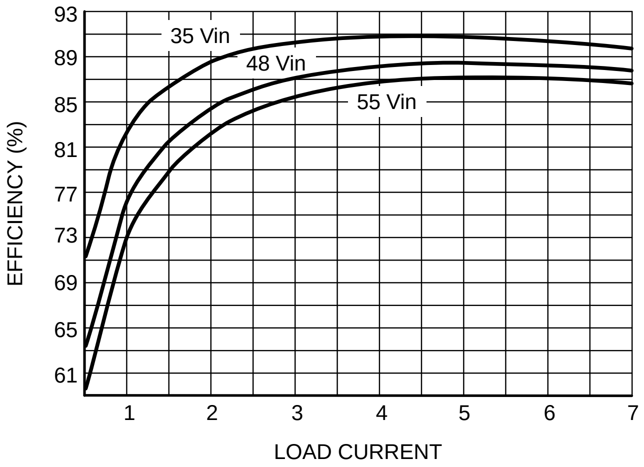


Figure 3. Efficiency vs. Load Current
V_{OUT} = 5 V

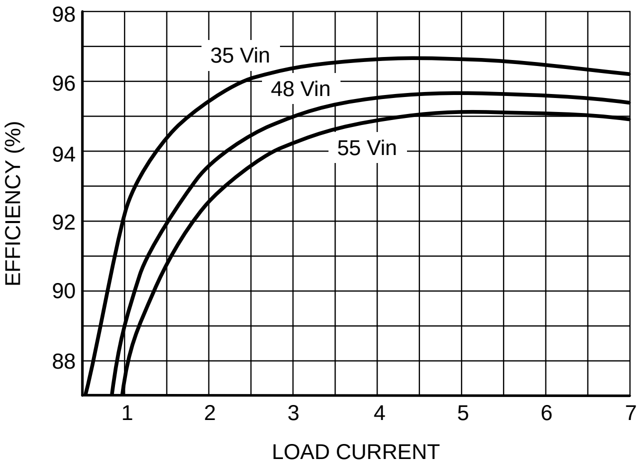


Figure 4. Efficiency vs. Load Current
V_{OUT} = 12 V

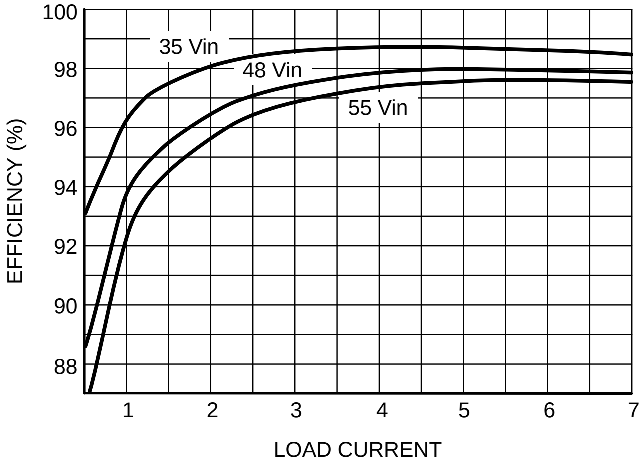


Figure 5. Efficiency vs. Load Current
V_{OUT} = 24 V

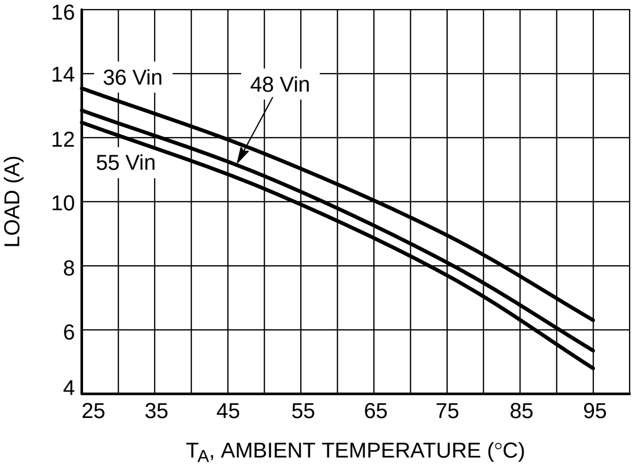


Figure 6. Thermal Derating
V_{OUT} = 5 V

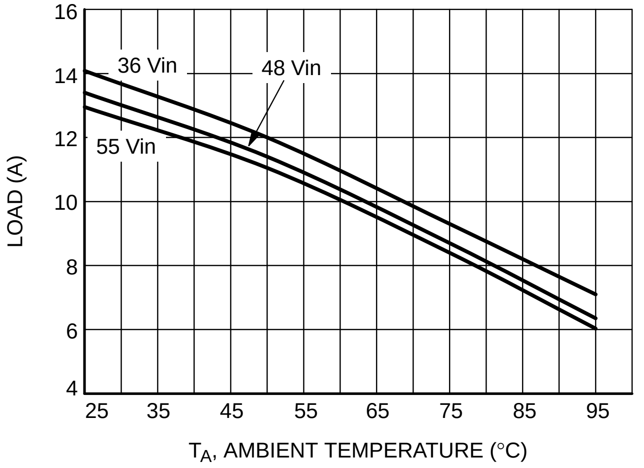


Figure 7. Thermal Derating
V_{OUT} = 12 V

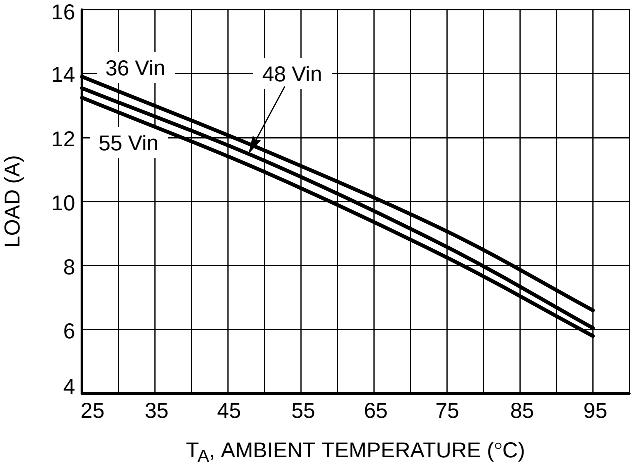


Figure 8. Thermal Derating
V_{OUT} = 24 V

TYPICAL CHARACTERISTICS

V_{IN} = 48 V, V_{OUT} = 5 V, C_{OUT} = 5 x 10 μF, L = 15 μH, F_{SW} = 300 kHz, T_A = +25°C, unless otherwise noted.

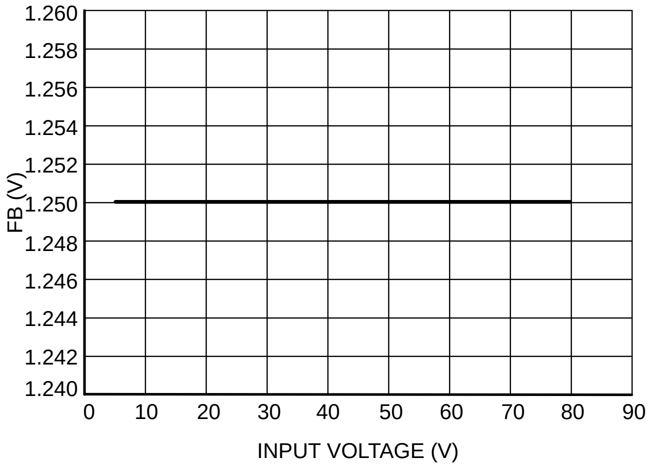


Figure 9. FB vs. Vin

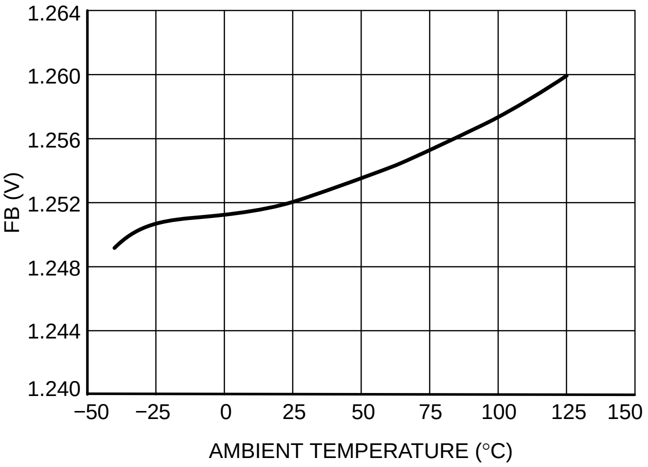


Figure 10. FB vs. $T_{ambient}$

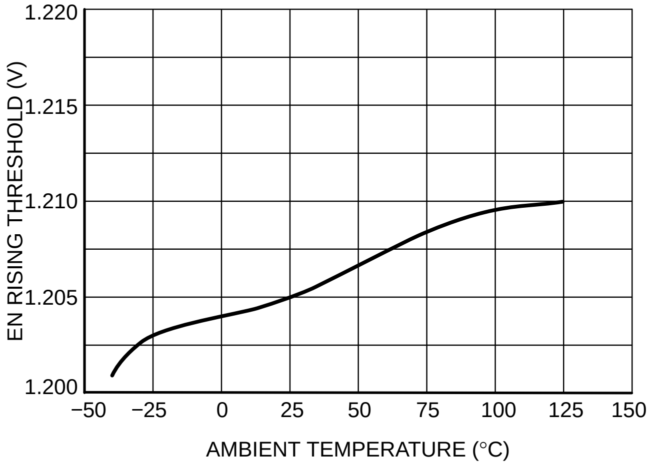


Figure 11. EN Rising Threshold vs. $T_{ambient}$

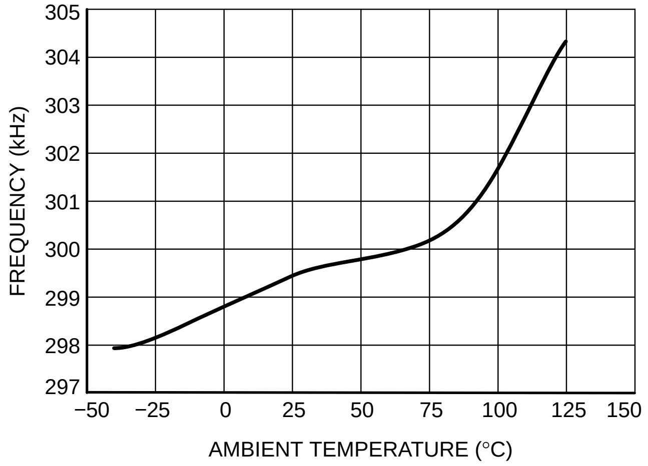


Figure 12. Frequency vs. $T_{ambient}$

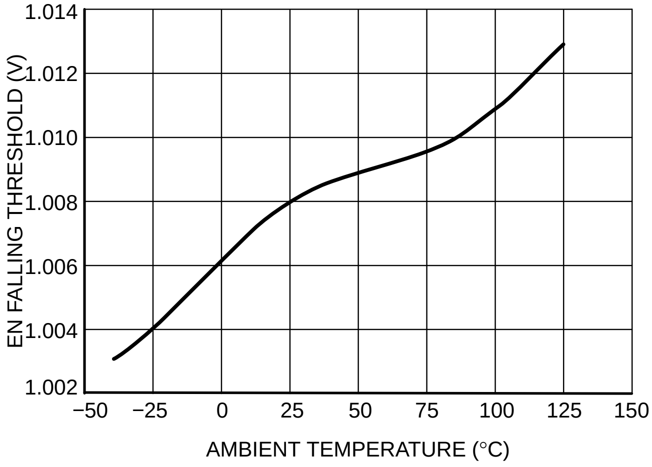


Figure 13. EN Falling Threshold vs. $T_{ambient}$

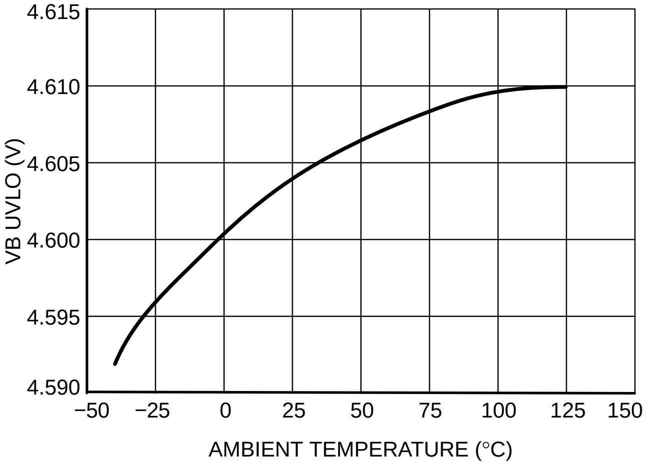


Figure 14. VB UVLO vs. $T_{ambient}$

TYPICAL CHARACTERISTICS

V_{IN} = 48 V, V_{OUT} = 5 V, C_{OUT} = 5 x 10 μF, L = 15 μH, F_{SW} = 300 kHz, T_A = +25°C, unless otherwise noted.

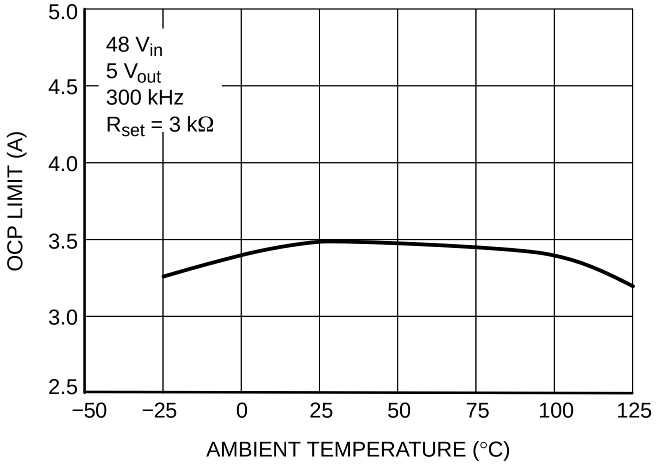


Figure 15. OCP Limit vs. $T_{ambient}$

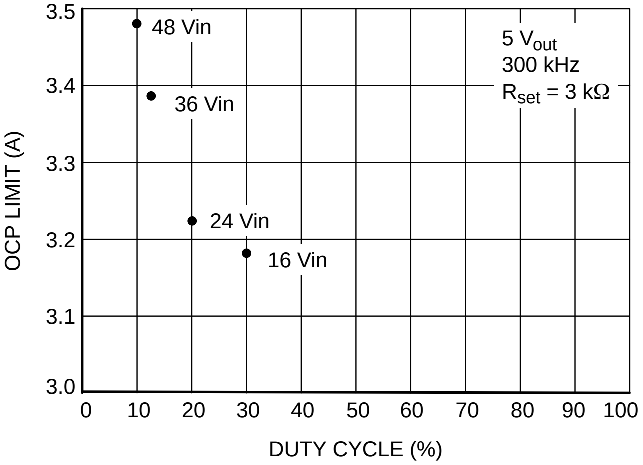


Figure 16. OCP Limit vs. Duty Cycle

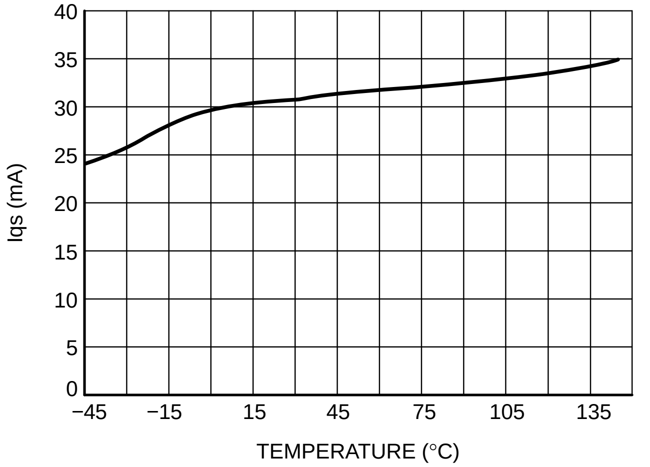


Figure 17. VIN Quiescent Current vs. $T_{ambient}$

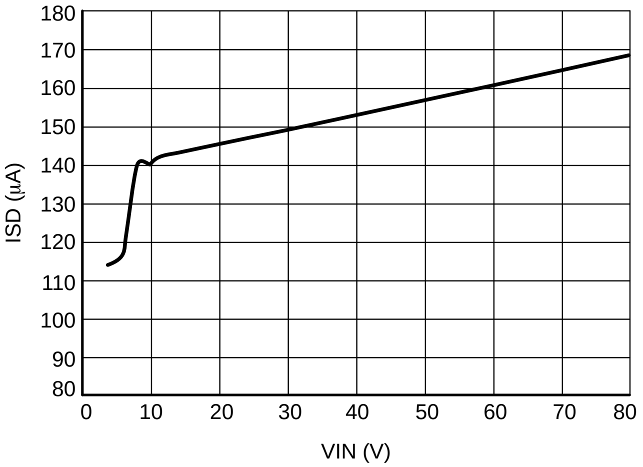


Figure 18. Shutdown Current vs. VIN

FUNCTIONAL CHARACTERISTICS

V_{IN} = 48 V, V_{OUT} = 5 V, F_{SW} = 300 kHz, L = 15 μH, C_{OUT} = 5 x 10 μF.

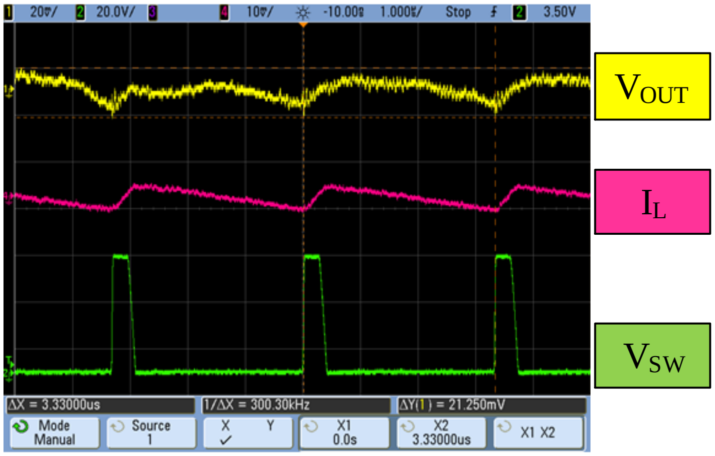


Figure 19. Steady State Operation at No Load

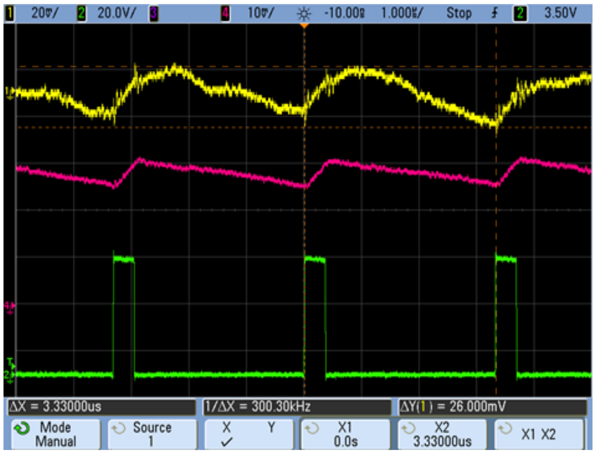


Figure 20. Steady State Operation at 6A Load

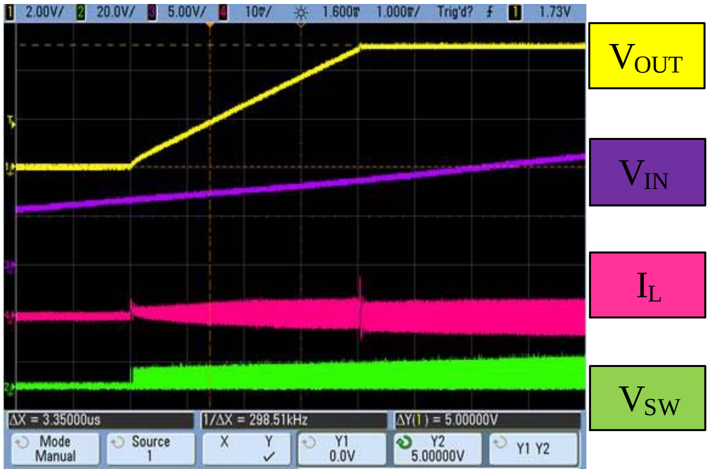


Figure 21. Start−Up Transition at No Load

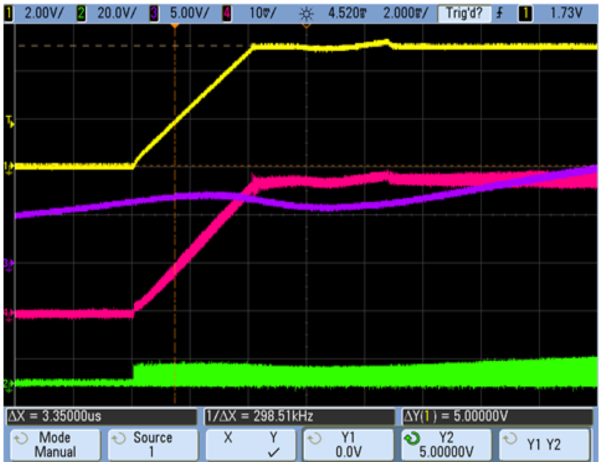


Figure 22. Start−Up Transition at 6A Load

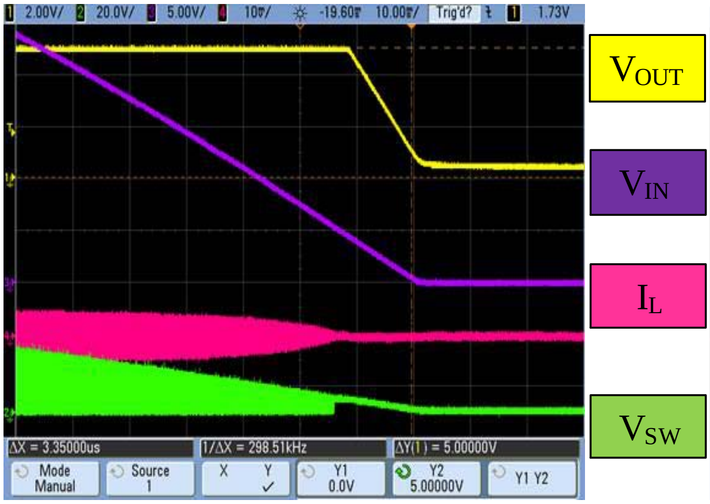


Figure 23. Shut−Down Transition at No Load

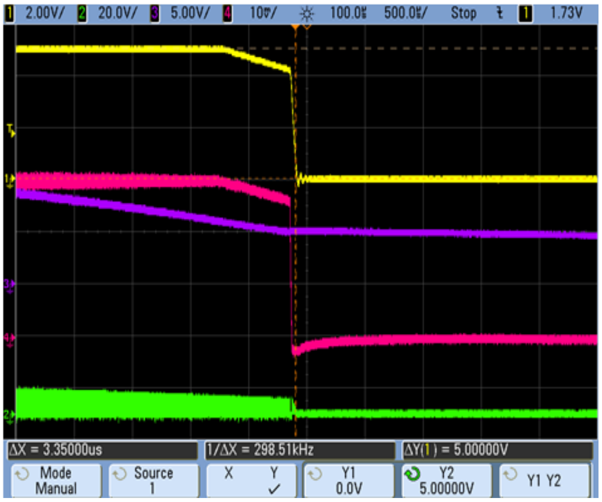


Figure 24. Shut−Down Transition at 6A Load

FUNCTIONAL CHARACTERISTICS

V_{IN} = 48 V, V_{OUT} = 5 V, F_{SW} = 300 kHz, L = 15 μH, C_{OUT} = 5 x 10 μF.

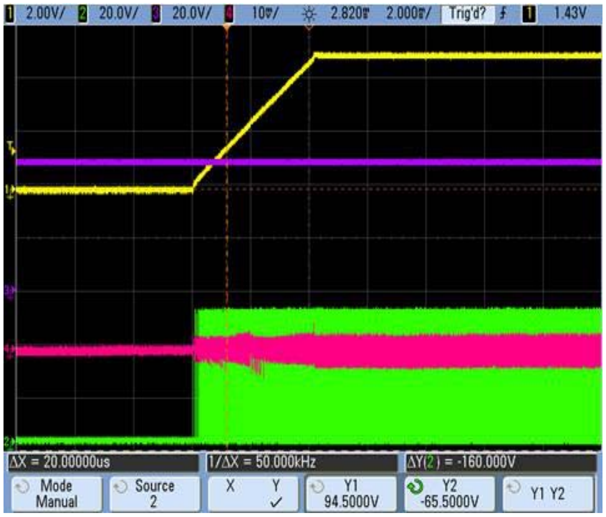


Figure 25. Start−Up Transition at No Load (EN = High)

V_{OUT}

V_{IN}

I_L

V_{SW}

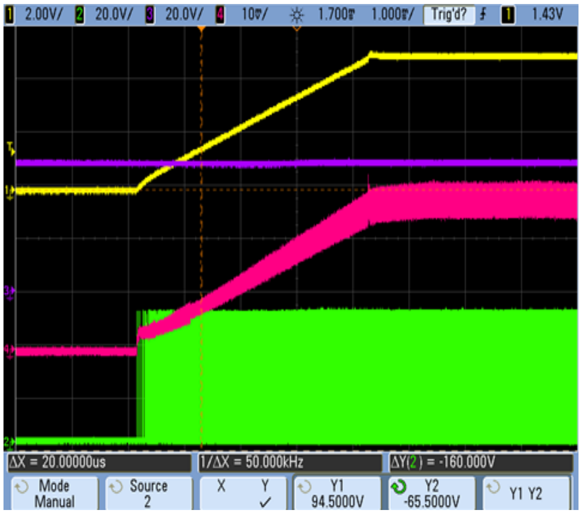


Figure 26. Start−Up Transition at 6A Load (EN = High)

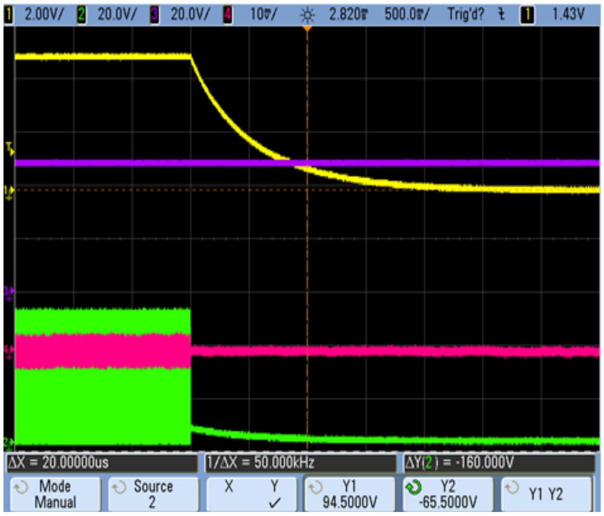


Figure 27. Shut−Down Transition at No Load (EN = Low)

V_{OUT}

V_{IN}

I_L

V_{SW}

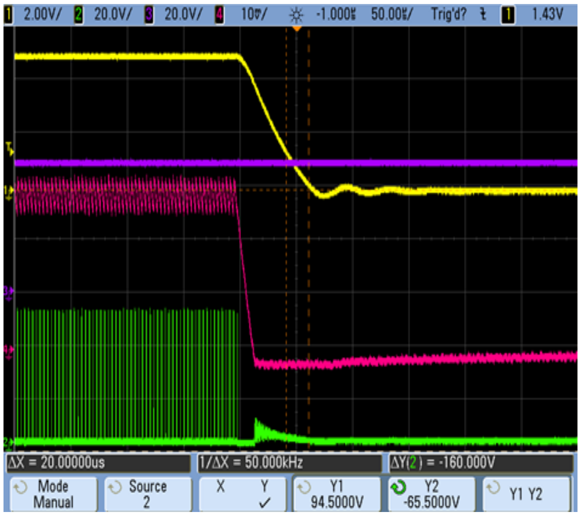


Figure 28. Shut−Down Transition at 6A Load (EN = Low)

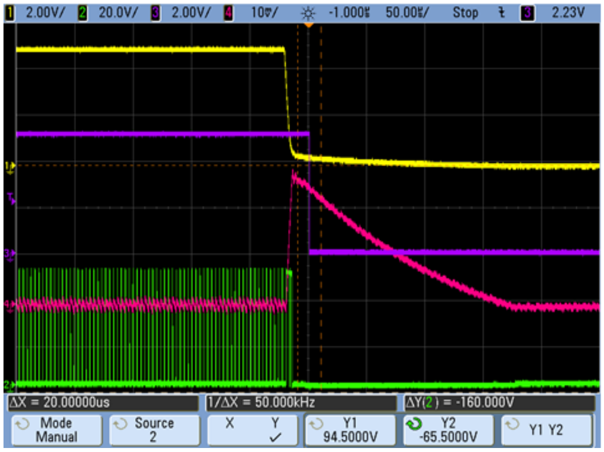


Figure 29. Short Circuit Test at No Load

V_{OUT}

P_{Gd}

I_L

V_{SW}

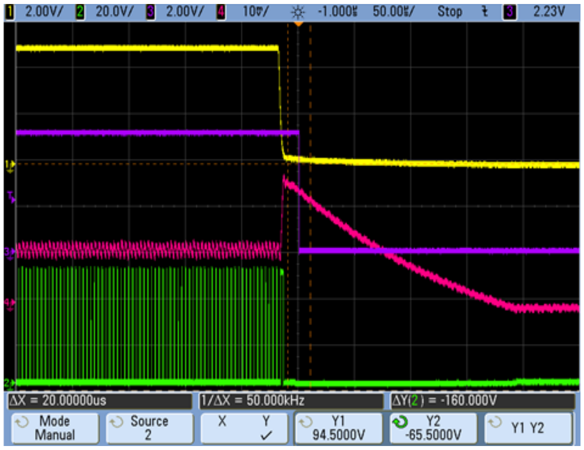
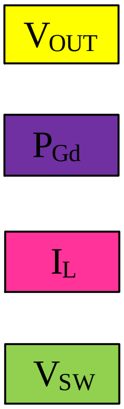


Figure 30. Short Circuit Test at 6A Load

FUNCTIONAL CHARACTERISTICS

V_{IN} = 48 V, V_{OUT} = 5 V, F_{SW} = 300 kHz, L = 15 μH, C_{OUT} = 5 x 10 μF.

Figure 31. Recovery transition from Output Short at No Load



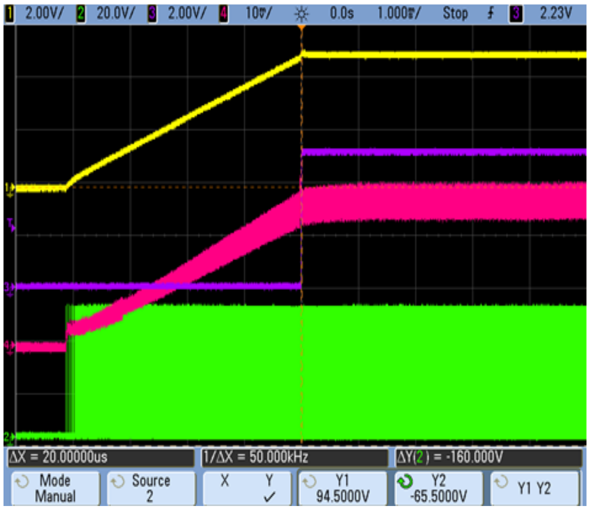


Figure 32. Recovery transition from Output Short at 6A Load

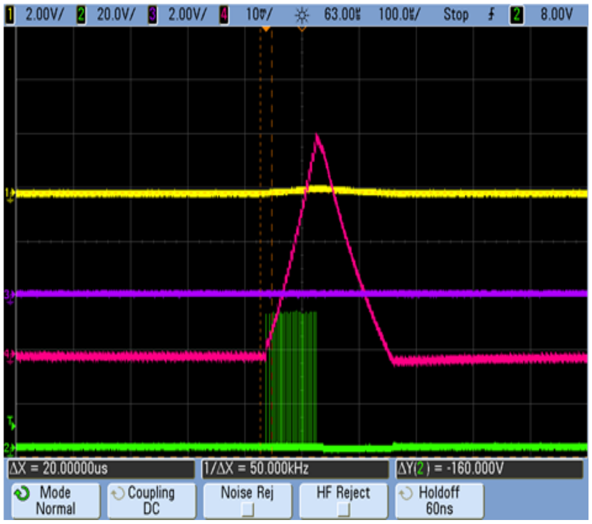
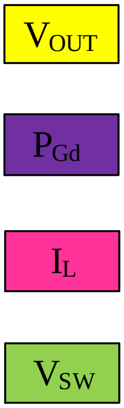


Figure 33. Power−Up by toggling EN with Output Short



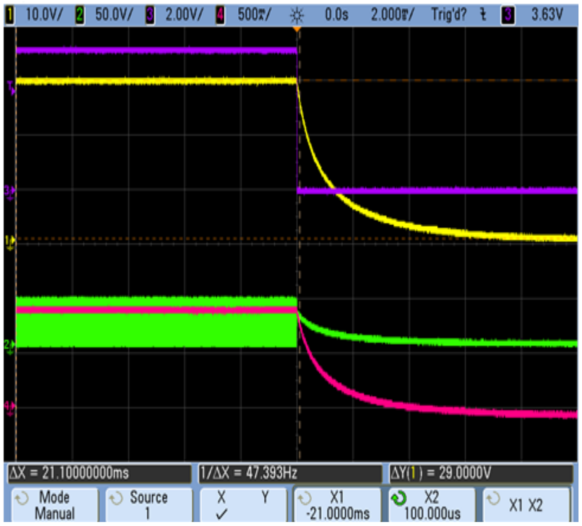


Figure 34. NCP4060 entering OTP

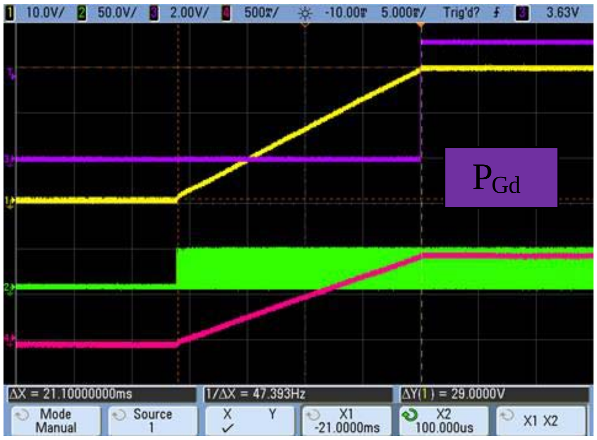


Figure 35. NCP4060 recovering from OTP

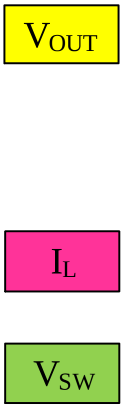


Figure 36. Start−Up with Pre−Biased Output

APPLICATION INFORMATION

Overview

The NCP4060 is a high voltage, high efficiency, PWM synchronous buck converter. It operates from input voltages ranging from 16 V to 80 V. The NCP4060 is capable of delivering 6 A DC load currents up to 10 A peak load currents. Its switching frequency is user programmable from 100 kHz to 500 khz. The NCP4060 utilizes voltage mode control with voltage feed−forward to respond swiftly to input voltage changes.

The NCP4060 has a complete set of protection features including high−side FET overcurrent protection (HSOCP), low−side FET overcurrent protection (LSOCP), output over and under voltage protection (OVP, UVP), and thermal shutdown. The enable function is highly programmable to allow for adjustable startup voltages at higher input voltages (UVLO). There is also an adjustable soft−start and open−drain power good signal.

Reference Voltage

The NCP4060 incorporates a highly accurate internal reference of 1.25 V. The accuracy of the reference is guaranteed within 1.5% over the entire operating temperature range of the controller.

Oscillator

The NCP4060 has a programmable switching frequency that covers a range from 100 khz to 500 khz. A resistor from pin 9 (RT) to ground sets the switching frequency. Equation 1 below allows the user to determine the timing resistance for the desired switching frequency. Note that the NCP4060 has a 330 ns minimum OFF time, which would limit the maximum duty cycle at high switching frequency (see Table 6).

$$F = \frac{12 \cdot 10^9}{RT} \qquad \text{(eq. 1)}$$

Table 6. MINIMUM AND MAXIMUM DUTY CYCLES at Various Output Voltages vs. Switching Frequency

	0 to 6 A Load	200 Khz	300 Khz	400 Khz
Vout = 50 V	Max Duty Cycle	89%	89%	85%
Vout = 28 V	Max Duty Cycle	92%	87%	83%
Vout = 12 V	Max Duty Cycle	92%	88%	84%
Vout = 5 V	Min Duty Cycle	8%	8%	10%
Vout = 3.3 V	Min Duty Cycle	8%	8%	10%

Users may also refer to the switching frequency Vs RT Resistance curve to approximate the resistor value.

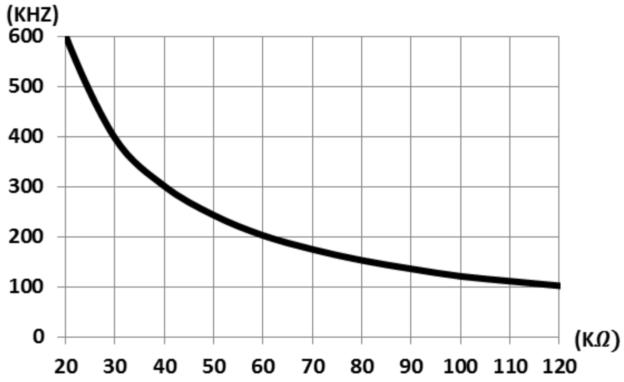


Figure 37. Fsw vs. RT

Ramp

The NCP4060 adopts voltage feed−forward architecture to provide good line regulation over a wide input voltage range. The internal ramp is a saw tooth waveform at the PWM frequency with peak−to−peak amplitude of VIN/30 with an offset of 0.17 V from AGND.

Error Amplifier

The error amplifier's primary function is to regulate the converter's output voltage using a resistor divider connected from the converter's output to the FB pin of the controller, as shown in the Applications Schematic. A type III compensation network must be connected around the error amplifier to stabilize the converter. It has a bandwidth of greater than 24 MHz, with open loop gain of at least 60 dB.

Programmable Soft−Start

An external capacitor connected from the SS pin to ground sets up the soft start period, which can limit the start−up inrush current. The soft start period can be programmed based on the Equation 2. Vref = 1.25 V, Iss = 2.5 μA.

$$t_{SS} = \frac{C_{SS} \cdot V_{ref}}{I_{SS}} \qquad \text{(eq. 2)}$$

OCP is the only fault that is active during a Soft Start.

Adaptive Non−Overlap Gate Driver

In a synchronous buck converter, a certain dead time is required between the low side drive signal and high side drive signal to avoid shoot through. During the dead time, the body diode of the low side FET freewheels the current. The body diode has much higher voltage drop than that of the MOSFET, which reduces the efficiency significantly. The longer the body diode conducts, the lower the efficiency. The NCP4060 implements adaptive dead time control to minimize the dead time and to prevent current shoot through.

Precision Enable (EN)

The ENABLE block allows the output to be toggled on and off and is a precision analog input. When the EN voltage exceeds V_EN, the controller will initiate the soft−start sequence as long as the input voltage and sub−regulated voltage have exceeded their UVLO thresholds. V_EN_hyst helps to reject noise and allows the pin to be resistively coupled to the input voltage or sequenced with other rails.

If the EN voltage is held below 0.82 V, the NCP4060 enters a deep disable state where the LDO and internal bias circuitry are off. As the voltage at EN continues to rise, the Enable comparator and reference are active and provide a more accurate EN threshold. The drivers are held off until the rising voltage at EN crosses V_EN.

An internal 2.5 μA pull−up automatically enables the device when the EN pin is left floating.

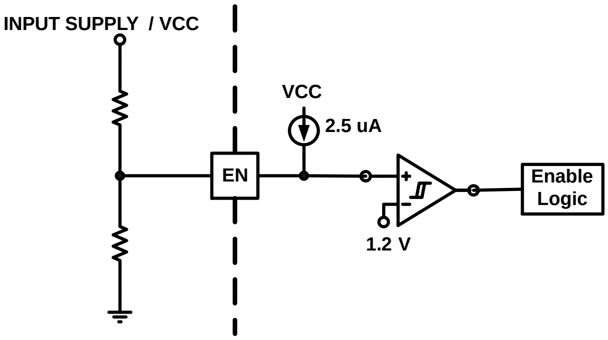


Figure 38. Enable Functional Block Diagram

It is highly recommended to implement a voltage divider between VIN and the EN pin when working with high output voltages to ensure that the part powers up successfully without triggering UVP as Vin ramps up to its final value. The figure below portrays an example of such case.

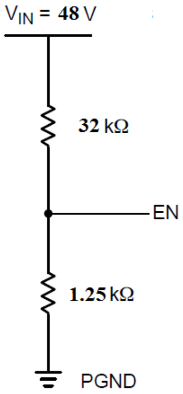


Figure 39. Voltage Divider between VIN and EN for a 48 V_{IN} / 24 V_{OUT} Buck

LDO Switch−over Scheme

To reduce power dissipation and increase efficiency, the NCP4060 adopts a novel LDO switch−over scheme. The LDO is typically supplied by the HV VCC pin and its output (VB) along with VDD which biases all the internal blocks. When operating at higher VIN/VCC ranges, a portion of the power dissipation happens across the HV LDO. To reduce this power dissipation, the user has an option to bootstrap the output of the regulator (VOUT) to the input of the LDO through the VEXT pin.

To utilize this feature, the user must connect the VEXT pin to the output of the regulator and the output voltage should be programmed to be greater than 7.2 V. Under this configuration, once the part is enabled, by default the LDO is supplied by the VCC pin. After soft−start is complete and regulation is established, an internal switch−over circuitry senses the output voltage. if VOUT is greater than 7.2 V then it switches the input supply of the LDO from VCC to VEXT. The switchover circuitry has about 0.9 V hysteresis to make sure there is no chattering or any other undesirable effects during the switch−over process. If VOUT is programmed to < 7.2 V, the LDO continues to be powered by VCC. If the switchover feature is not desired, user must connect VEXT to ground.

There may be cases where an external power supply is utilized to bias the VEXT pin instead of VOUT. This is possible, granted the correct sequencing of VCC/VIN & VEXT pins is done properly.

Under any circumstances, VEXT voltage cannot exceed VCC/VIN by 0.3 V. If this maybe a possible scenario, to protect the part, an external blocking diode is necessary between VIN and VCC to prevent VEXT back charging the supply VIN.

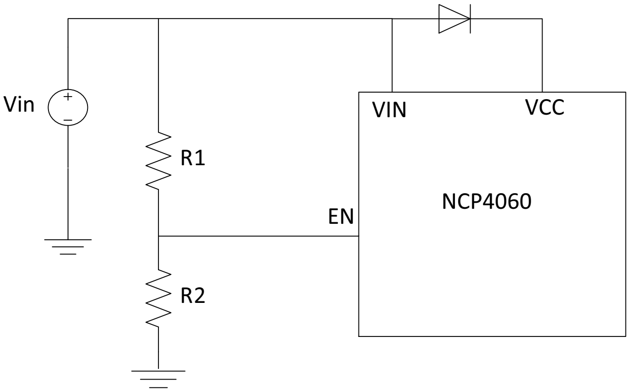


Figure 40. Input Blocking Diode for VEXT > VCC

Pre−Bias Startup

Some applications require the controller to initiate a startup sequence when the output retains its charge from a little above 0 V to just below the regulated output voltage. This particular situation can happen when the converter’s output capacitors have residue charge or the converter’s output is held up by a low current standby power supply. The NCP4060 supports pre−bias conditions by maintaining a smooth startup during a condition where the output voltage is present. However if the pre−bias voltage is higher than the set regulated voltage, switching does not occur until the output drops below the regulated value.

PROTECTION FEATURES

Hiccup Mode

The NCP4060 utilizes hiccup mode for all of its fault conditions. Upon entering hiccup mode after a fault detection, the NCP4060 turns off the high side and low side FET's and pulls PG low. It waits for tHICCUP ms before reinitiating a soft−start. tHiccup is defined as four soft start timeouts (tss). The equation for tss is shown in Equation 2. OCP is the only active fault detection during the hiccup mode soft start.

Over−Voltage Protection (OVP)

When the voltage at the FB pin goes above 1.625 V for greater than 5 μs (typical), an OVP fault is set and PG is asserted low. The high side FET will turn off and the low side FET will turn on. Once VFB falls below the Under−voltage Protection Threshold then the device enters hiccup mode.

Under−Voltage Protection (UVP)

An Under−voltage protection circuit monitors the VFB voltage to detect an under voltage event. When the VFB voltage drops below 0.875 V for longer than 20 μs, a UVP fault is set and the device will enter hiccup mode. UVP fault monitoring is disabled during soft start condition.

Over Current Protection (OCP)

The NCP4060 implements an overcurrent protection scheme based on lossless Low−side & High−side MOSFET current sensing.

During the OFF−time, the current circulating in the low−side FET creates a voltage drop across its Rdson, that Drain to Source voltage is measured and compared against the voltage of an internal temperature compensated current source on the ISET pin and a user selected RSET. When the Low−side OCP detects a fault, it will prevent the high−side from turning on until the low−side OCP drops below its trip point. Then, the high−side FET turns back on in the next clock cycle thus enabling a pulse skipping behavior. An internal OCP counter will count up to 3 consecutive OCP events within an 8 clock cycle before the NCP4060 goes into hiccup mode.

During high duty cycles, off times are small and due to the 150 ns blanking time the low−side OCP could miss detecting a fault. The role of the high−side OCP is to terminate an ON−time pulse when it detects a fault. The high−side OCP senses the current in the high−side FET, the drain to source voltage drop is compared against a preset reference voltage. The trip point of the high side OCP is two times that of the Low−side OCP.

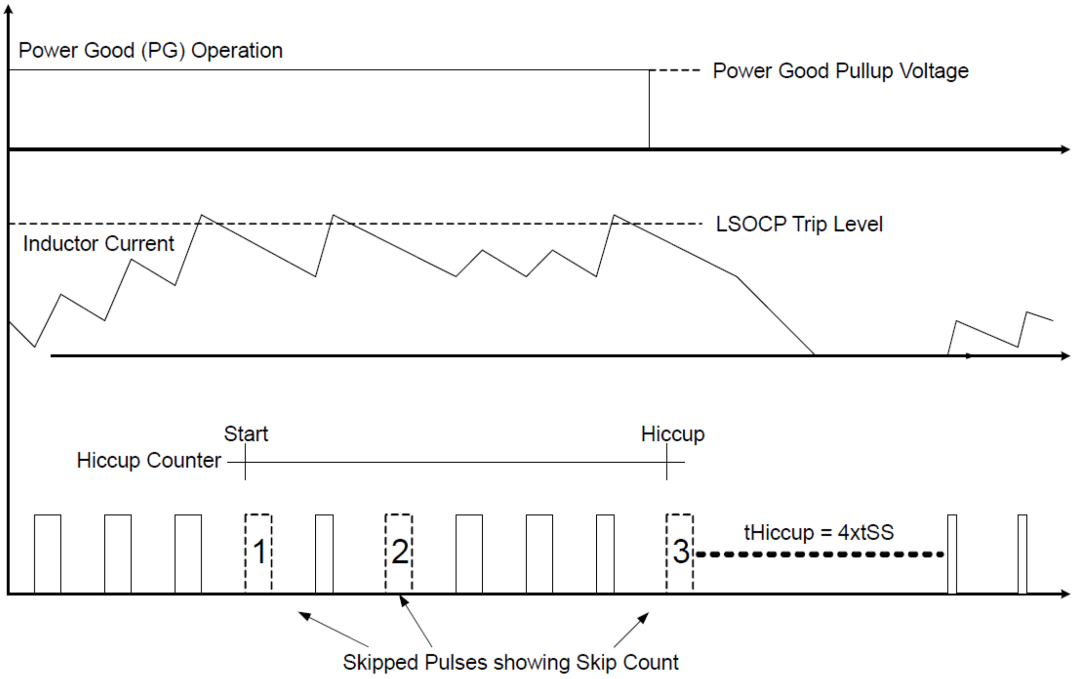


Figure 41. Description of LSOCP Block

The Scope shot below showcases a low side OCP event where channel 2 represents the inductor current and channel 1 the switch node. The NCP4060 samples the current through the Low side MOSFET's Rdson. When the peak current reached 3.2 A it captured a fault, forced the regulator to skip an On−time Pulse. Then, turned the Low−side MOSFET On to discharge the current in the inductor causing it to drop below its trip point which forced a high side turn−on and created the pulse skipping behavior described in the previous section. Once the NCP4060 registered 3 faults within 8 clock cycles it entered hiccup mode.

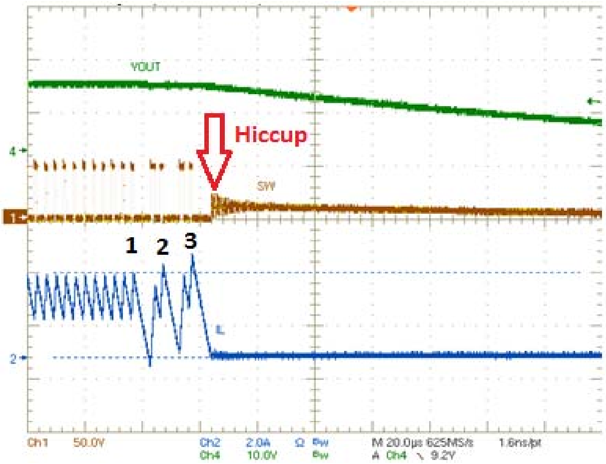


Figure 42. LSOCP Event

Over Current Protection Threshold (ISET)

The NCP4060 allows the user to adjust the LSOCP threshold with an external resistor, RSET. This resistor, along with an internal temperature compensated current source, ISET, sets the current limit reference voltage for the LSOCP comparator.

Internally, a current sense circuit samples the voltage cycle by cycle from VSW to GND. This voltage drop is then multiplied by a factor of 2X and compared against the ISET*RSET voltage threshold.

The basic design equation for LSOCP trip point selection is:

$$\mathrm{RSET} = \frac{2 \times \mathrm{Ilim} \times \mathrm{RDSON}}{\mathrm{ISET}} \qquad \text{(eq. 3)}$$

Where Rdson/ISET is 440 ohm/A across the operating ambient temperature range.

In case RSET is not connected, the device switches the OCP threshold to a fixed 150 mV value: an internal safety clamp on ISET is triggered as soon as the ISET voltage crosses 0.62 V, enabling the 150 mV fixed threshold. It is recommended to connect a 0.1 μF capacitor in parallel with Rset to filter any AC coupling on the ISET pin.

Thermal Shutdown (TSD)

The NCP4060 protects itself from overheating with an internal thermal monitoring circuit. If the junction temperature exceeds the thermal shutdown threshold of 150°C the NCP4060 turns both High−side and low−side MOSFETs OFF, PG pulls to ground then enters Hiccup mode. Once the temperature drops below the falling threshold, the part will initiate soft−start.

Power Good Monitor (PG)

NCP4060 monitors the output voltage and signals when the output is out of regulation or during a non−regulated pre−bias condition or fault detection. When the output voltage is within the OVP and UVP thresholds, the power good pin goes in high Z state. If the NCP4060 detects an OCP, OVP, UVP, TSD or is in soft start, it pulls PG pin low. The PG pin is an open drain 8.5 mA pull down output.

COMPONENT SELECTION

Setting the Output Voltage

A resistive voltage divider from Vout to the internal 1.25 V reference sets the ouput voltage. V_{out} can be calculated based off the following equation:

$$V_{out} = V_{FB} \cdot \frac{R1 + R2}{R2}$$

For external margining cases, set R2 ≤ 10K the injected external current cource range can be programmed based off the following equation:

$$I_{SourceMAX} = I_{SinkMAX} < 0.8 \cdot \left(\frac{VFB}{R2}\right)$$

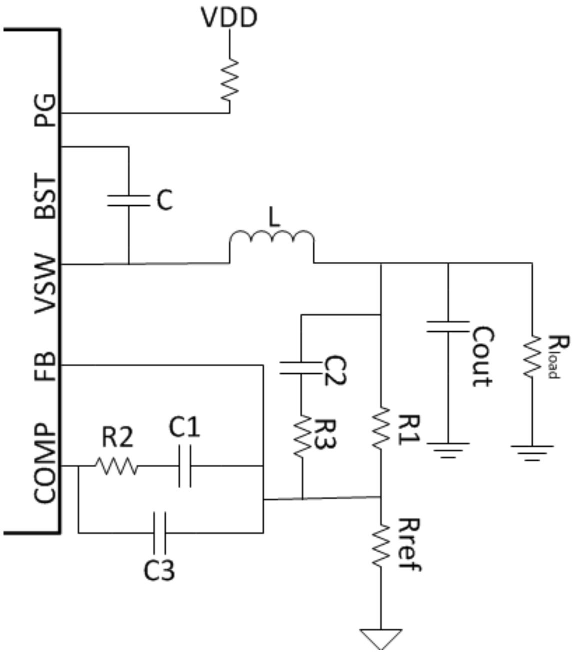


Figure 43. External Components around NCP4060

Selecting the Inducor

The inductor is the current source to the output load. A large inductor value will result−in low ripple currents which translates to low output voltage ripple. However a large inductor affects the loop response, has a higher series resistance and might take up valuable real−estate. A small inductor value will have large ripple which could stress the MOSFETs, increase core loss and requires more filtering to smoothen the output voltage.

A good compromise between size, cost and effectivity is to design the inductor current ripple to be 20% of the maximum output load current. The inductor value for a buck regulator can be calculated based off the following equation:

$$L = \frac{V_{OUT} \cdot \left(V_{IN(Max)} - V_{OUT}\right)}{V_{IN(Max)} \cdot F_{SW} \cdot 20\% \cdot I_{OUT(Max)}}$$

Where the peak inductor current value is :

$$I_{L(pk)} = I_{OUT(Max)} + 0.5 \cdot \Delta IL(pp)$$

And the RMS current through it is:

$$I_{L(RMS)} = \sqrt{I_{OUT(Max)}{}^2 + \frac{\Delta IL(pp)^2}{12}}$$

Selecting Input Capacitors:

In a typical DC−DC application the input capacitor is designed based on a target input voltage ripple of 2%. The input voltage ripple is primarly constituted of ESR and capacitance based ripple. Using capacitors with low ESR is recommended. Ceramic capacitors are best for providing low ESR however designers must take into account the degradation in capacitance value with applied voltage. Use the following equation for calculating $C_{IN.}$

$$C_{IN} = \frac{I_{OUT} \cdot D \cdot (1 - D)}{F_{SW} \cdot [V_{ripple-ESR} \cdot I_{OUT} \cdot \left(1 + \frac{\Delta IL(pp)^2}{12}\right)]}$$

Where the RMS Current through the capacitor is:

$$I_{CIN(RMS)} = I_{OUT} \cdot \sqrt{D \cdot \left(1 - D + \frac{\Delta IL(pp)^2}{12}\right)}$$

Selecting Output Capacitors:

The output bulk maintains the DC output voltage. The use of ceramic capacitors is recommended to sustain a low output voltage ripple. At switching frequency the ceramic capacitors are capacitance dominante use the following equation for calculating C_{Out} where the ripple output voltage is within 1% of Vout.

$$\Delta_{OUT} = \frac{V_{OUT} \cdot (1 - D)}{8 \cdot F_{SW}{}^2 \cdot L \cdot C_{OUT}}$$

And the RMS current through it is

$$I_{COUT(RMS)} = I_{OUT} \cdot \frac{\Delta IL(pp)}{\sqrt{12}}$$

Selecting External Compensation:

The NCP4060 is a voltage mode buck regulator with an error amplifier compensated by external components to achieve accurate output voltage regulation and to respond to fast transient events. The goal of the compensation network is to provide a loop gain function with the highest cross−over frequency at adequate phase and gain margins.

The output stage (LC) of the buck regulator is a double pole system. The resonance frequency of this lowpass filter is shown below:

$$f_{p0} = \frac{1}{2\pi \cdot \sqrt{LC_{OUT}}}$$

The output filter has a zero that is calculated from the output capacitance and output capacitor ESR:

$$f_{z0} = \frac{1}{2\pi \cdot ESR \cdot C_{OUT}}$$

The bode plot of the power stage, error amplifier and the desired loop gain are drawn in the figure below. The first zero (f_{z1}) compensates the phase lag of the pole located at the origin followed by a second zero (f_{z2}) to compensate for one of the poles of the LC filter in order to crossover (f_c) at −20 dB slope. The second pole (f_{p2}) is aimed to cancel the ESR zero and finally the third pole (f_{p3}) is to provide attenuation for frequencies above $f_{sw/2}$.

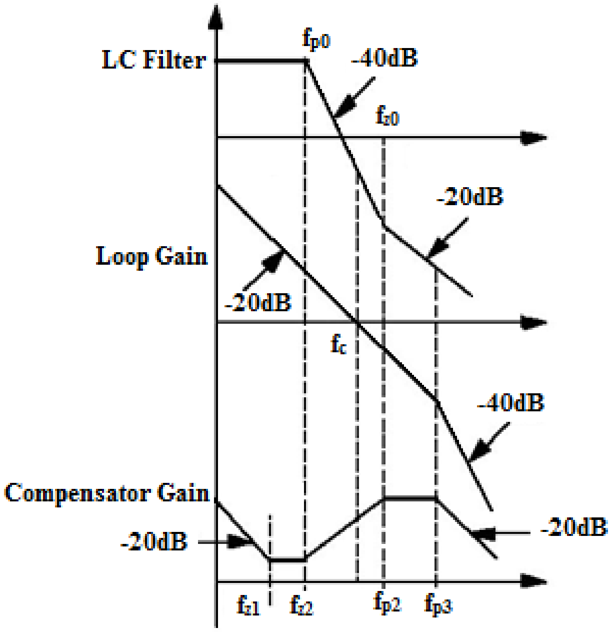


Figure 44. Power Stage, Loop Gain and Compensator Bode Plots

For ease of calculation, with C1 >> C3:

$$f_{z1} = \frac{1}{2\pi \cdot (R1 + R3) \cdot C2}$$

$$f_{z2} = \frac{1}{2\pi \cdot R2 \cdot C1}$$

$$f_{p2} = \frac{1}{2\pi \cdot R3 \cdot C2}$$

$$f_{p3} = \frac{1}{2\pi \cdot R2 \cdot C3}$$

$$f_c = \frac{V_{IN}}{2\pi \cdot V_{Ramp} \cdot R1 \cdot C1}$$

(Typically set to f_{sw} / 10)

The table below showcases typical compensation values for 48 V_{In} , 5 V_{Out} at 300 kHz with a 15 μH inductor and 5 x 10 μF MLCCs.

Table 7. Compensation Values for 48 V_{In}, 5 V_{Out}, 300 kHz

Values	Cross−Over Frequency	Phase Margin	Gain Margin
R_{ref} = 6.65 kΩ	35 kHz	60 Degrees	−20 dB
C1 = 10 nF			
R2 = 2.2 kΩ			
R3 = 200 Ω			
C2 = 4 nF			
C3 = 150 pF			
R1 = 20 kΩ			

PCB Layout Guidelines

All signals carrying pulsed currents must be kept short and wide to keep trace inductance to an absolute minimum. All current carrying loops must be kept short since inductance of ac current carrying loop is proportional to the area enclosed by the loop. Input ceramic caps must be placed as close as possible to Vin, V_B, V_{DD} Pins to sustain a smooth Supply Voltage. Route the Switch node and HB away from sensitive analog signals such as the feedback Voltage.

Connect Vin, Vsw and GND pads to large copper areas. It is highly recommended to use 2 Oz CU for improved thermal performance. Add Vias within pads to connect to bottom layers.

A picture of the Top layer of the NCP4060 Eval Board is provided to highlight the recommended layout guidelines.

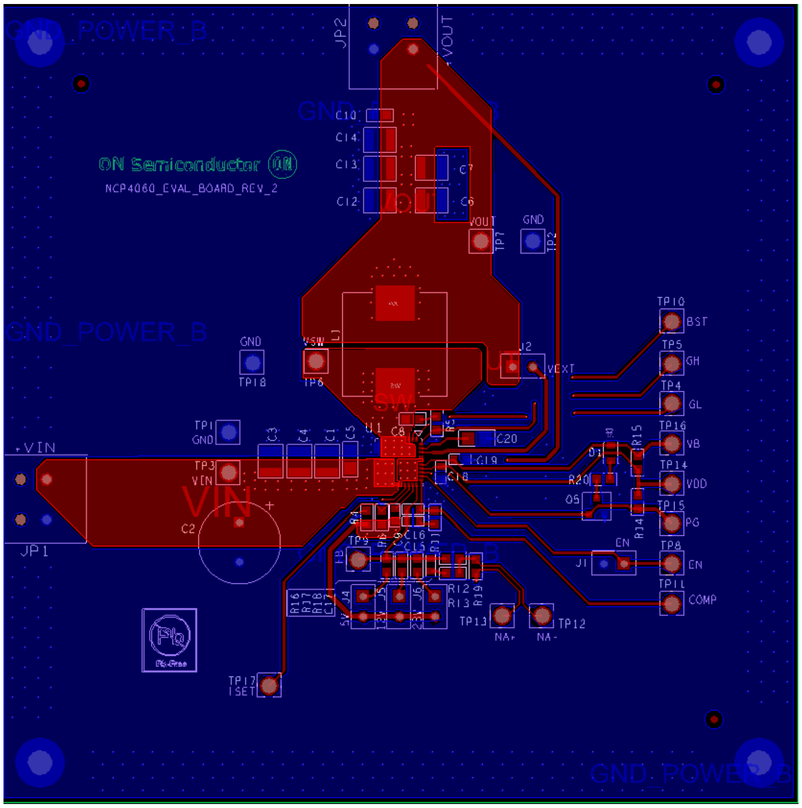


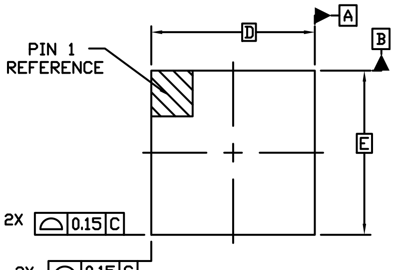
Figure 45. Top Layer of NCP4060 Eval Board

PACKAGE DIMENSIONS

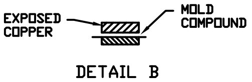
QFN20 6x6, 0.5P

CASE 485FC

ISSUE B



TOP VIEW



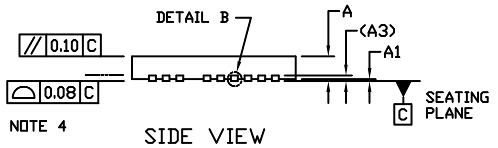
DETAIL B

ALTERNATE CONSTRUCTION

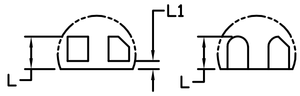
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN.	MILLIMETERS MAX.
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	3.15	3.35
D3	2.50	2.60
D4	2.15	2.35
D5	1.50	1.60
E	6.00 BSC	
E2	4.15	4.25
E3	2.38	2.48
E4	2.28	2.48
E5	2.20	2.40
L	0.30	0.50
L1	---	0.15
L3	0.10	0.30

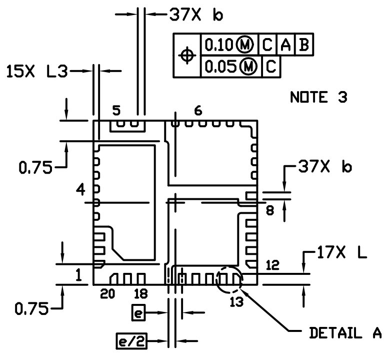


SIDE VIEW

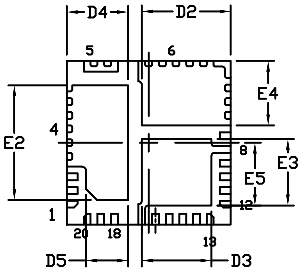


DETAIL A

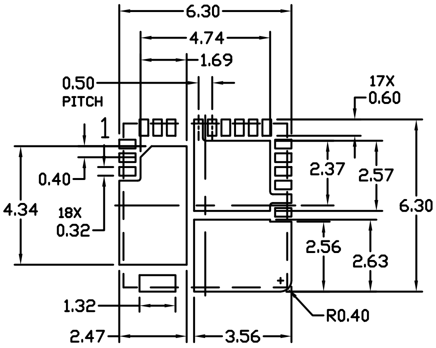
ALTERNATE TERMINAL CONSTRUCTIONS



BOTTOM VIEW



BOTTOM VIEW SUPPLEMENTAL



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