eGaN® FET Electrical Characteristics

EFFICIENT POWER CONVERSION

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In this paper the basic electrical characteristics of eGaN FETs are explained and compared against silicon MOSFETs. A good understanding of the similarities and differences between these two technologies is a necessary foundation for understanding how much we can improve existing power conversion systems.

MAXIMUM RATINGS:

Every semiconductor has a limit to its capabilities. These limits are typically expressed prominently in a device data sheet and serve as a guide to designers as to how to create designs that do not have hidden quality or reliability issues. EPC's eGaN FET data sheets display these maximum limits at the top of the first page. An example is shown in Table 1.

For the EPC2010 the maximum V_{DS} (Voltage applied from drain to source) is listed as 200 V. This limit assumes the voltage applied to the gate is 0 V with reference to the source. A higher gate-to-source voltage might result in current flow between drain and source which could overheat the device if the FET thermal limit is exceeded. This thermal limit is given in the second-to-last row of Table 1. In this example, it is a maximum of 125°C.

The maximum drain current (I_D) rating is given both as a continuous current and as a pulsed current. The continuous current rating (12 Amperes in this example) assumes the ambient temperature is maintained at 25°C and that there is a thermal resistance from the device junction to the ambient of less than 13 °C/Watt. With a worst case device on-resistance and a worst case temperature coefficient to that on-resistance, the device will remain under 125°C with 12 A DC applied. The pulsed I_D (60 A in this example) is also set such that the maximum junction temperature of the device will remain below 125°C if a single pulse of 300 μS duration is applied.

V_{GS} (The voltage applied between gate and source) has a maximum of 6 V in the positive direction and 5 V in the negative direction. These values are relatively low compared with power MOSFETs and designers need to make certain their layouts do not have overshoot that takes the gate voltage beyond these limits.

eGaN FETs have a minimum operating and storage temperature (T_J and T_{STG}) of -40°C. Below that value there has been no testing to establish functionality and therefore that has been chosen as the lower limit. Similarly, the maximum operating temperature of 125°C and storage temperature of 150°C are the highest temperatures at which devices were tested for long-term stability.

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage	200	V
I_D	Continuous (T_A =25˚C, θ_{JA} = 17)	12	A
	Pulsed (25˚C, Tpulse = 300 μs)	60	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-5	
T_J	Operating Temperature	-40 to 125	°C
T_{STG}	Storage Temperature	-40 to 150	

Table 1: Maximum ratings for an EPC2010 eGaN FET [1] as an example.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Static Characteristics (T_J= 25˚C unless otherwise stated)							
BV$_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0$ V, $I_D = 200$ µA	200			V	(1)
I$_{DSS}$	Drain Source Leakage	$V_{DS} = 160$ V, $V_{GS} = 0$ V		50	150	µA	(2)
I$_{GSS}$	Gate-Source Forward Leakage	$V_{GS} = 5$ V		1	3	mA	(3)
	Gate-Source Reverse Leakage	$V_{GS} = -5$ V		0.2	1		(4)
V$_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 3$ mA	0.7	1.4	2.5	V	(5)
R$_{DS(ON)}$	Drain-Source On Resistance	$V_{GS} = 5$ V, $I_D = 6$ A		18	25	mΩ	(6)
Source-Drain Characteristics (T_J= 25˚C unless otherwise stated)							
V$_{SD}$	Source-Drain Forward Voltage	$I_S = 0.5$ A, $V_{GS} = 0$ V, T = 25˚C		1.8		V	(7)
		$I_S = 0.5$ A, $V_{GS} = 0$ V, T = 125˚C		1.8			

All measurements were done with substrate shorted to source.

Table 2: Key operating parameters for the EPC2010 eGaN FET as an example

KEY DEVICE PARAMETERS:

The key operating parameters should give the designer much of the information necessary to design a system with predictable results. Table 2 is an example of these key parameters for the same EPC2010 used in the prior section. These parameter values are for room temperature except where indicated otherwise.

BV$_{DSS}$ (Drain-to-source breakdown voltage – line (1) in Table 2) is the same as the maximum V_{DS} however, in this table, the maximum current that the device will conduct at this voltage is given (200 µA). This leakage current, multiplied by the BV$_{DSS}$, indicates this device will only dissipate 40 mW while blocking full voltage; insignificant in most power conversion systems.

I$_{DSS}$ (Drain-to-source leakage current – line (2) in Table 2) is another way of looking at the amount of power dissipated while blocking voltage. In this example, the I$_{DSS}$ is specified at 80% of rated BV$_{DSS}$ because it is a more common operating point for most systems using 200 V rated transistors. Note that at 160 V the typical power loss from the current leaking from drain to source is only 8 mW.

I$_{GSS}$ (Gate-to-source leakage lines (3) and (4) in Table 2) is specified in both the forward and reverse direction. Most designs will be able to easily accommodate the small leakage current that is normal in an e-mode GaN transistor. Figure 1 shows the I$_{GSS}$ for an EPC2010 as a function of voltage for 25°C and 125°C.

V$_{GS(TH)}$ (Threshold voltage – line (5) in Table 2) is the voltage applied from gate-to-source below which the device is conducting minimal current. It has a typical value of 1.4 V in this example. This device as specified will have less than 3 mA current from drain-to-source if the gate voltage is maintained below 0.7 V. Unlike a power MOSFET, this threshold voltage is relatively insensitive to temperature as shown in Figure 2.

R$_{DS(ON)}$ (On-Resistance – line (6) in Table 2) is the resistance of the eGaN FET when 5 V is applied from gate to source and 6 A is flowing from drain to source at 25oC. The R$_{DS(ON)}$ will vary with both the gate voltage applied and the junction temperature of the device. As can be seen in Figure 3, only 4 V is needed to be applied to the gate in order to achieve the lowest (fully saturated) R$_{DS(ON)}$ for drain currents less than 40 A.
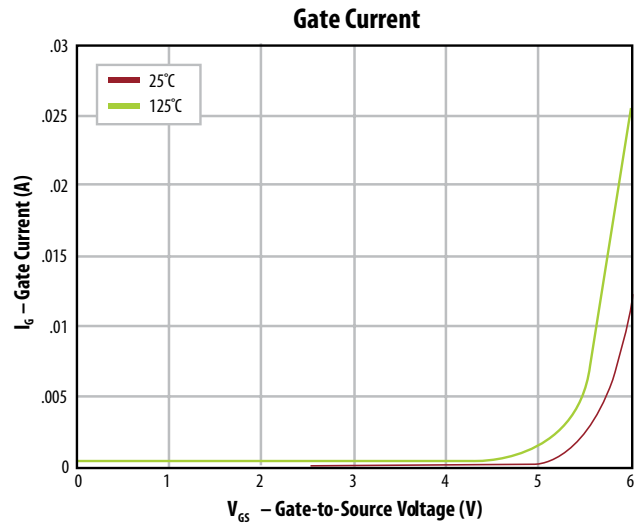

Figure 1: Gate current vs gate-source voltage at 25°C and 125°C for the EPC2010 as an example.
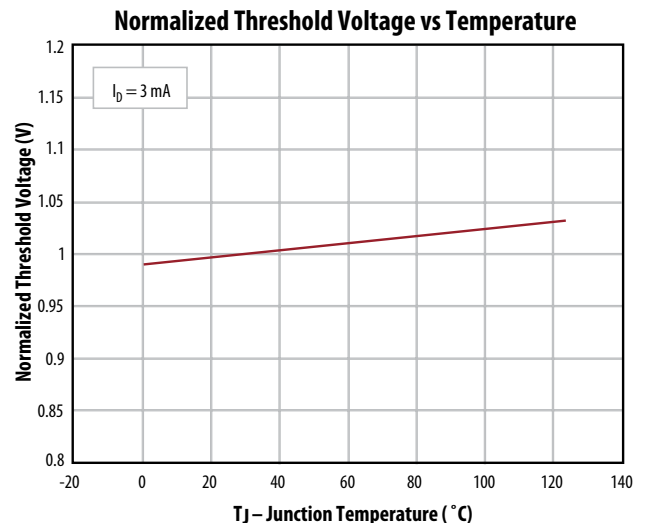

Figure 2: Normalized threshold voltage vs temperature showing only a 3% change over the operating range of the EPC2010.
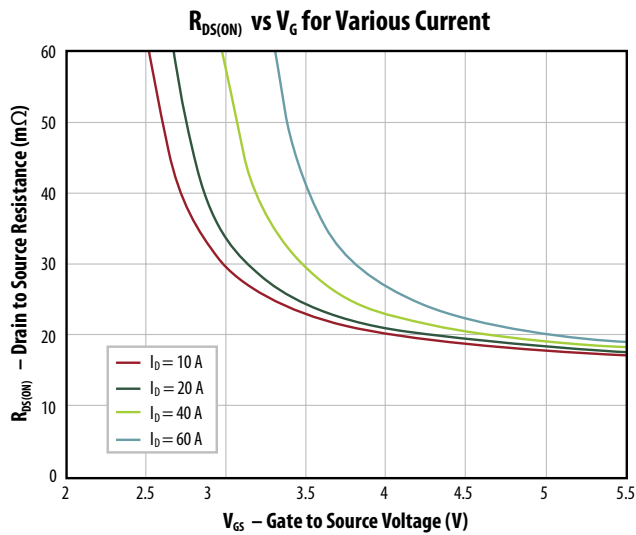
$R_{DS(ON)}$ vs V_G for Various Current

Figure 3: On-resistance vs gate-to-source voltage for various drain current levels for the EPC2010.

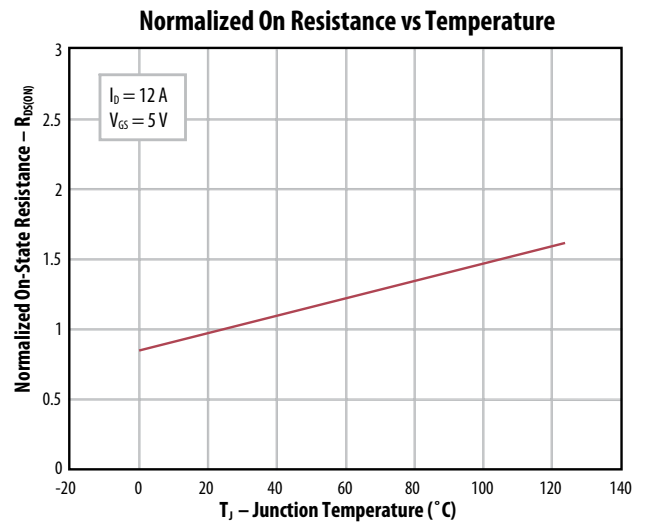### Normalized On Resistance vs Temperature

Figure 4: On-resistance vs temperature for the EPC2010.

One of the advantages of eGaN technology over silicon is the lower increase in on-resistance ($R_{DS(ON)}$) with temperature as shown in Figure 5. Whereas silicon has >70% increase in $R_{DS(ON)}$ between 25°C and 100°C [2], the eGaN FET shows about 50% increase. This translates into roughly 15% lower $R_{DS(ON)}$ at a typical 100°C junction temperature assuming the same initial $R_{DS(ON)}$ at 25°C.

V_{SD} (Source-drain forward voltage – line (7) in Table 2) is the voltage drop across the device when voltage is applied from source to drain. This is the reverse direction from the normal forward FET conduction. At 0.5 A and with 0 V between gate and source, the typical value of V_{SD} is 1.8 V. Figure 6 shows how this "body diode" forward drop varies with source-drain current. It should be noted that, because this body diode is formed by turning on the 2DEG in the reverse direction using the drain-gate voltage to enhance the channel, if the gate voltage is lowered below 0 V, the forward drop will follow. For example, if the gate drive of a circuit turns off the eGaN FET by applying a negative 1 V to the gate, the V_{SD} at 0.5 A will be 2.8 V.
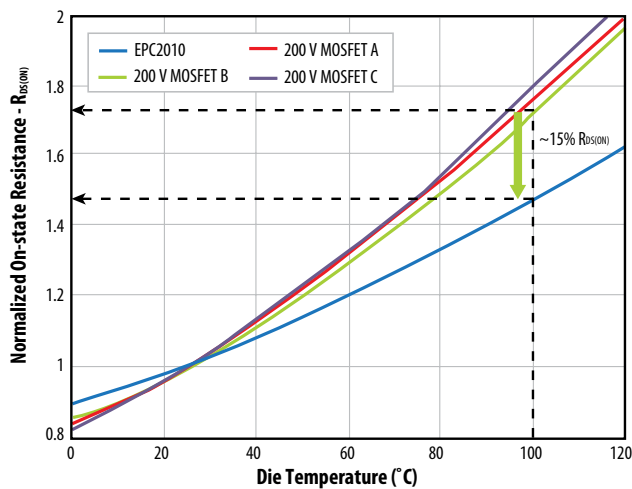
Figure 5: Comparison between normalized $R_{DS(ON)}$ vs temperature for the EPC2010 eGaN FET and various 200 V rated silicon MOSFETs.
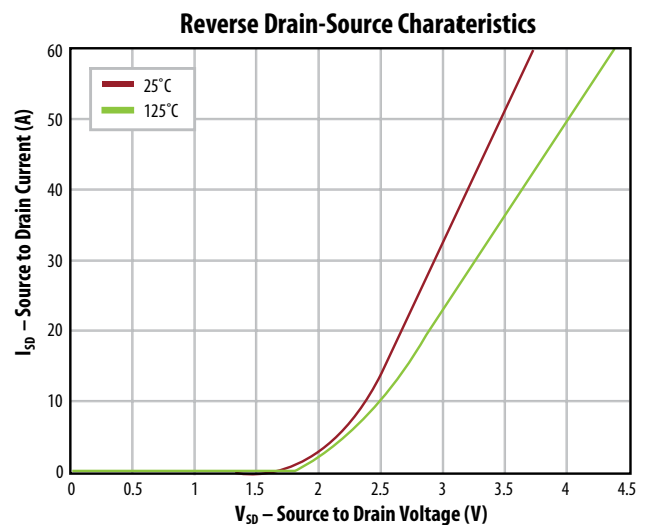
Reverse Drain-Source Charateristics

Figure 6: Body-diode forward drop vs source-drain current and temperature for the EPC2010.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Characteristics (T_J= 25˚C unless otherwise stated)						
C_{ISS}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V		480	540	pF
C_{OSS}	Output Capacitance			270	350	
C_{RSS}	Reverse Transfer Capacitance			9.2	12	
Q_G	Total Gate Charge (V_{GS} = 5 V)	V_{DS} = 100 V, I_D = 12 A		5	7.5	nC
Q_{GD}	Gate to Drain Charge			1.7	2.6	
Q_{GS}	Gate to Source Charge			1.3	2	
Q_{OSS}	Output Charge			40	50	
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate shorted to source.

Table 3: Capacitance and charge specifications for EPC2010.

CAPACITANCE AND CHARGE

A FET's capacitance is the biggest factor in determining the energy that will be lost in a device during a transition from the ON to OFF state, or from the OFF to the ON state. The capacitance determines the amount of charge that needs to be supplied to various terminals of the device to change the state. The faster this charge is supplied, the faster the device will switch. As an example, Table 3 lists the values for Capacitance (in pico-farads) and Charge (in nanocoulombs) that can be expected from the EPC2010. Figure 7, a cross section depicting a typical eGaN FET, illustrates the location of the capacitive component elements of each of the data sheet values and their physical origin.

The capacitive elements in Figure 7 can be related to the data sheet values as follows:
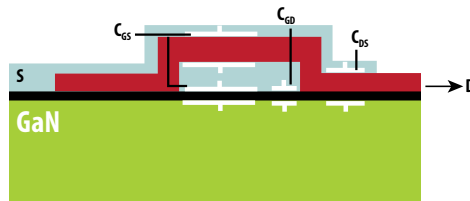
- $C_{OSS} = C_{GD} + C_{DS}$
- $C_{ISS} = C_{GD} + C_{GS}$
- $C_{RSS} = C_{GD}$

Figure 7: Cross section of the eGaN FET showing the location of capacitive elements.

These capacitances are a function of the voltage applied to various terminals. Figure 8 shows how the values change as the voltage from drain to source increases. The reason for the drop in capacitance as V_{DS} goes up is that the free electrons in the GaN are depleted away. For example, the initial step down in C_{OSS} (Output capacitance) is caused by the depletion of the 2DEG near the surface. Further increase in V_{DS} extends the depletion region deeper into the body of the device thus increasing the distance between the plates of the capacitor.

If you integrate the capacitance between two terminals across a range of voltage applied to the same terminals, you obtain the amount of charge, "Q" that was consumed charging the capacitor. Since current over time equals charge, it is often very convenient to look at the amount of charge necessary to change the voltage across various terminals in the eGaN FET. Figure 9 shows the amount of gate charge, Q_G, which must be supplied to increase the voltage from gate to source to a desired voltage. Referring to this figure, it can be seen that about 5 nanocoulombs are needed to achieve 5 V on the gate. If a designer wants to achieve 5 V on the gate, a value that will ensure the device is fully turned ON, they must deliver this amount of charge. If the gate drive is capable of supplying 1 A of current, it will take about 4.5 nS to achieve this voltage.
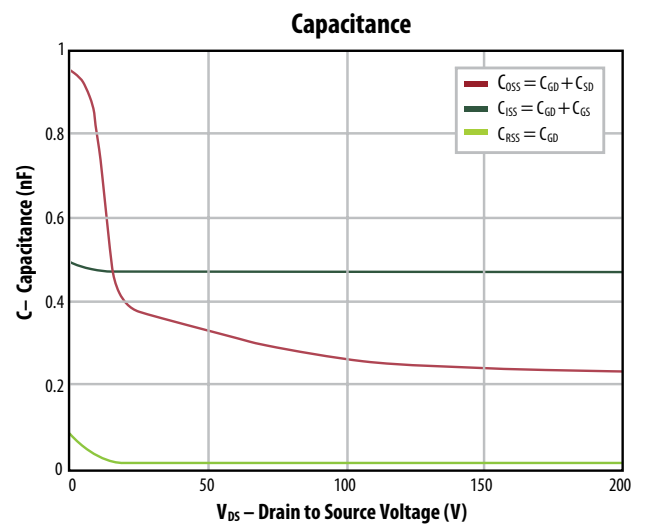

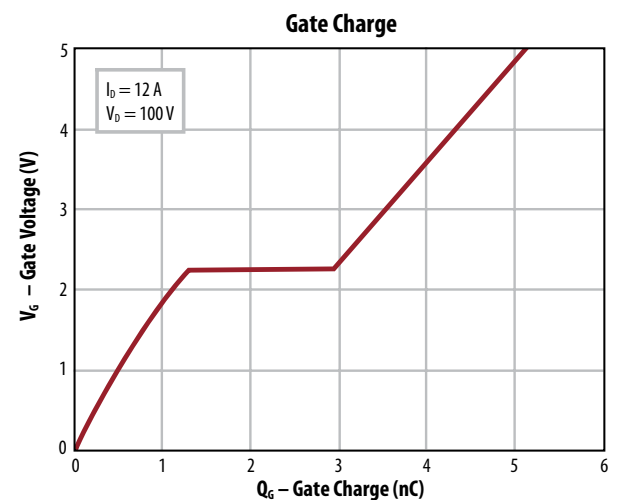*Figure 8: Capacitance vs Drain-Source Voltage for the EPC2010.*

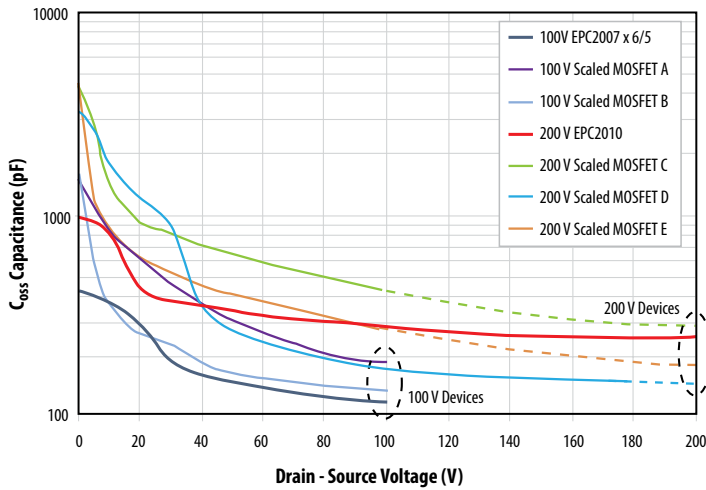*Figure 9: Gate charge vs gate voltage for the EPC2010.*

Figure 10: C_{OSS} vs. V_{DS} normalized to 25 mΩ for various eGaN FETs and comparable MOSFETs.
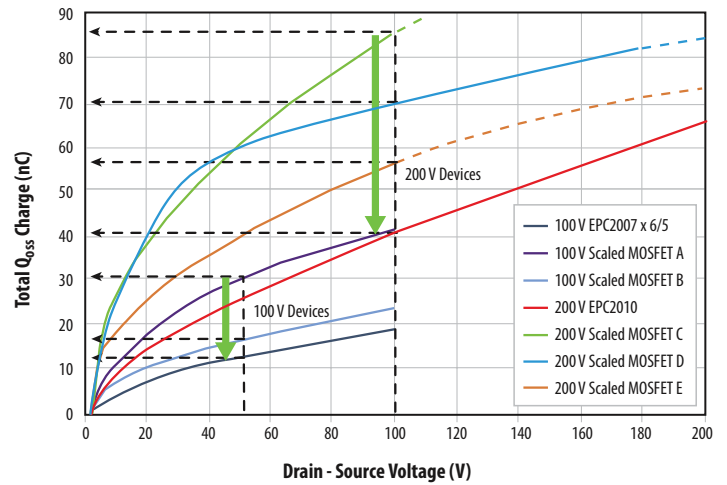

Figure 11: Q_{OSS} vs V_{DS} normalized to 25 mΩ for various eGaN FETs and comparable MOSFETs.

The same concept is true for the charge needed to be supplied to the output terminals (Q_{OSS}).

The Q_{GD} and Q_{GS} are also specified separately because the ratio of these two values, Q_{GD}/Q_{GS}, called the Miller Ratio, is often an important metric to determine the point at which a device can turn on due to a transient applied between drain and source.

OUTPUT CAPACITANCE LOSSES

During 'hard' switching (device commutates both voltage and current) of a half-bridge, the turn on transition, energy equal to that stored in the C_{OSS} of both devices is dissipated in the switch turning on. By way of example, a common topology used in DC-DC conversion is the buck converter [3]. In a typical buck converter, the other switch node voltage transition (turn-off) is considered 'soft' switching, as the inductor energy is used to charge C_{OSS} in a lossless manner. In the past, when using older power MOSFETs, this loss component was much less important compared to the actual switching loss, but, as device switching FOM keeps improving, this component is becoming more dominant and therefore more important when determining total loses in the device. This value can be calculated by integrating the C_{OSS} vs. voltage curve to the working voltage for a converter employing the device. In Figure 10, the C_{OSS} vs. voltage for 100 V and 200 V eGaN and silicon MOSFETs is compared. (All devices have been normalized to 25 mΩ). Overall, the total eGaN FET Q_{OSS} losses are much lower than comparable silicon as evident when plotting Q_{OSS} vs. voltage for the same devices as in Figure 11. At half rated voltage eGaN FETs show between three quarters and half the Q_{OSS} losses of comparative silicon devices.

DIODE RECOVERY

There is one other charge element, Q_{RR}, in Table 3 that does not directly relate to a device capacitance. EPC's eGaN structure is a lateral device, absent of the parasitic bipolar junction common to silicon MOSFETs. As such, 'body diode' operation has a different mechanism, but similar function. With zero bias applied from gate to source, there is an absence of electrons under the gate region (device is OFF). As the drain voltage is decreased, a positive bias on the gate is created relative to the drift region, injecting electrons under the gate. Once the gate threshold is reached, there will be sufficient electrons under the gate to form a conductive channel. The benefit of this mechanism is that there are no minority carriers involved in conduction, and therefore no reverse recovery losses. Q_{RR} therefore is ZERO.

THERMAL RESISTANCE

The thermal properties of the eGaN FET in the Land Grid Array (LGA) package are shown in Table 4.

Thermal Characteristics		**TYP**	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.8	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	16	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	56	°C/W

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Table 4: Thermal Characteristics of the EPC2010.

The three parameters listed are defined as follows:

- $R_{\theta JB}$ is the Thermal Resistance from the device junction to the bottom of the solder bumps, without consideration of the type or size of the mounting circuit board.

- $R_{\theta JC}$, is the thermal resistance from the device junction through the back (silicon side) of the device, and is given for those end user who wish to add additional heat-sinking to the top of the eGaN FET [4].

- $R_{\theta JA}$, is given for those cases where the end user simply wants to mount the eGaN FET onto the application's circuit board with no additional heat sinking. It specifies the thermal resistance that a user can expect when the device is mounted onto an FR4 PCB with one square inch of 2 ounce copper.

Once the electrical and mechanical design of a circuit is completed, these values for thermal resistance can be used to determine the final device temperature that can be expected under various operating conditions.

TRANSIENT THERMAL IMPEDANCE

Rarely is a transistor used with a continuous DC flow of current through the device. In order to give designers a measure of the thermal impact with a short pulse, or a repetition of pulses of various duty cycles, eGaN FET data sheets also have a Transient Thermal Impedance Graph as shown in Figure 12 [5].

As an example let's look at an EPC2010 mounted on a PCB without a heatsink on the back. If the circuit pulses the part with a 10 W instantaneous pulse (P_{DM}) at a 10% duty cycle, and the pulses are 100 µs long, and the board is sufficient to absorb the heat with little temperature impact, the effective thermal resistance and junction temperature rise would be as follows:

$$R_{\theta JB(Effective)} = R_{\theta JB} \times 0.1 \text{ or } 5.6 \text{ }^{o}C/W \text{ (1)}$$

$$T_{J} = P_{DM} \times 5.6 \text{ } oC/W \text{ or } 56 \text{ }^{o}C \text{ (2)}$$
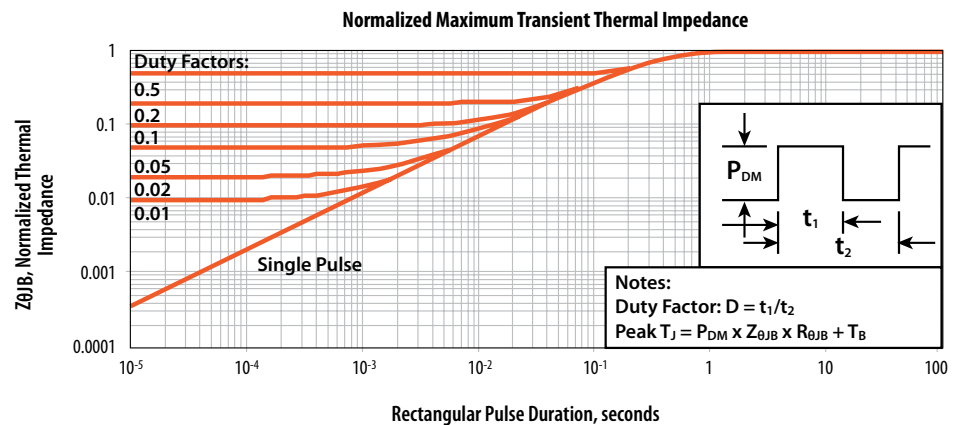

Figure 12 Transient Thermal Response Curve for all EPC eGaN FETs.

Note that you would have to add to the ΔT_{J} in equation (2) any measured rise in the temperature of the surface of the PCB to get a more accurate gauge of the actual rise in device temperature.

THE FIGURE OF MERIT (FOM)

It is helpful to compare the electrical performance of an eGaN FET with a power MOSFET so a designer can understand the benefits that can be achieved with this displacement technology. To effectively compare the two technologies, some figures of merit need to first be defined.

A FOM that has been used by MOSFET manufactures to show both generational improvements and to compare their products to other competitive devices is the product of the gate charge, Q_{G}, and the $R_{DS(ON)}$ for a given device. What makes this so useful is that no matter the size of the die, this FOM is almost constant for a given technology or 'Generation' of device. As we will show below, this FOM is related to device performance and can be useful in predicting power loss improvements with improved technologies, but it is less sensitive to differences when a device is used more as a switching element than as a conducting element. We will therefore discuss two distinct FOMs. The first of these is the traditional FOM. We will call that the "Rectifier FOM" because it is most applicable when a FET is used as a rectifier element such as in the lower transistor of a buck converter. The second and new FOM, we will call the "Switching FOM" because it best describes relative performance of devices used mostly as switching elements such as in the upper transistor in a classic buck converter.

1) The Rectifier FOM (lower is better), also known as the conduction FOM, compares rectifier performance in terms of conduction and gate drive power loss ($R_{DS(ON)} \times Q_{G}$). For a 'soft' switching device, where Q_{GD} is not important, you would like to lower $R_{DS(ON)}$ to improve efficiency, but this increases Q_{G} and thereby increases gate drive losses and overdrive time.

2) The Switching FOM (lower is better) compares switching performance. $R_{DS(ON)} \times Q_{GD}$ is used because Q_{GD} plays a dominant role in switching loss, and it is difficult to reduce this number without increasing $R_{DS(ON)}$ for a given technology.

Of these two FOMs, the switching performance is more important in 'hard switching' converter circuits.

Figure 13 plots $R_{DS(ON)}$ vs. Q_{GD} for eGaN FETs as well as for various equivalent silicon MOSFETs. We can see that, based on switching FOM, eGaN FETs offer a distinct advantage over any equivalent voltage rated silicon device. Below are some general observations:

- 40 V eGaN FETs are comparable to 25 V lateral silicon devices.

- 100 V eGaN FETs are comparable to 40 V vertical silicon devices

- 200 V eGaN FETs are comparable to 100 V vertical silicon devices

The rectifier FOM is shown in Figure 14 and plots $R_{DS(ON)}$ vs. Q_G for the eGaN FET as well as for different equivalent silicon MOSFETs. From this we can draw a number of conclusions:

- 40 V eGaN FETs are comparable to the best 25 V lateral silicon devices.

- 100 V eGaN FETs are comparable to 25 V vertical silicon devices.

- 200 V eGaN FETs are comparable to 40 V vertical silicon devices

Although a FOM is a useful tool for comparing switching power devices, there are a number of other parameters of equal importance that also need to be considered. We will now look at package-related comparisons between eGaN FETs and state-of-the-art MOSFETs.

PACKAGE RELATED PARAMETERS

As low voltage silicon MOSFET performance has improved over the last number of years, the need for high performance packaging has become a significant limiting factor in device performance. This led to the development of such innovative packages as the DirectFET [6], and PolarPak [7]. This still leaves the question: What are the key requirements of a high performance package?

Semiconductor devices are packaged to improve robustness and ease of handling. At higher voltages, some packaging may also be needed to meet voltage clearance and creepage requirements. Packaging, however, degrades performance compared to the bare semiconductor die in the form of increased cost, increased on-resistance, increased lead inductance, increased size, and reduced thermal performance.

Figure 13: $R_{DS(ON)}$ vs. Q_{GD} for various eGaN FETs and MOSFETs.
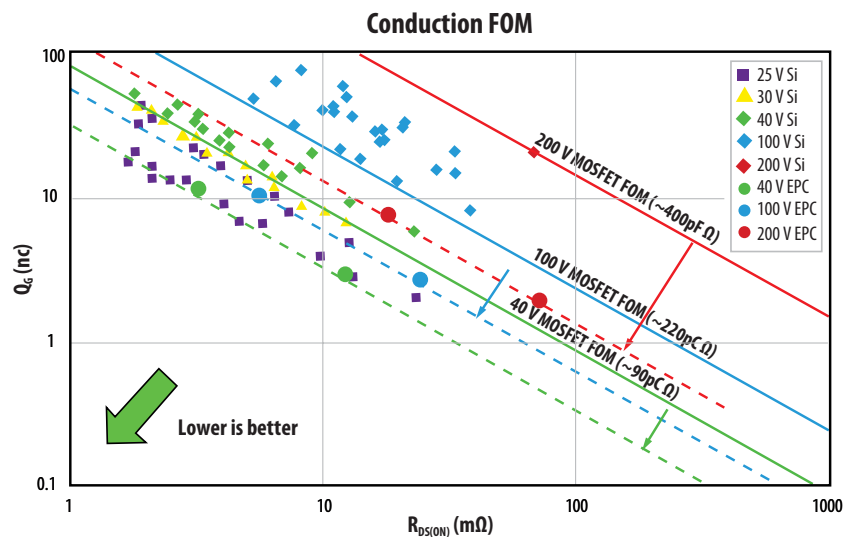
Figure 14: $R_{DS(ON)}$ vs. Q_G for various eGaN FETs and MOSFETs.

What sets high performance packaging apart is being able to realize the required advantages of device packaging while minimizing the drawbacks. With low voltage, leadless, dual-side-cooled packages such as DirectFET, PolarPak, chipscale, or LGA (Land Grid Array) become elegant solutions. Here the choice of package is largely dictated by the device terminal structure; vertical vs. lateral. A lateral device lends itself to easy chipscale packaging (e. g. Greatwall BGA MOSFETs [8]), while a vertical, "flipped" device needs to bring the 'back' terminal down to the printed circuit board (such as DirectFet or PolarPak). In a similar fashion, EPC's eGaN devices are in LGA packages where the interdigitation of source and drain terminals is used to minimize both connection resistance and parasitic inductance.
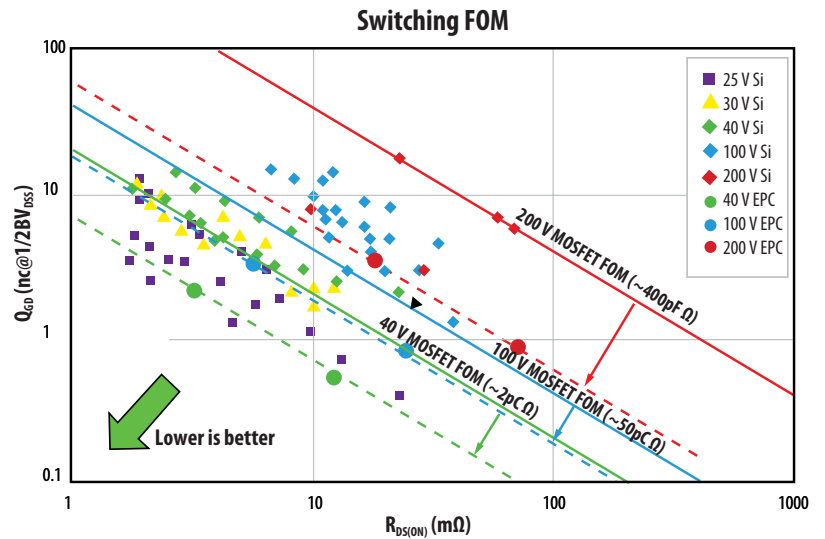
Estimated Package Resistance
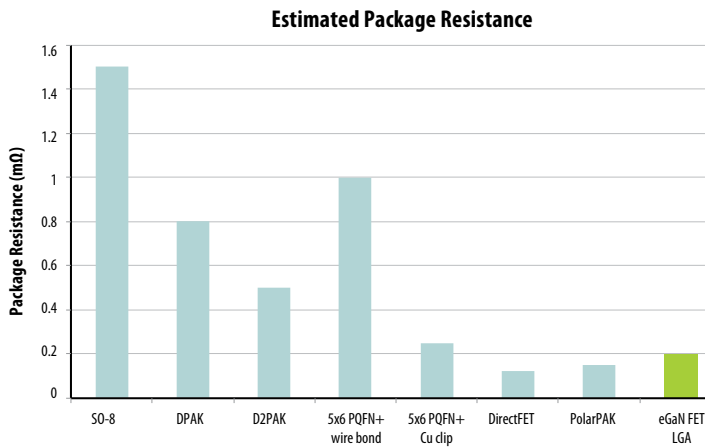

Figure 15: Estimated die free package resistance
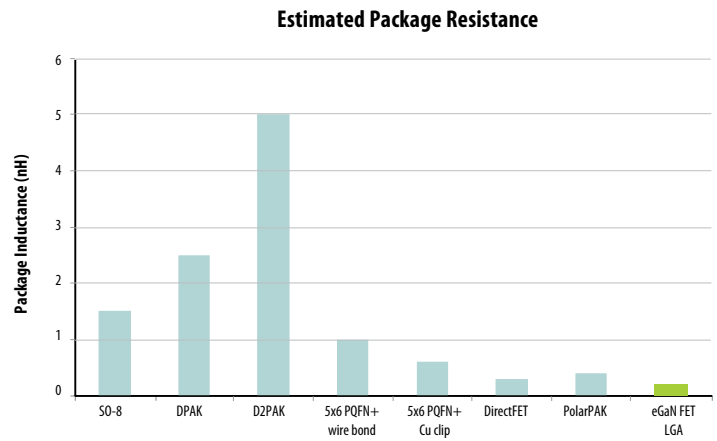for various power packages.

Estimated Package Resistance

Figure 16: Estimated die free package inductance
for various power packages.

PACKAGE RESISTANCE

The estimated packaging resistance of various standard power packages is shown in Figure 15 alongside the LGA parts.

PACKAGE INDUCTANCE

The addition of package inductance can have varied effects, depending on which terminal of the die the package inductance is added. A comparison of package inductance for the LGA is shown in Figure 16 compared to estimated values for some standard power packages. Common source inductance (inductance inside the package connected to the source terminal that carry both drain and gate return currents) can significantly increase switching losses by slowing down device switching through induced opposition of the applied gate voltage. To understand this further, consider the turn-on of a device as shown in Figure 17. As the device reaches threshold voltage and starts carrying increasing current, the di/dt induces a voltage across the source inductance that opposes the gate drive voltage. This voltage is trying to turn the device back OFF. The same is true during turn-off where the induced voltage adds to the gate drive voltage, thus trying to keep the device ON. It is therefore important to minimize common source impedance for optimum switching performance.
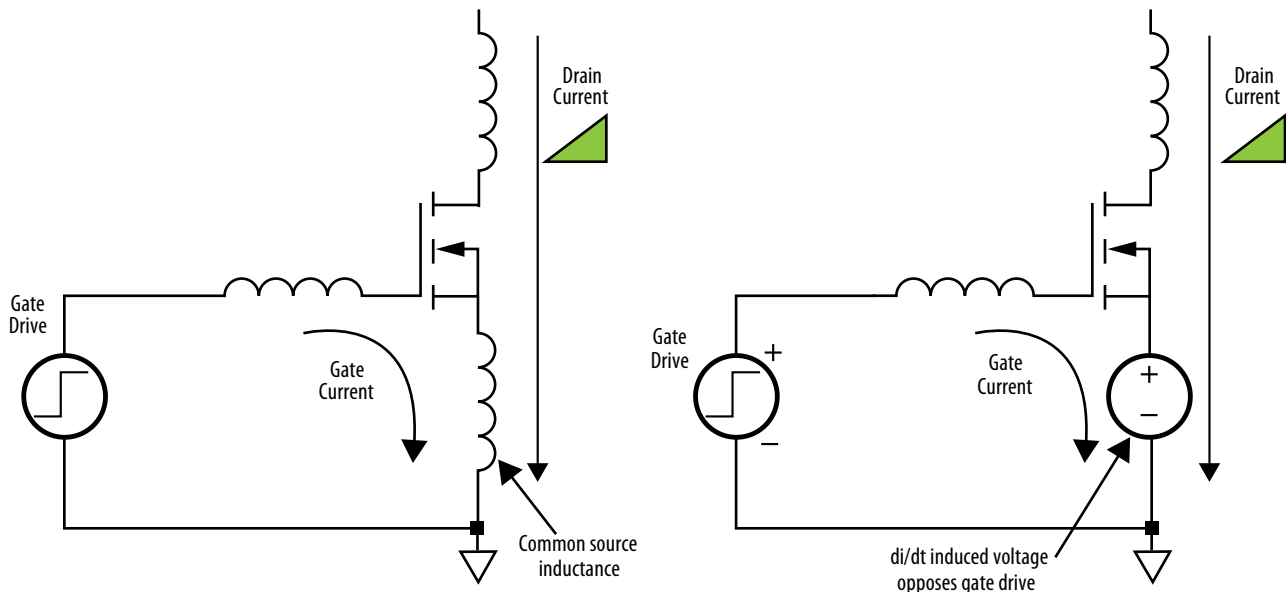

Figure 17: Equivalent circuit of device at turn-on showing di/dt induced voltage generated by the common source inductance.

PACKAGE SIZE

As end-products face the pressures of lower cost and smaller size, the size of the power devices has become of increasing importance. In general, a smaller size is desirable as long as the thermal requirements can be met. As mentioned earlier, the act of encapsulating a device inside a package will almost always deteriorate thermal and electrical performance. eGaN FETs allow a much lower on-resistance per unit area for the same voltage rating which leads to significantly smaller die and package size.

SUMMARY

In this paper we discussed the basic electrical, thermal, and mechanical characteristics of eGaN FETs and showed they have distinct advantages over current state-of-the-art silicon power MOSFETs. Since the silicon power MOSFET has come a long way since its introduction over thirty years ago, it would be fair to assume that future optimization of the basic eGaN power transistor structure and geometry will show similar improvement in years to come.

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