EPC eGaN® FETs Reliability Testing

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Efficient Power Conversion (EPC) Corporation introduced its first enhancement-mode Gallium Nitride (eGaN®) FETs in 2009 and since that time has published five reliability reports, as well as a textbook covering the subject [1-6]. The first section of this paper reports on the qualification testing of EPC's eGaN FETs under a wide variety of stress conditions. The test matrix covers the 40 V to 200 V eGaN FET families. The second section reports on the failure rate predictions using acceleration factors derived by operating devices well outside of normal operating conditions.

PART I: 40 TO 200 V QUALIFICATION TESTING

Qualification Test Overview

EPC's eGaN FETs were subjected to a wide variety of stress tests under conditions that are typical for silicon-based power MOSFETs. These tests included:

- High temperature reverse bias (HTRB): Parts are subjected to a drain-source voltage at the maximum rated temperature
- High temperature gate bias (HTGB): Parts are subjected to a gate-source voltage at the maximum rated temperature
- High temperature storage (HTS): Parts are subjected to heat at the maximum rated temperature
- Temperature cycling (TC): Parts are subjected to alternating high- and low temperature extremes
- High temperature high humidity reverse bias (H3TRB): Parts are subjected to humidity under high temperature with a drain-source voltage applied
- Unbiased autoclave (AC or Pressure Cooker Test): Parts are subjected to pressure, humidity, and temperature under condensing conditions
- Moisture sensitivity level (MSL): Parts are subjected to moisture, temperature, and three cycles of reflow.
- Electrostatic discharge (ESD): Parts are subjected to ESD under human body (HBM) and machine (MM) models.

The stability of the devices is verified with DC electrical tests after stress biasing. The electrical parameters are measured at time-zero and at interim readout points at room temperature. Electrical parameters such as the gate-source leakage, drain-source leakage, gate-source threshold voltage, and on-state resistance are compared against the datasheet specifications. A failure is recorded when a part exceeds the datasheet specifications. eGaN FETs are stressed to meet the latest Joint Electron Device Engineering Council (JEDEC) standards when possible.

Parts were mounted onto FR5 (high Tg FR4) or polyimide adaptor cards. Adaptor cards of 1.6 mm in thickness with two copper layers were used. The top copper layer was 1 oz. or 2 oz., and the bottom copper layer was 1 oz. Kester NXG1 type 3 SAC305 solder no clean flux was used in mounting the part onto an adaptor card.

High Temperature Reverse Bias

Parts were subjected to 80% of the rated drain-source voltage at the maximum rated temperature for a stress period of 1000 hours. The part type on stress testing covered the voltage range of 40 – 200 V.

Stress Test	Part Number	Revision	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTRB	EPC2001	C	100	L (4.11 x 1.63)	T=150°C, V_{DS}=80 V	0	77 x 2	1000
HTRB	EPC2016	C	100	M (2.11 x 1.63)	T=150°C, V_{DS}=80 V	0	77 x 3	1000
HTRB	EPC2014	C	40	M (1.70 x 1.09)	T=150°C, V_{DS}=32 V	0	77 x 1	1000
HTRB	EPC8004		40	S (2.05 x 0.85)	T=150°C, V_{DS}=32 V	0	77 x 1	1000
HTRB	EPC2010	C	200	L (3.55 x 1.63)	T=150°C, V_{DS}=160 V	0	77 x 2	1000
HTRB	EPC2012	C	200	M (1.71 x 0.92)	T=150°C, V_{DS}=160 V	0	77 x 1	1000

Table 1. High Temperature Reverse Bias Test

Note: EPC20xxC devices will begin to ship in 4Q2014

High Temperature Gate Bias

Parts were subjected to 5.75 V or 5.5 V gate-source bias at the maximum rated temperature for a stress period of 1000 hours. The part type on stress testing covered the voltage range of 40 – 200 V.

Stress Test	Part Number	Revision	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTGB	EPC2001	C	100	L (4.11 x 1.63)	T=150°C, V_{GS}=5.75 V	0	77 x 2	1000
HTGB	EPC2016	C	100	M (2.11 x 1.63)	T=150°C, V_{GS}=5.75 V	0	77 x 3	1000
HTGB	EPC2014	C	40	M (1.70 x 1.09)	T=150°C, V_{GS}=5.5 V	0	77 x 1	1000
HTGB	EPC8004		40	S (2.05 x 0.85)	T=150°C, V_{GS}=5.5 V	0	77 x 1	1000
HTGB	EPC2010	C	200	L (3.55 x 1.63)	T=150°C, V_{GS}=5.75 V	0	77 x 2	1000
HTGB	EPC2012	C	200	M (1.71 x 0.92)	T=150°C, V_{GS}=5.75 V	0	77 x 1	1000

Table 2. High Temperature Gate Bias Test

High Temperature Storage

Parts were subjected to heat at the maximum rated temperature. EPC2001C and EPC2016C were selected for this test to illustrate the capability.

Stress Test	Part Number	Revision	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTS	EPC2001	C	100	L (4.11 x 1.63)	T=150°C, Air	0	77 x 1	1000
HTS	EPC2016	C	100	M (2.11 x 1.63)	T=150°C, Air	0	77 x 2	1000

Table 3. High Temperature Storage Test

Temperature Cycling

Parts were subjected to temperature cycling between -40°C and +125°C for a total of 1000 cycles. Ramp rate of 15°C/min and dwell time of 5 minutes were used in accordance with the JEDEC Standard JESD22A104. The part types covered the voltage range of 40 – 200 V.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Cys)
TC	EPC2001	100	L (4.11 x 1.63)	-40 to +125°C, Air	0	35 x 3	1000
TC	EPC8007	40	S (2.05 x 0.85)	-40 to +125°C, Air	0	35 x 1	1000
TC	EPC2010	200	L (3.55 x 1.63)	-40 to +125°C, Air	0	35 x 1	1000

Table 4. Temperature Cycling Test

High Temperature High Humidity Reverse Bias

Parts were subjected to a drain-source bias at 85% RH and 85°C under 49.1 PSIA vapor pressure for a stress period of 1000 hours. The testing was done in accordance with the JEDEC Standard JESD22A101. The part types covered the voltage range of 40 – 200 V. The 40 V parts were subjected to 40 V drain-source bias, the 100 V parts were subjected to 80 V drain-source bias, and the 200 V parts were subjected to 100 V drain-source bias.

Stress Test	Part Number	Revision	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
H3TRB	EPC2001	C	100	L (4.11 x 1.63)	T=85°C, RH=85%, V_{DS}=80 V	0	25 x 1	1000
H3TRB	EPC2016	C	100	M (2.11 x 1.63)	T=85°C, RH=85%, V_{DS}=80 V	0	25 x 2	1000
H3TRB	EPC2015 *		40	L (4.11 x 1.63)	T=85°C, RH=85%, V_{DS}=40 V	0	50 x 1	1000
H3TRB	EPC2010 *		200	L (3.55 x 1.63)	T=85°C, RH=85%, V_{DS}=100 V	0	50 x 1	1000
H3TRB	EPC2012 *		200	M (1.71 x 0.92)	T=85°C, RH=85%, V_{DS}=100 V	0	50 x 1	1000

*Table 5. High Temperature High Humidity Reverse Bias Cycling Test * Results published in previous reliability report [5]*
Note: EPC20xxC devices will begin to ship in 4Q2014

Autoclave (Unbiased Pressure Cooker)

Parts were subjected to 100% RH at 121°C under 29.7 PSIA vapor pressure for a stress period of 96 hours in accordance with the JEDEC Standard JESD22A102. Parts were not electrically biased during stress. EPC2001C and EPC2016C were selected for this stress test to illustrate the capability.

Stress Test	Part Number	Revision	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
AC	EPC2001	C	100	L (4.11 x 1.63)	T=121°C, RH=100%	0	25 x 1	96
AC	EPC2016	C	100	M (2.11 x 1.63)	T=121°C, RH=100%	0	25 x 2	96

Table 6. Autoclave Test

Moisture Sensitivity Level

Parts were subjected to 85% RH at 85°C for a stress period of 168 hours. The parts were also subjected to three cycles of Pb-free reflow in accordance with the IPC/JEDEC joint Standard J-STD-020. EPC2001, EPC8003 and EPC8007 were selected for this stress test to illustrate the capability.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
MSL1	EPC2001	100	L (4.11 x 1.63)	T=85°C, RH=85%, 3 reflow	0	25 x 1	168
MSL1	EPC8003	40	S (2.05 x 0.85)	T=85°C, RH=85%, 3 reflow	0	25 x 1	168
MSL1	EPC8007	40	S (2.05 x 0.85)	T=85°C, RH=85%, 3 reflow	0	25 x 1	168

Table 7. Moisture Sensitivity Level Test

Electrostatic Discharge

Parts were subjected to ESD HBM and MM in accordance with the JEDEC Standard JESD22A114 Human Body Model and JESD22A115 Machine Model. EPC2001 and EPC8006 were selected for the test to cover the die size range.

EPC2001 L (4.11 x 1.63)	Pin-Pin	Passed Voltage	Failed Voltage	JEDEC Class
HBM	G-S	(±) 400 V	(+) 500 V	CLASS 1A
HBM	G-D	(±) 1500 V	(-) 2000 V	CLASS 1C
HBM	D-S	(±) 2000 V	(+) 3000 V	CLASS 2
MM	G-S	(±) 200 V	(-) 400 V	CLASS B
MM	G-D	(±) 400 V	(+) 600 V	CLASS C
MM	D-S	(±) 600 V	—	> CLASS C

EPC8006 S (2.05 x 0.85)	Pin-Pin	Passed Voltage	Failed Voltage	JEDEC Class
HBM	G-S	(±) 350 V	(±) 500 V	CLASS 1A
HBM	G-D	(±) 250 V	(+) 350 V	CLASS 1A
HBM	D-S	(±) 250 V	(+) 350 V	CLASS 1A
MM	G-S	(±) 25 V	(+) 50 V	CLASS A
MM	G-D	(±) 100 V	(-) 200 V	CLASS A
MM	D-S	(±) 50 V	(+) 100 V	CLASS A

Table 8. Electrostatic Discharge Test

Note: EPC20xxC devices will begin to ship in 4Q2014

PART II: PREDICTING EGAN FET RELIABILITY

Drain Acceleration

The dominant failure mechanism of GaN transistors of all types under HTRB stress is a dynamic upward shift of the on-resistance ($R_{DS(on)}$) [7]. The shifting increases with drain bias, and, at high enough bias, the part will eventually fail when the resistance exceeds the datasheet limits. The effect is caused by electron trapping near the conductive channel (2DEG) and in the deep buffer layers of the GaN epitaxial film [8]. Control of the near-surface traps and the lateral and vertical electric fields is necessary to mitigate dynamic $R_{DS(on)}$ shifting.

To quantify the effect, we have conducted a matrix of HTRB tests at accelerated drain voltages and at three different temperatures (35°C, 90°C, and 150°C). Each leg consisted of 32 eGaN FETs, and the drain voltage during stress ranged from 100 V to 130 V in 10 V increments. These tests were conducted on two 100 V devices: EPC2001C and EPC2016C. Note that within the same voltage family of eGaN FETs, the dynamic $R_{DS(on)}$ shift is the same when normalized by the initial $R_{DS(on)}$. A total of 18 such temperature voltage legs were included in the study. During the HTRB stress, the $R_{DS(on)}$ of each part was monitored in situ at regular intervals in time. $R_{DS(on)}$ has a predictable dependence on time, increasing proportionally to the logarithm of the stress time.

$$R(t) = R_0\left(\alpha + \beta \ln[t]\right) \qquad (1)$$

In equation (1), α, β, and R_0 are fit parameters that are extracted from the measured $R_{DS(on)}$ time series for each individual part. Using these fits, it is possible to extrapolate the time at which the $R_{DS(on)}$ will exceed the failure limit, even if this time is well beyond the actual measurement time. Figure 1(a) shows representative data at 150°C.

The (extrapolated) time to fail for each part is indicated by a solid dot in a Weibull plot [9]. The data for each voltage/temperature leg was fit to a 3-parameter Weibull distribution using maximum likelihood estimation (MLE) [10]. The ML estimates also yielded 90% confidence intervals on the fit parameters.

The Weibull fits were used to calculate various statistical quantities such as the mean time to failure (MTTF), and the time at which a certain percentage of the parts are expected to fail (TF%). The latter is shown in Figure 1(b) for three different failure percentages: 1%, 0.01% and 1 ppm. The diamonds indicate the MLE, while the error bars give the uncertainty resulting from the 90% confidence intervals on the Weibull parameters. At 100 V (the max rated V_{DS}), the expected time for 1 ppm failure rate from $R_{DS(on)}$ shift exceeds 20 years.

Figure 1A: Weibull Plots for $R_{DS(on)}$ Failure (150°C)

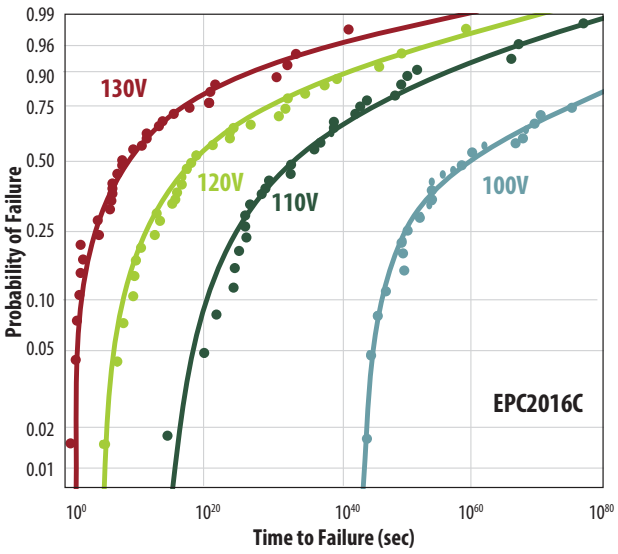

Figure 1(a): Representative Weibull plots for $R_{DS(on)}$ failures under HTRB stress.

Figure 1B: Time to Failure vs. V_{DS} (150°C)

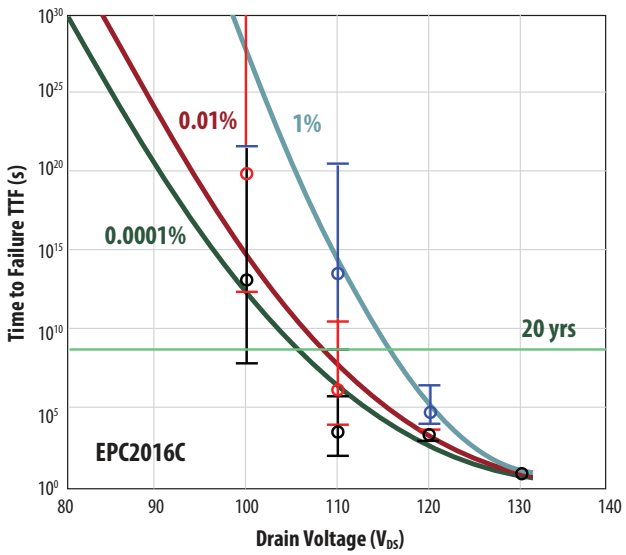

Figure 1(b): Time to failure versus drain voltage. The 20-year line is indicated by green horizontal line.

Fig. 2(a) shows the mean time to failure versus V_{DS} for all three temperature legs in the study. The raw data (resulting from Weibull fits) is indicated by solid dots. The error bars indicate 90% confidence intervals arising from statistical uncertainty in the Weibull fits. The solid lines are 2nd order polynomial fits to the data; these are merely interpolated values and have no physical significance. As can be seen, the failure rate is strongly accelerated by drain voltage and only weakly affected by temperature between 35°C and 150°C. At $V_{DS(max)}$ (100 V), the MTTF is orders of magnitude beyond the 10-year line, independent of the operating temperature. Figure 2(b) shows the failure in time (FIT) rate, derived directly from the MTTF [11]. The FIT rate is below 1 failure per billion device hours at 110 V and is negligibly small at $V_{DS(max)}$.

Figure 2A: MTTF vs. V_{DS} and Temperature

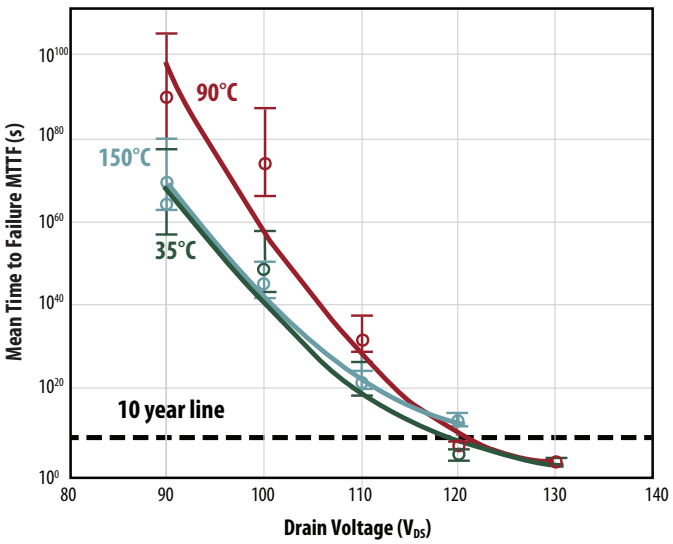

Figure 2(a): Mean time to failure versus drain voltage and temperature during HTRB stress (EPC2001C). The dashed green line indicates 10 years.

Figure 2B: Fit Rate vs. V_{DS} and Temperature

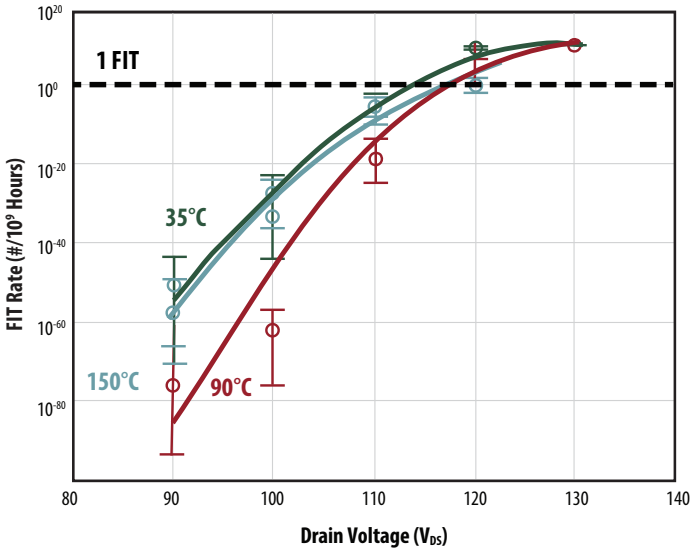

Figure 2(b): Failures in Time (FIT) rate versus V_{DS} and temperature (EPC2001C). Units are expressed in number of failures per billion device-operating hours.

Gate Acceleration

There are several mechanisms that can contribute to failure during HTGB stress at high gate voltage. These included dielectric failure, gate sidewall rupture, and an increase in off-state drain leakage resulting from gate stress. The dominant gate failure mechanism for eGaN FETs is an increase in off-state drain leakage induced by extended operation at high gate voltage and is highly accelerated with gate voltage.

To determine the voltage acceleration of HTGB failure, a matrix of tests was conducted at voltages between 6 V and 6.7 V, all at a temperature of 150°C. Note that this voltage range is outside of the safe operating range of less than 6 V for eGaN FETs. Each voltage leg consisted of 32 parts, and parts were post-screened at three increments: 24 hrs, 100 hrs, and 200 hrs.

The data was analyzed using the same methods as described for the HTRB acceleration study. Raw time to failure was fit to a Weibull distribution for each voltage leg. Using the MLE parameter (and confidence intervals), the MTTF and FIT rate versus V_{GS} was calculated. These are shown in Figure 3(a) and 3(b) respectively. The green line interpolating the data is a best-fit exponential acceleration function. This was not chosen on a priori theoretical grounds, but it does provide a reasonable fit to the data.

With the use of this acceleration function, the MTTF can be predicted at gate voltages within the normal safe operating range. At 6 V (the datasheet limit), the MTTF is well above 10 yrs at 150°C. To predict the time to failure at a specified probability level (e.g. 1%, 0.1%), further data must be collected to refine the Weibull fits.

Figure 3A: MTTF vs. V_{GS}

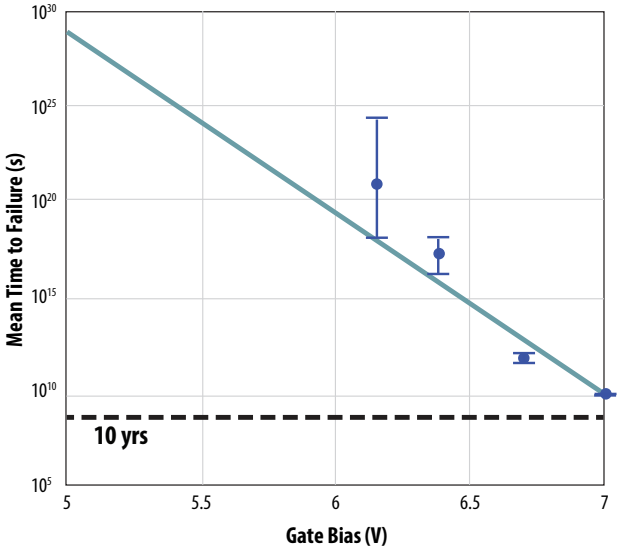

Figure 3(a): Mean time to gate failure versus gate voltage at 150°C. 10 years is indicated by the dashed black line.

Figure 3B: FIT Rate vs. V_{GS}

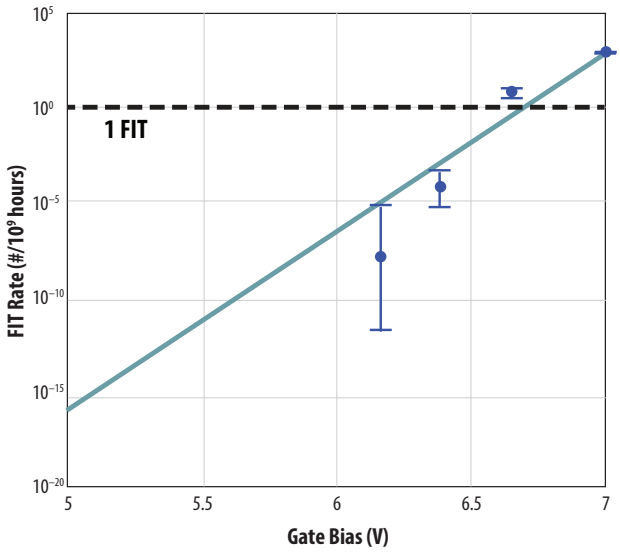

Figure 3(b): Failure in time (FIT) rate versus gate voltage at 150°C.

SUMMARY

A conventional power package such as a TO220, LFPAK, or SO8 is needed to protect a silicon-based vertical power device from the environment. EPC's eGaN FETs are produced in a chipscale, or "flip-chip" format that eliminates the inefficiencies of conventional semiconductor packaging. Package-related parasitic resistance and inductance are eliminated. There are also fewer thermal interfaces that improve the thermal resistance of the eGaN FET compared with comparable MOSFETs [12,13].

Even more significant is the elimination of all the potential reliability problems that have been experienced over the lifetime of the silicon power MOSFET. Wirebonds are gone. Epoxy delamination is gone. Die cracking experienced during the package molding and trimming process is gone. The designer now has a product with minimum waste and fewer mechanical elements to fail.

To demonstrate this significant improvement, eGaN FETs have been subjected to a wide variety of standard stresses for device qualification. These tests included High Temperature Reverse Bias, High Temperature Gate Bias, High Temperature Storage, Temperature Cycling, High Temperature High Humidity Reverse Bias, Autoclave, Moisture Sensitivity, and Electrostatic Discharge. The eGaN FETs tested covered voltages of 40 V, 100 V, and 200 V. Parts were stable under the stress conditions and are fully qualified for the die size covered by the device test matrix.

It is worth noting that products were tested well beyond their maximum rated operating limits to further demonstrate the robustness of the technology and the form-factor. Drain-source stress and gate stresses were applied in order to accelerate the known failure mechanisms of the transistor. These tests have further shown that the eGaN FET products are able to operate with very low probability of failures within the reasonable lifetime of end products manufactured today.

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