

Benchmark DC-DC Conversion Efficiency with eGaN FET-Based Buck Converters



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For applications requiring high power density and high power, but not requiring electrical isolation, the buck converter has been the work-horse topology for many years. Computers, servers, telecom equipment, satellites, medical equipment, and industrial equipment all use these simple, low cost, high performance DC-DC converters to power a wide variety of loads – mostly high performance digital ICs such as microprocessors, memory, DSPs, and ASICs of all types. Improvements in buck converters over the past few years have been limited by the power MOSFET's sedate switching speeds which, in this "hard-switched" topology, translates into lower power conversion frequencies (size and cost), lower efficiency (size and cost), and lower V_{IN}/V_{OUT} ratios (less efficient power management systems). In this paper we show that eGaN FETs unlock a new spectrum of performance that can be translated into significant power conversion system cost and performance improvements [1,2].

EGAN® FET PERFORMANCE IN HARD SWITCHING CIRCUITS

To drive frequency higher in a buck converter, especially at a high input voltage, power devices must have very low dynamic losses. The dominant component to the dynamic losses is the classic hard switching event where current commutates to the device turning on before the voltage across that device collapses. This event is shown in figure 1, and is reversed during turn off of the high side device. The energy of each switching period is approximated by; $E_{SW} = V_{IN} \times I_{OUT} \times t$, where t is determined by the various components of the device gate charge (Q_G), device series gate resistance (R_G), driver impedance, drive voltage, inductance common to the power and the drive loops, and device transfer characteristics. Due to eGaN FETs requiring much less die area and having a lateral structure, they have ultra-low gate and Miller charges (Q_{GD}). This, combined with a gate electrode designed to have low R_G , make switching times for these devices very short, and energy dissipated due to classical hard switching very low.

There are four additional components that contribute to dynamic losses. These include diode recovery charge (Q_{RR}) where the energy loss (E_{RR}) is equal to the recovery charge times the input voltage. A second is the output charge (Q_{OSS}) which has an energy loss (E_{OSS}) determined by multiplying one-half of the output charge times the input voltage. Third, the energy loss (E_G) associated with the gate charge (Q_G) is calculated as the gate charge times V_{GS} . The fourth contributor to loss in energy is the reverse conduction voltage (V_{SD}) and it is determined by the following equation: $E_{SD} = V_{SD} \times I_{OUT} \times t_R$ (where t_R is the total reverse conduction time).

To determine the total energy loss, or power dissipation, the sum of these individual four components combined with the energy loss in each switching period is multiplied by the frequency.

$$P_{DYN} = f \times (E_{SW} + E_{RR} + E_{OSS} + E_G + E_{SD})$$

eGaN FETs, unlike standard power MOSFETs, have no minority carriers to be stored in a junction, and therefore no Q_{RR} . The output capacitance, C_{OSS} , and charge, Q_{OSS} , is also smaller because eGaN FETs are physically smaller than MOSFETs of comparable $R_{DS(ON)}$. Both V_{GS} and Q_G are low, so E_G is negligible for eGaN FETs. Finally, due to the reverse current conduction mechanism, eGaN FETs have a high V_{SD} when compared with the body diode forward voltage of a MOSFET. This condition has the potential to increase the energy loss E_{SD} and is influenced by the total reverse conduction time, a condition that can be controlled by the time that the rectifier-switch is acting like a diode [4].

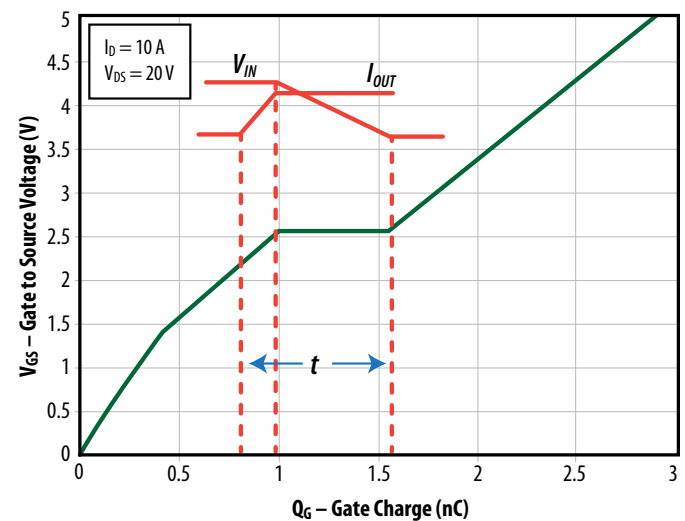


Figure 1: Classical hard switching waveform.

BUCK CONVERTERS

The basic buck converter circuit is shown in figure 2. The higher the ratio of input voltage (V_{IN}) to output voltage (V_{OUT}), the greater the benefits of using eGaN FETs become, since most of the components contributing dynamic losses are related to V_{IN} . This voltage is converted down to the required voltage, often powering a microprocessor, memory or other power-bus voltage using a single stage buck converter.

Four different eGaN FET based buck converter designs were compared against state-of-the-art MOSFET counterparts to demonstrate the improvements that can be expected over a wide range of operation.

- 1) $48 V_{IN} - 1.2 V_{OUT}$
- 2) $19 V_{IN} - 1.2 V_{OUT}$
- 3) $12 V_{IN} - 1.2 V_{OUT}$ with 2 parallel eGaN FETs
- 4) $60 V_{IN} - 10 V_{OUT}$

Measurements were taken at frequencies from 300 kHz up to 1 MHz.

$48 V_{IN} - 1.2 V_{OUT}$ BUCK CONVERTERS

Now that there is a FET that can switch reliably and with low loss in less than 10 ns [3], many of the limitations and problems created by the minimum on-time of today's silicon MOSFETs vanish. Small and efficient high-ratio single-stage step down converters can now be built. Converting 48 V to load voltages such as 1.2 V, or converting 12 V to 0.7 V in one stage is possible. We will first look at this extreme case of a 48 V – 1.2 V single stage converter, followed by other, less extreme examples.

The silicon transistors that were selected are representative of the best generally available in the market today. Another criterion was to match as closely as possible the on-resistance and current rating of the silicon and eGaN devices. Table 1 gives a summary of the key characteristics of the transistors used in this buck converter comparison.

There are a few key points to understand in this comparison. First, the gate charge of the silicon devices is many times that of the eGaN FETs. The silicon control FET requires 18 nC to switch; the eGaN FET only requires 2.7 nC. This 6:1 ratio means the eGaN FETs will have a substantially lower switching loss. The synchronous rectifier FETs also have a large difference in total gate charge, but the losses tend to be dominated by device $R_{DS(ON)}$.

Secondly, due to the much lower gate capacitance, the standard figure-of-merit (FOM) of the eGaN FETs is three to six times better than that of the MOSFETs.

Lastly, note the PCB area required by the devices. The silicon devices require 61.5 mm² of board space. The eGaN FETs only require 8.5 mm². The MOSFETs require seven times the PCB area of the eGaN FETs. The savings in board space by the eGaN FETs will be a significant savings in a system with many voltage rails.

Figure 3 is a comparison between the eGaN FETs and the MOSFETs operating at 500 KHz. Also plotted in this figure is the efficiency for the MOSFET-based buck converter operating at 300 kHz. The eGaN FET-based converter

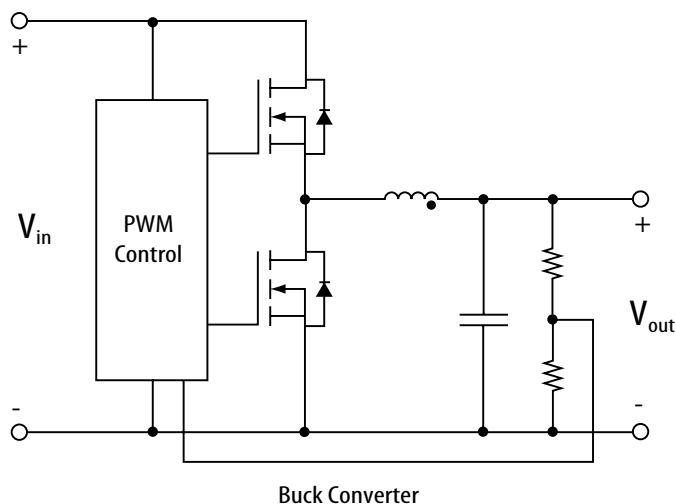


Figure 2: Basic buck converter circuit.

	Part Number	V_{DS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (mΩ)	Q_G (nC)	Q_{GD} (nC)	Rectifier FOM (mΩ-nC)	Switching FOM (mΩ-nC)	Package Type	PCB Area (mm ²)
Silicon Control FET	Si7850	60	8.7	25	18	5.3		132	PowerPAK SO-8	31.7
Silicon Sync FET	RJK0652	60	35	6.5	29	8.8	189		LFPK	29.8
eGaN Control FET	EPC1007	100	6	24	2.7	1		24	LGA	1.8
eGaN Sync FET	EPC1001	100	25	5.6	10.5	3.3	59		LGA	6.7

Table 1: MOSFETs and eGaN FETs used in the 48 V – 1.2 V buck converter

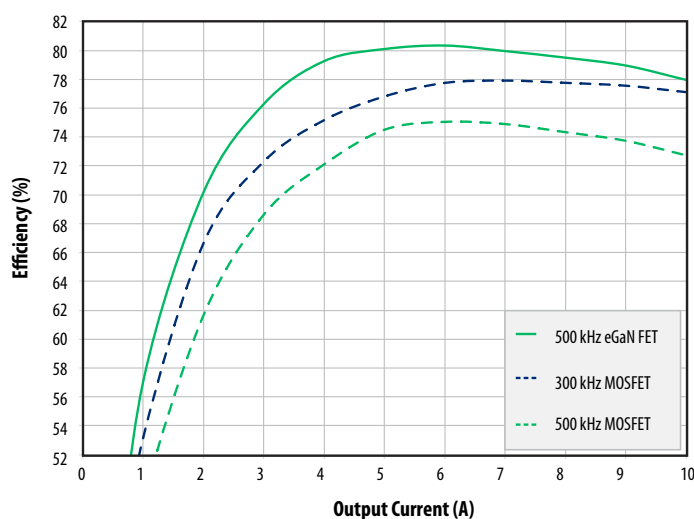


Figure 3: 48 V – 1.2 V efficiency vs. output current comparing 100 V EPC2001 eGaN FETs against state-of-the-art 60 V silicon MOSFETs.

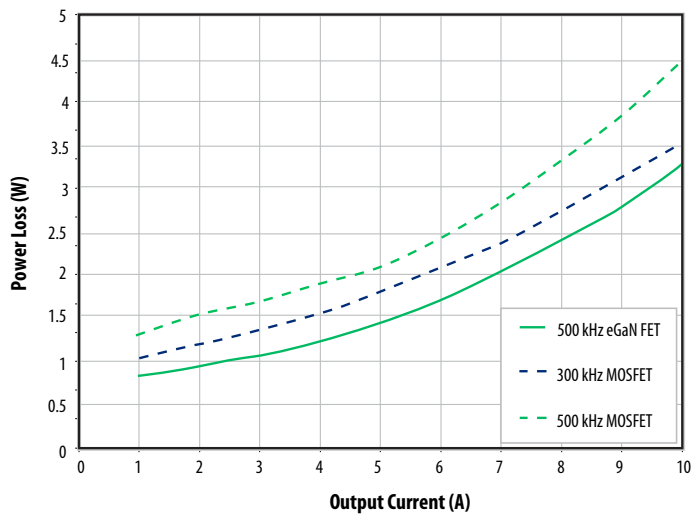


Figure 4: 48 V – 1.2 V losses vs. output current comparing 100 V EPC2001 eGaN FETs against state-of-the-art 60 V silicon MOSFETs.

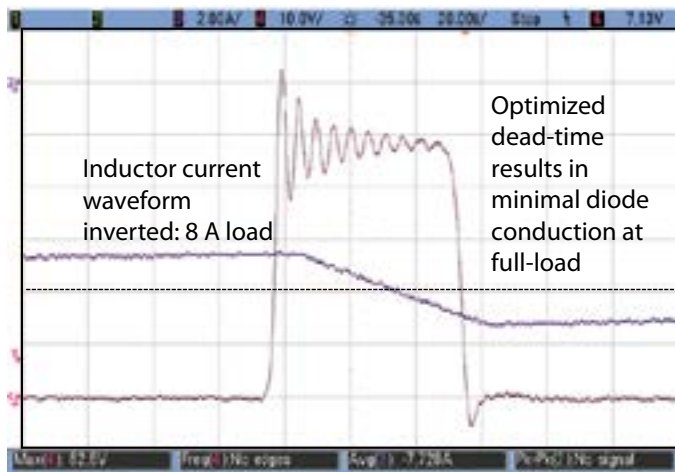


Figure 5: 48 V – 1.2 V eGaN FET-based converter switch node voltage with 500 kHz switching and optimized dead-time.



Figure 6: 48 V – 1.2 V eGaN FET hard switching transition time.

is superior at all frequencies. The data in figure 4 demonstrates that the silicon devices are dissipating about 1 watt more than the eGaN devices at an output current of 8 A.

Figure 5 shows the measured switch node voltage and output current (inverted) of the eGaN FET-based converter switching at 500 kHz with an on-time of about 100 ns. Even at this very short on-time the waveform has nearly vertical edges and flat tops. A controller could easily reduce the on-time by a factor of five in order to maintain control and good transient response during a sudden load reduction.

If the goal is fastest possible switching, figure 6 shows a hard-switched transition where the rise time is about 2.5 ns. This kind of switching speed is unheard of with silicon power MOSFETs.

If the goal is to minimize the losses, figure 7 shows that soft-switching transitions of less than 5 ns are possible. The caveat is that the soft-switching transition time is load dependent.

While these fast transitions enable operation at very high frequencies with good efficiency and small size, they require care in the physical design. With voltages and currents switching in just a few nanoseconds, parasitic capacitances and inductances that are negligible today will not be negligible in an eGaN FET-based system.

19 V_{IN} – 1.2 V_{OUT} BUCK CONVERTERS

In the competitive world of notebook computers, the key performance attributes are battery life, weight, and size (particularly height) for a given level of performance. Recent advances in power MOSFET technology allow significant improvements in efficiency, performance, and size of the point of load (POL) converters used to convert the battery and charger voltage (approximately 19 V in a four-cell system down to the 1.2 V needed for the microprocessor and graphics processors). Pushing frequency higher to reduce the size and cost of energy storage and transmission elements such as capacitors, inductors and transformers has been discussed for many years but, with traditional power MOSFETs, the tradeoff between frequency and efficiency has been too costly to implement commercially. eGaN FETs now make it possible for designers to

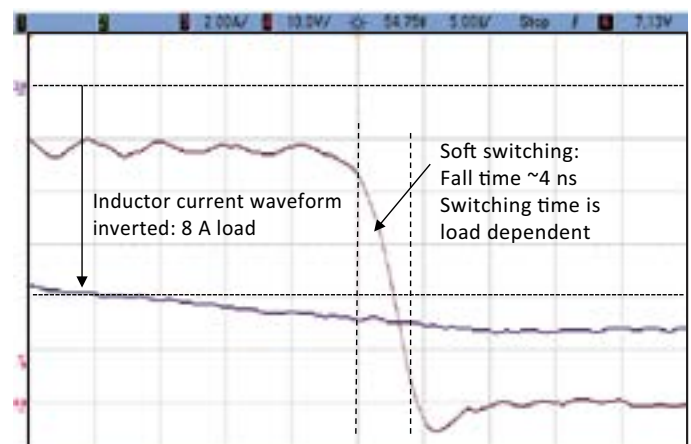


Figure 7: 48 V – 1.2 V eGaN soft switching transition.

reduce the space occupied by their DC-DC converters in 4-cell and industrial systems by increasing frequency while still exceeding the efficiency of converters based on conventional silicon power MOSFETs.

The devices compared were the EPC1014 (40 V, 16 mΩ) on the high side (control) and EPC1015 (40 V, 4 mΩ) on the low side (rectifier), and Infineon MOSFETs BSZ130M03MS (30 V, 15 mΩ) on the high side and BSZ035N03M (30 V, 4.3 mΩ) on the low side. In all cases, a single device was used for each socket. The MOSFETs were chosen as they are state of the art and similar $R_{DS(ON)}$. 40 V eGaN FETs were compared with 30 V MOSFETs because higher overshoot can be expected with the much higher switching speeds of the eGaN FETs. Table 2 shows important characteristics of the switching devices.

Gate drive voltages for all experiments were $5 V_{GS}$ for the ON state, and $0 V_{GS}$ for the OFF state. The converters were run open-loop with the duty cycle adjusted for the appropriate output voltage. The output filter was kept small to take advantage of the space savings enabled by high frequency conversion. For 800 kHz testing, only one output filter capacitor was used, and for 300 kHz testing a 470 μ F PosCap was added. Tests were performed from zero load to 10 A. A baseline was obtained using the same MOSFETs at 300 kHz, a typical switching frequency for this application.

The tests show that the circuit with eGaN FETs running at 500 kHz was comparable to the baseline of MOSFETs at 300 kHz, while the MOSFET circuit saw an efficiency decrease of roughly 1.5% through most of the current range at 500 kHz.

At low current, the efficiency decreases for the eGaN FET solution because the fixed dead-time was minimized for optimal high current operation. This resulted in the loss of the zero-voltage switching (ZVS) advantage at light loads. However, when the dead-time was increased, as an adaptive type driver would do, the 500 kHz efficiency of the eGaN FET system became comparable to that of the 300 kHz MOSFET system under all load conditions.

Between the size reduction of the power switches and the elimination of the PosCap, the increased frequency capability of the eGaN FET system realized a saving of 36 mm² of board space (about 20%) with no efficiency penalty. Efficiency results can be seen in figure 8.

The frequency was then increased to 800 kHz on the eGaN FET-based system, and output filter reduced to maximize board space savings. Even with the higher switching speeds, overshoot was limited to 33 V, and ringing was mostly damped in only a few cycles as shown in figure 10.

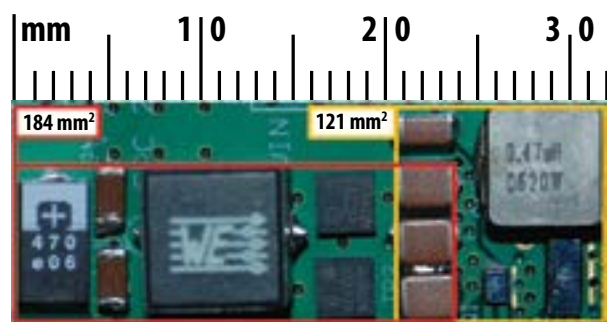


Figure 9: 19 V - 1.2 V size comparison between MOSFET-based buck converter (RED) and eGaN FET-based converter (yellow).

	Part Number	V_{DS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (mΩ)	Q_G (nC)	Q_{GD} (nC)	Rectifier FOM (mΩ-nC)	Switching FOM (mΩ-nC)	Package Type	PCB Area (mm ²)
Silicon Control FET	Si7850	60	8.7	25	18	5.3		132	PowerPAK SO-8	31.7
Silicon Sync FET	RJK0652	60	35	6.5	29	8.8	189		LFPACK	29.8
eGaN Control FET	EPC1007	100	6	24	2.7	1		24	LGA	1.8
eGaN Sync FET	EPC1001	100	25	5.6	10.5	3.3	59		LGA	6.7

Table 2: MOSFETs and eGaN FETs used in the 19 V - 1.2 V buck converter.

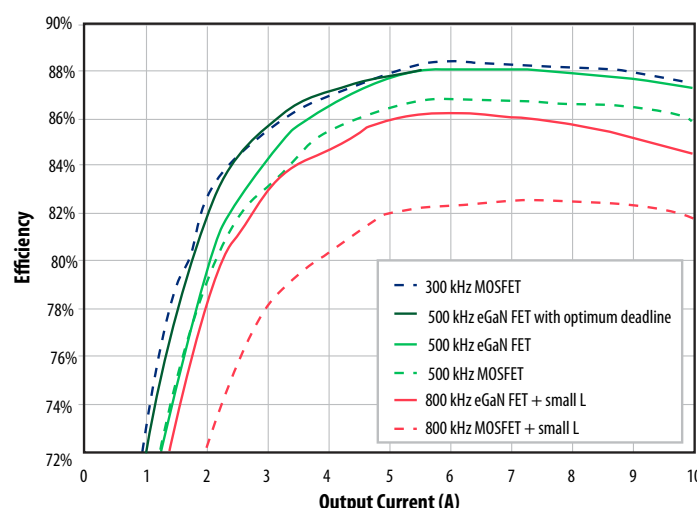


Figure 8: The 19 V - 1.2 V efficiency vs. output current comparing 40 V eGaN FETs against state-of-the-art 30 V silicon MOSFETs.

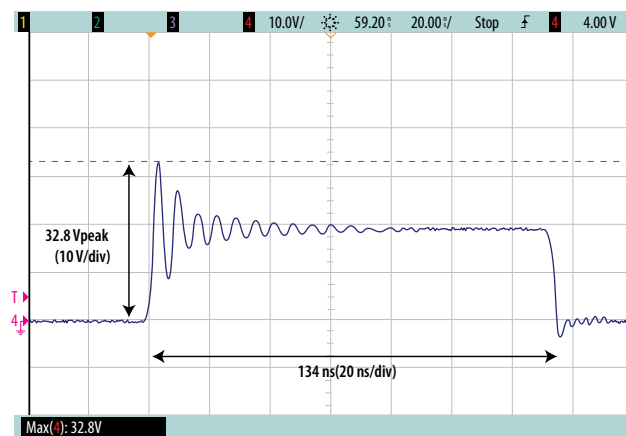


Figure 10: 19 V - 1.2 V switch-node wave form showing control eGaN FET on-time at 500 kHz, 10 A.

The result was impressive. Efficiency over most of the current range stayed within 1% of the 500 kHz MOSFET system. The peak efficiency was over 86%, and the board space saved was 30 mm² (an additional 20%). Board space requirements are compared in figure 9. This 33% space savings can be translated into a reduced size and cost for the multi-layer printed circuit board or into increased system performance by using that space for processing power and memory.

Modern DC-DC converters have limits on the voltage variation both in terms of transients and ripple. Increasing frequency allows the output filter to be reduced while still maintaining a low ripple. The output filter components in these experiments were reduced to keep voltage ripple reasonably constant at about 12 mV peak-to-peak (1% of DC voltage). Figure 11 shows the output voltage ripple waveforms for 300 kHz, 500 kHz, and 800 kHz operation.

PARALLELED eGaN[®] FETS IN A 12 V_{IN} – 1.2 V_{OUT} BUCK CONVERTER

At higher output currents, it is common for a designer to parallel transistors. In reference 13 the key considerations for paralleling the ultra-fast eGaN FETs were discussed. To evaluate the performance difference between paralleled MOSFETs and eGaN FETs, a buck converter was designed with an input voltage up to 19 V and output of 1.2 V. The circuit uses the Linear Technology buck regulator LTC3833 IC [5] for both designs. The Texas Instruments LM5113 eGaN driver [6] was added to the eGaN FET version of the converter to provide gate drive compatibility.

Two variations in the layout design of the eGaN version buck converter were made and are shown in figure 12. The variations are a single FET version and dual paralleled FET version; the paralleled device being the synchronous rectifier. The layout of the paralleled version was based on evaluation design E from reference 13.

Figure 13 shows photos of the buck converters built for the comparative evaluations[†]. The eGaN FET boards are approximately 2" x 2" and the yellow dotted line indicates the footprint area of the converter itself.

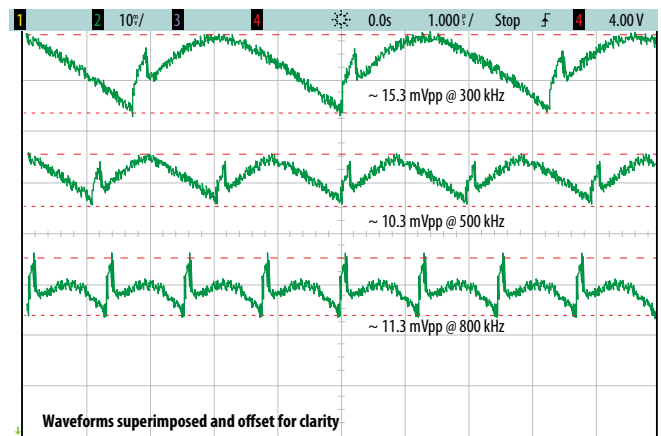


Figure 11: 19 V - 1.2 V output voltage ripple waveforms.

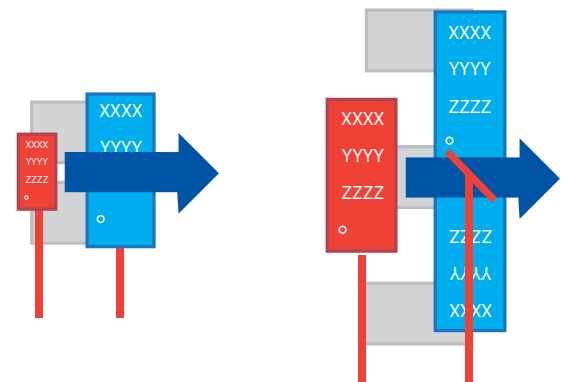


Figure 12: eGaN FET synchronous rectifier buck converter layouts for parallel evaluation.

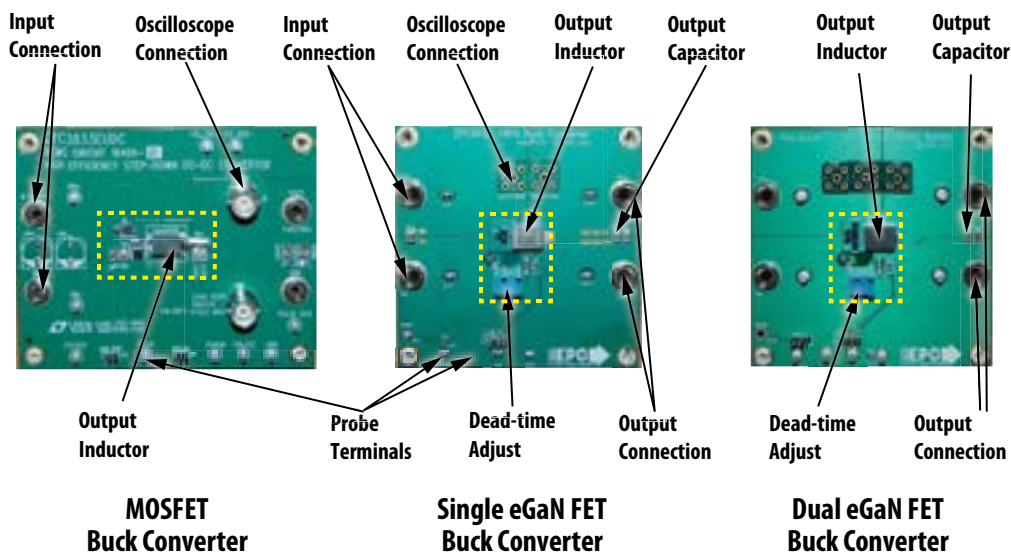


Figure 13: Photo of the evaluation buck converters. MOSFET version (left), single eGaN FET version (center), and dual eGaN FET version (right).

[†]The best theoretical design discussed in reference 13, "Design B," was not selected for this evaluation because, at the time of the design, we did not realize its superior attributes.

The MOSFET version of the synchronous buck converter was evaluated using the Linear Technology demo board DC1640A [7]. The converters' design summaries are given in table 3.

The inductance values given in table 3 are only for the synchronous rectifier FET as these were the only devices paralleled in the dual FET versions. By measuring the oscillation frequency of the gate voltage at the gate of the devices using specially designed probes within the PCB, and having low gate driver resistances ($<0.5\ \Omega$), the gate inductance could be calculated from the first order resonance equation using the value of the gate-source capacitance. Using the dimensions between the two device sources, the inter-device source inductance could be calculated using the flat conductor inductance formula [8]. The length of the inductor was given as the distance between two source pads closest to each other and the width of the conductor as the width to the via sets. The thickness was given as the conductor thickness.

Both converters were operated at a switching frequency of 1 MHz and with 12 V on the input. The MOSFETs [9,10] selected were based on physical fit into the demo board and having a similar gate threshold voltage as the eGaN FETs [11]. All the converters were built using the same output inductor, a Würth 744308025 250 nH, 370 $\mu\Omega$, and four paralleled 100 μF ceramic 1206 size output capacitors.

Figure 14 shows the efficiency measurements for each of the converters over a wide load current range. The results clearly show the superior efficiency performance of the eGaN FET-based converter over the MOSFET equivalent. This efficiency improvement is despite the near double $R_{\text{DS(ON)}}$ value the eGaN FET when compared to the MOSFET. The MOSFET version efficiency is further negatively affected by the 30 ns of body diode conduction inherent in the controller.

	Single FET Design	Dual FET Design
eGaN	EPC2007/ EPC2001	EPC2001/ 2x EPC2001
MOSFET	BSZ130N03MS / BSZ035N03MS	BSZ035N03MS / 2x BSZ035N03MS
Gate inductance eGaN FET [nH]	3.2	6.8
Gate inductance MOSFET [nH]	10.4	12.8
Source inductance eGaN FET [pH]	120	286
Source inductance MOSFET [pH]	1320*	1100*
di/dt limit eGaN [A/ns]	17.7	7.4
di/dt limit MOSFET [A/ns]	1.7	2.0
dv/dt limit eGaN [V/ns]	11.5	5.6
dv/dt limit MOSFET [V/ns]	9.7	6.2

* Includes inductance internal to the MOSFET package.

Table 3: Summary of 12 V - 1.2 V conversion MOSFET and eGaN FET converter design characteristics.

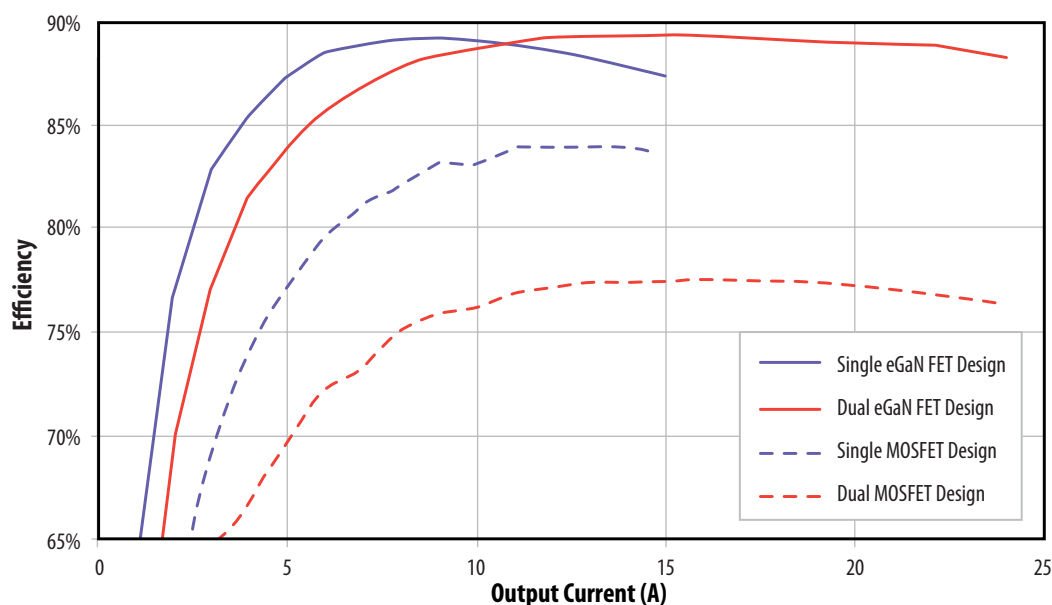


Figure 14: 12 V - 1.2 V efficiency vs. output current at 1 MHz.

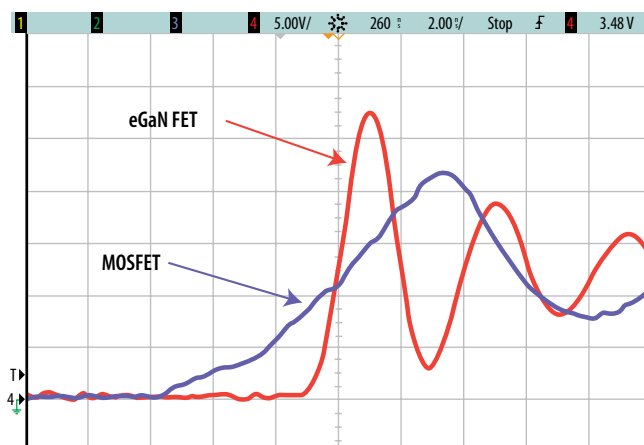


Figure 15: 12 V - 1.2 V conversion measured waveforms for the single device buck converter.

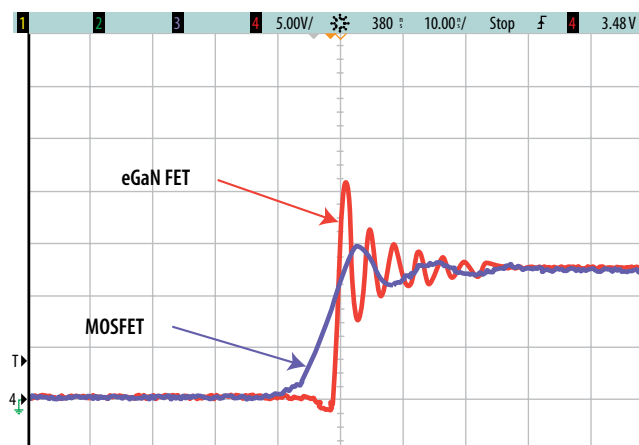


Figure 16: 12 V - 1.2 V conversion measured waveforms for the dual device buck converter.

The switching voltage node waveforms for each of the buck converters are shown in figure 15 and figure 16 for the single device and dual device converters respectively.

The dv/dt for each of the converters was also measured and the results given in table 4. In the dual eGaN FET case, the dv/dt is higher than predicted for immunity as calculated in reference 13. The fact that the measured dv/dt is higher than the predicted immunity does not indicate that any parameter of the eGaN FET is exceeded. The gate can experience a negative voltage spike during turn-off that can improve the Miller capacitance ratio. The designer must measure and look for signs of unwanted turn-on on the waveforms. One of these signs may be a small bump during the transition period on the drain-source voltage.

It should be noted that paralleling of FETs for the synchronous rectifier switch of a buck converter is a special case as described in [12]. This case has favorable conditions for the FET making it much less susceptible to source inductance than in the case of other types of converters and switches. Reference [12] goes as far as to indicate that increased source inductance up to a point may even be beneficial.

60 V_{IN} – 10 V_{OUT} BUCK CONVERTERS

To explore a different voltage range, a buck converter for 60 V to 10 V conversion at 10 A was built using the LM5113 driver IC. This circuit was compared at 800 kHz versus a MOSFET design running at 500 kHz. Once again, the eGaN FET solution completely enveloped the MOSFET solution.

	Single FET Design	Dual FET Design
eGaN FET design measured dv/dt [V/ns]	12	10
MOSFET design measured dv/dt [V/ns]	2.2	1.2

Table 4: Measured dv/dt for each of the design examples (12 V - 1.2 V)

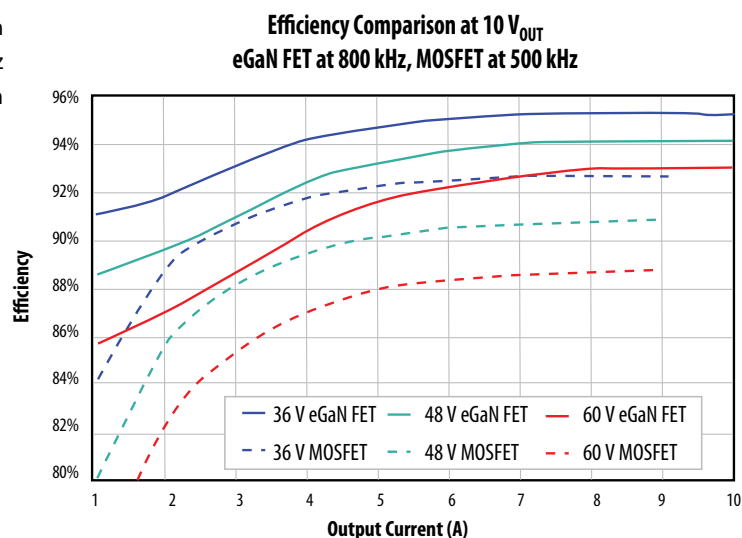


Figure 17: The 60, 48, and 36 V – 10 V efficiency vs. output current comparing 100 V eGaN FETs against state-of-the-art 60 V silicon MOSFETs.

SUMMARY

As illustrated in figure 18, eGaN FET-based buck converters can improve efficiency compared with power MOSFETs over virtually the entire spectrum of V_{IN}/V_{OUT} ratios and operating frequencies.

We have also demonstrated significant system size reductions without loss of efficiency, as well as significant space savings by driving frequency from the traditional 300 kHz up to 1 MHz. By using eGaN FETs, power conversion system designers now have a new opportunity to reduce system size and enhance efficiency while reducing overall system cost.

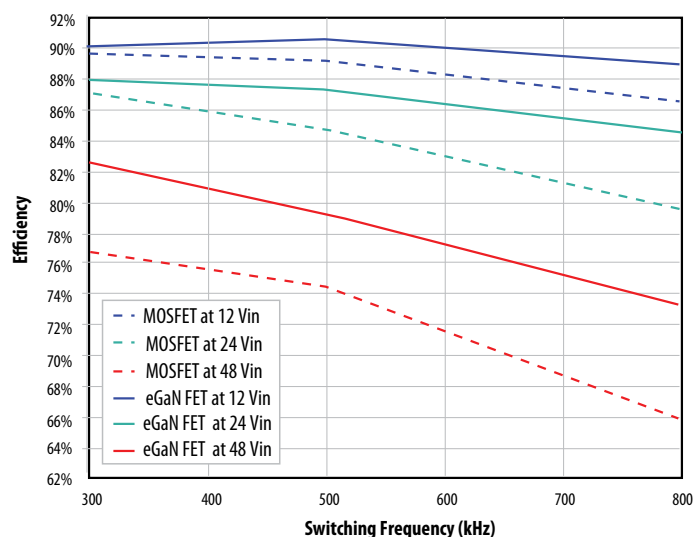


Figure 18: 1.2 V_{OUT} buck converter efficiency using eGaN FETs at various input voltages and various frequencies compared against state-of-the-art silicon MOSFETs.

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