Digital Interfaces and EMC Performance

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The increasing demand for the transfer of higher volumes of information and the evolution of techniques allowing faster transfer of data between devices have had an important influence in the development of digital interfaces and signaling standards that allow internal and external data transfer at faster speeds.

There are two major driving forces in the development of data transfer and encoding methods. The first driving force is the convergence of PC and multimedia technologies. Second is the increasing need for interoperability between different and more capable digital multimedia devices able to interconnect and exchange digital content.

Trend of Digital Interfaces

Supported by the increasing computing capabilities, processor speeds, and storage capabilities, we have witnessed over time the introduction of various types of interfaces, some of them aimed at specific applications and some of them for general purposes (see Figure 1). Low voltage differential signaling (LVDS) found its main application in data transmission between the graphics processor and the LCD panel (internal application), while SATA technology is aimed at storage applications (can be internal or used externally through the eSATA extension), and DVI, HDMI and the latest Display Port are technologies aimed at the digital displays field and which are expected to coexist for some time.

Figure 1: Digital interfaces

A predominant factor that drives digital interface development is the data transfer rate (see Figure 2). This is reflected in faster movement of data in the case of USB, FireWire (IEEE1394), better resolution of images and audio in the case of DVI, HDMI, and Display Port. An important technological factor that has allowed the transmission of high speed digital signals is the advent of the differential data transfer signaling method. This has definitely marked a departure from the traditional parallel data flow and its limitations.

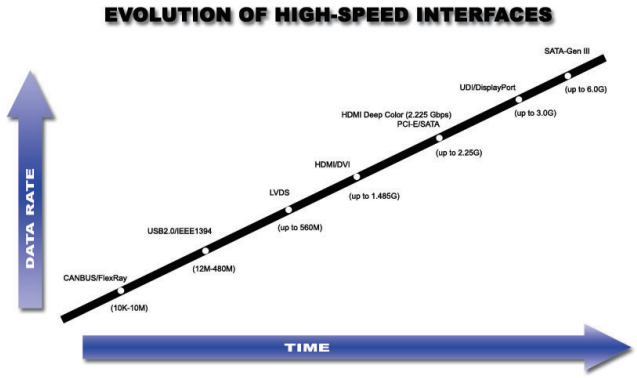


Figure 2: Evolution of various digital interfaces in the PC industry

All of the aforementioned digital interfaces use some type of signaling method based on differential pair transmission. The differential signal transmission method allows the serialization of packets of data which are then transmitted over a pair of traces or wires.

LVDS (Low Voltage Differential Signaling)

The differential signal transmission method allows the serialization of data and its transmission over a pair of PCB traces or wires. This is also called a double-ended system, and is represented as in the diagram in Figure 3.

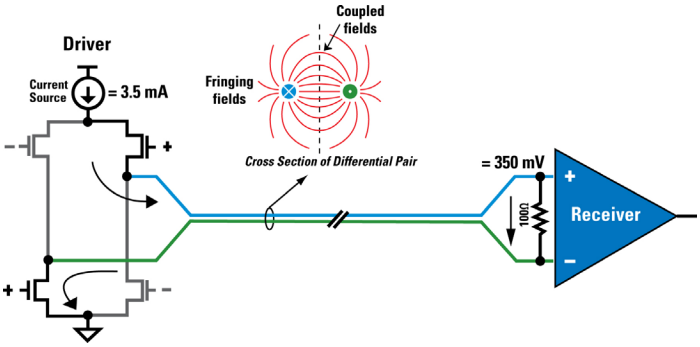


Figure 3: Simplified diagram of LVDS driver and receiver via 100Ohm differential impedance media[1] (Reprinted courtesty of National Semiconductor)

When the driver switches, it changes the direction of the current flow across the resistor, creating a valid "one" or "zero" logic state. The receiver has high DC

input impedance; therefore, the majority of the driver current (about 3.5mA in the above example) flows across the 100 Ohm termination resistor, generating about 350 mV across the receiver input. This creates a differential current flow across the pair. Because of the low voltage swing from one logic level to the other, the transition times between logic states are short, allowing high switching speeds without affecting the signal integrity.

Some of the attributed benefits of the differential mode signaling are:

- The timing of the signals can be more precisely defined, and the crossover point of the differential signals is easier to control, than the absolute voltage relative to some other reference (as in the case of single ended lines);
- Higher speeds of data transmission are possible, due to the low swings in voltages;
- Greater signal to noise ratios, due to the fact that the resulting signal is twice the magnitude at the receiver;
- Differential mode noise is cancelled out, due to the opposite magnitudes (layout traces will be key to this).

The actual implementation of differential pair in the various types of interfaces varies, but the general topology is as indicated in the diagram shown in Figure 4 for practical proposes. In general, it is composed of a source, a physical medium, a receiver (or sink), and a control protocol.

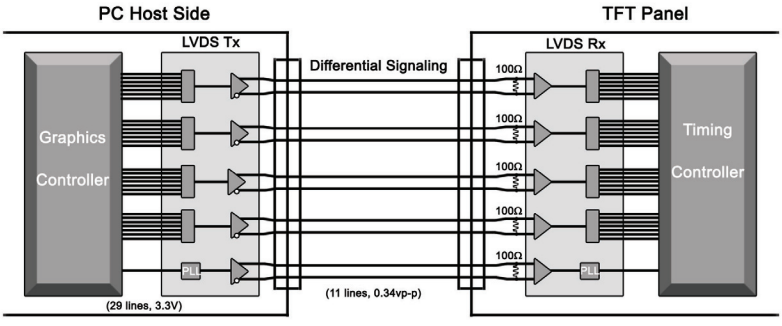


Figure 4: Simplified differential mode signal method

Differential Mode and Common Mode Noise in Differentials Signals

There is an important basic principle about the generation and emission of noise in differential signals. Since differential mode signals are transmitted in opposite phases, any differential noise (traveling opposite direction through the D+ and D- lines) is cancelled out. This represents an advantage because of the low risk of EMI emissions (see Figure 5).

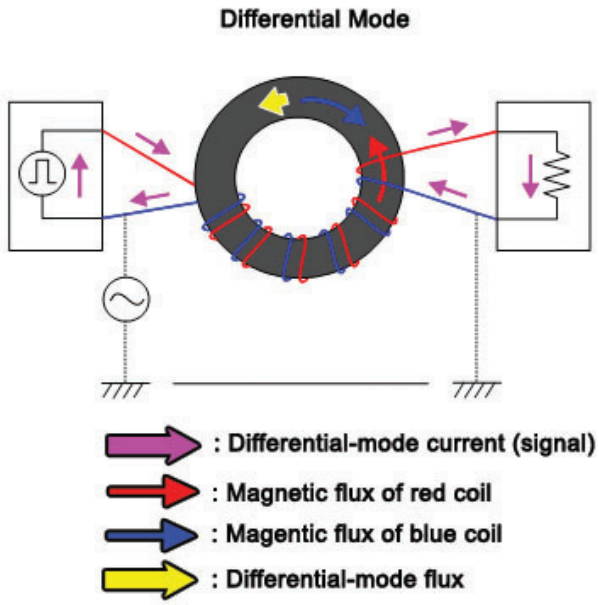


Figure 5 : Differential mode signal and noise cancel mechanism

Common mode noise on the other hand (which travels in the same direction through D+ and D- lines), normally returns to the source via a common ground route (see Figure 6).

Ideally, the differential transmission scheme represents high immunity to differential noise, and high rejection to the common mode noise. In real life design, and because of the nature of the different components involved, some level of common mode noise is always present, which might contribute to EMI emissions. The sources of common mode noise can be complex to determine, and can have a number of potential sources in the actual circuit.

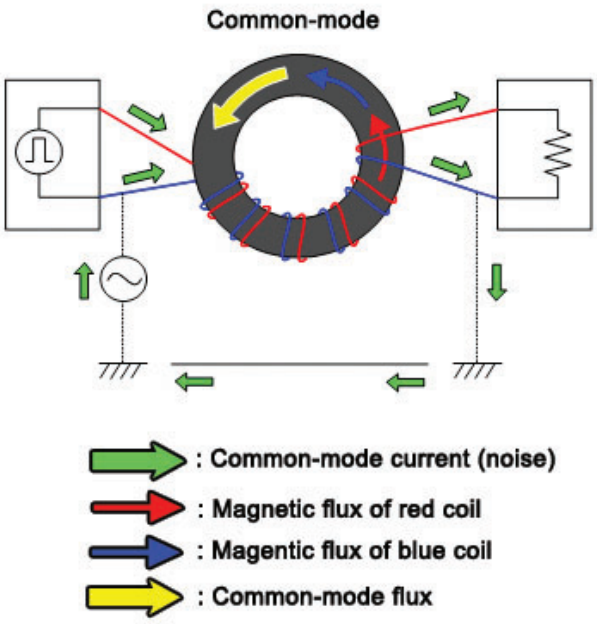


Figure 6: Common mode signal and noise re-enforcement mechanism

Signal Integrity

As speeds increase, the performance of the differential pair represents more challenges to the designer, since the operating conditions of the signals occur under tighter constraints. As data rate increases, the unit interval (UI) is reduced, requiring tighter control of the signal quality to avoid data errors.

Design Considerations for EMC Performance

Despite the good characteristics of the differential signals, it is important to note some of the general challenges that the designer faces when using a differential type of design, including:

a. Common mode noise—which leads to potential errors clock and data;

b. Imbalances between the conductors of each pair—potentially creating signal reflections;

c. The coupling between conductors of each pair.

A solution or mitigation to these issues can be found through the use of passive components that meet the following requirements:

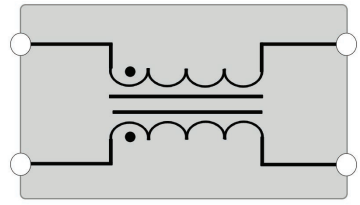
- Good passing characteristics of the differential data signals without attenuation from the source to sink devices;
- Present high impedance to high frequency common mode noise;
- Match the required differential impedance (through its characteristic impedance) to maintain proper balance.

The common mode filter has proven to be effective in the improvement of these challenges. Its construction and operating conditions can be adjusted to ensure that a particular design meets the tight requirements of EMI compliance and signal integrity.

The common mode filter is a passive component constructed with 2 parallel windings over a ferrite material core.

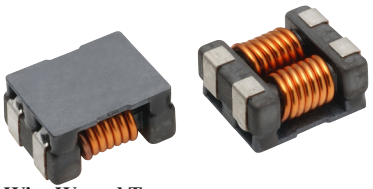
Some of the critical characteristics to be considered in high speed application are:

- Characteristic impedance, similar to the TMDS (in the range of 100 Ohm) in the case of HDMI;

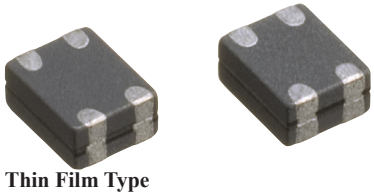


Nondirectional

Circuit Representation



Wire Wound Type



Thin Film Type

Figure 7 (a-c): Common mode filter symbol and types

- Its insertion loss (which provides the EMI emissions characteristic reduction for a specific frequency range);

There is also the possibility of choosing between wire wound and thin film technology (multilayered type) which typically provide similar electrical characteristics.

However, the thin film type provides more design space flexibility, due to its small profile (see Figure 7).

The Common Mode Filter as a Noise Suppressor and Signal Integrity Solution

For purposes of this analysis, we will use the HDMI application to showcase the effect of a common mode filter in the improvement and countermeasure of typical noise and signal integrity issues often encountered in high speed interfaces designs.

As mentioned earlier, HDMI signal transmission system utilizes a method called TMDS (transmission minimized differential signal), which is a variation of the LVDS1 method (see Figure8).

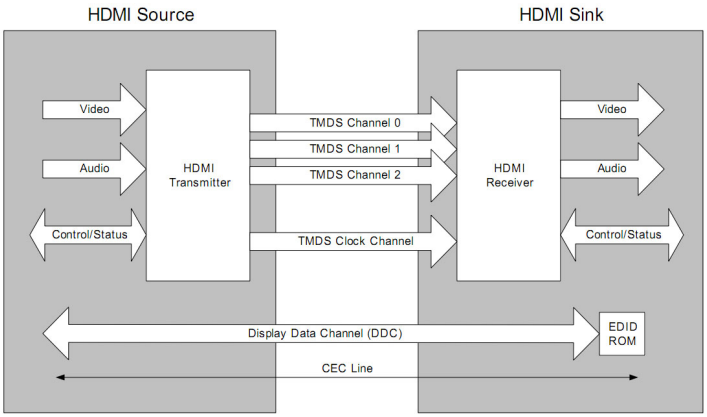


Figure 8: HDMI TMDS basic block diagram1

The HDMI test specification 1.3 defines specific criteria for signal integrity and impedance matching conditions for HDMI circuit through the compliance test specification (CTS) document. The CTS specification breaks down the test into its major system components (source, medium, sink and protocol).[1]

In the following cases, special test set-up and fixtures have been used to obtain real-life validation of the solutions (which is the intention of this article), and will be referring mainly to the source, and sink areas of the system (see Figure 9).

EMI Suppression

One common source for EMI noise generation can be the internal signal clock. For example, at 480p resolution (clock=27MHz), the EMI level might be very low. However, if the resolution increases to 1080p (HDTV resolution with clock=148.5 MHZ), the EMI level increases considerably. This is one of the main challenges that the designer faces in the PCB design.

The main characteristic to be considered for the common mode filter is the cut-off frequency (typically specified at -3db). In the case of HDMI, -3 dB at 6 GHz is the target specification. A wire wound or thin film technology CMF can provide similar performance (see Figure 10).

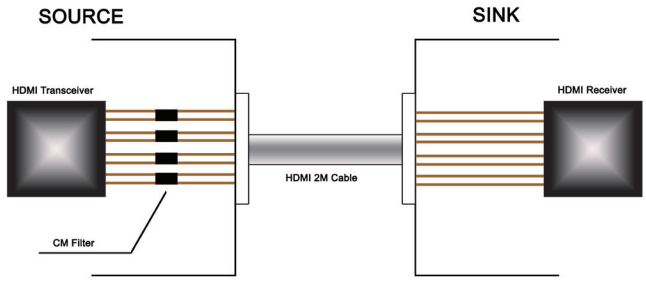


Fig 9: HDMI TMDS basic test set-up

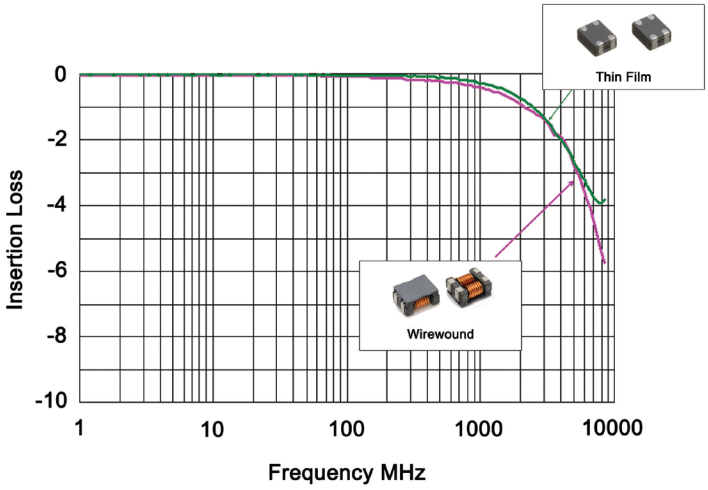


Figure 10: Insertion loss versus frequency chart of common mode filters for 1080p resolution application

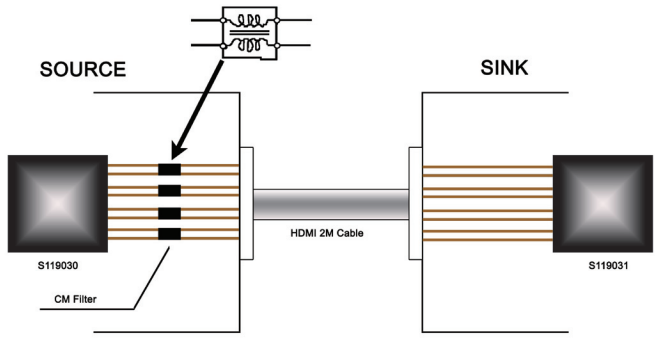


Figure 11: Common mode filter connection drawing

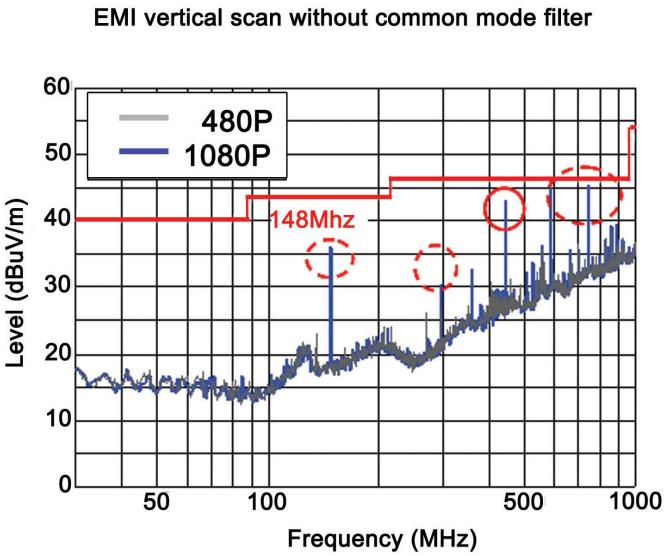


Fig 12: EMI scan comparing 480p and 1080p video resolution emissions (at 1080p resolution the EMI level is considerable higher than 480p)

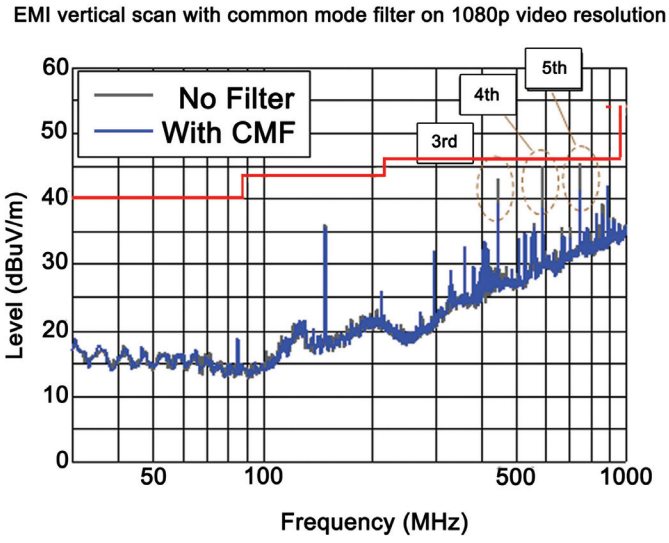


Fig 13: EMI Scan using 1080p resolution (the contribution of the common mode filter is more visible in reducing the high frequency harmonics)

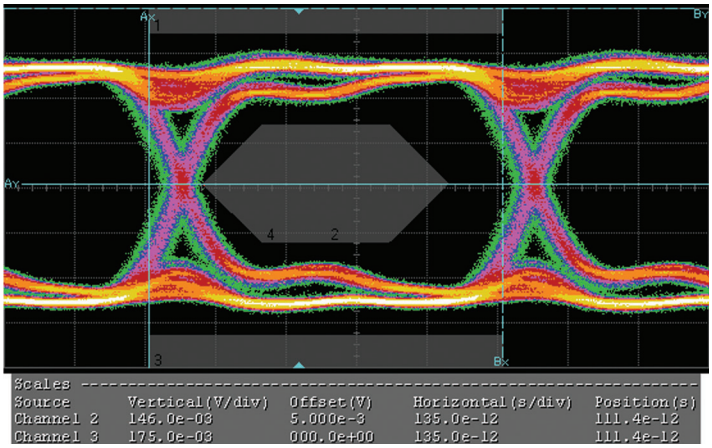


Figure 14: Original signal eye pattern – without common mode filter

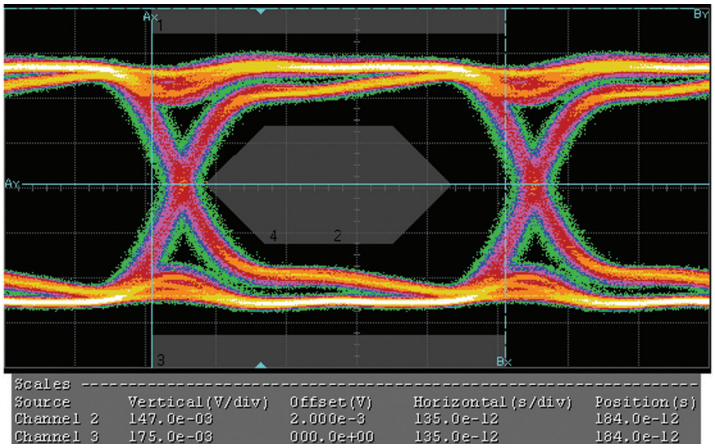


Figure 15: Eye pattern measured using the common mode filter

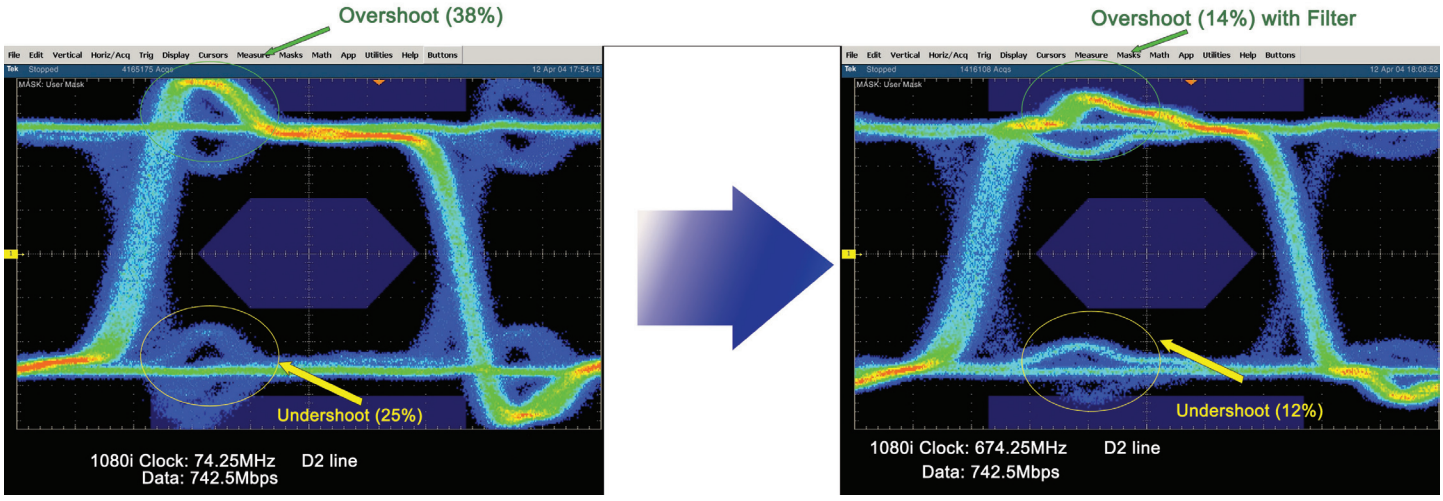


Fig 16. a) Signal with Overshoot Problem

b) Signal with improved Overshoot

By choosing the correct common mode filter as shown in Figure 11, the high frequency harmonics can be adequately suppressed.

During the testing of this solution, the effect of the noise suppression can be observed in the following EMI scan curves (with and without the use of the common mode filter). For simplicity, we only present the horizontal scan curves (see Figures 12 and 13).

At the same time, it is important to verify that the common mode rejection induced by the filter does not degrade the signal quality, causing a distorted eye pattern. In this particular case, the resulting eye pattern of the transmitted signal was measured and no distortion was detected (see Figures 16 and 17).

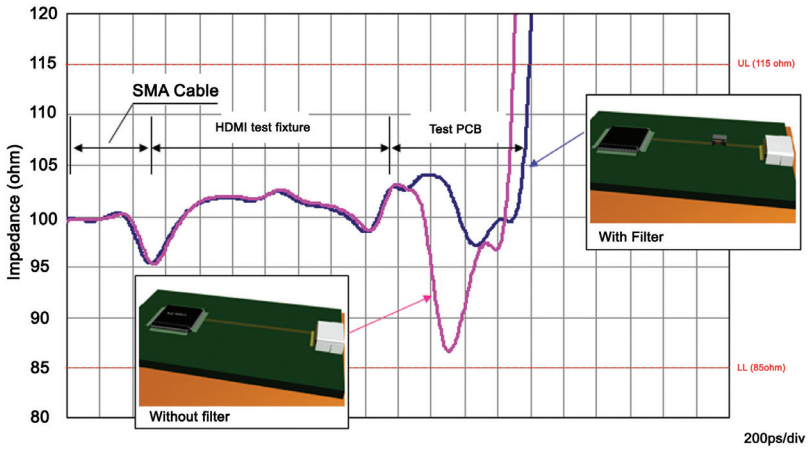


Figure 17: Reflectometry diagram showing the effect of the common mode filter

Signal Quality Improvement for Distorted Signals

Another issue often encountered is called "undershoot" and "overshoot" problems in the TMDS signal. Sources of this problem can be impedance mismatching, capacitances introduced by ESD devices, stray capacitances due to PCB layout, etc. The HDMI criteria for under and overshoot is:

Overshoot < 15% for 2*Vswing
Undershoot < 25% for 2*Vswing

Looking at Figures 16a and 16b, the target value for the overshoot is less than 15%, and the undershoot value less than 15%. The waveform in its current state measured an overshoot of 38% and undershoot of 25% at 1080i video resolution mode (74.25MHz clock) and data transmission of 742.5Mbps. The over and undershoot can be significantly reduced with the use of a common mode filter. This brings the overshoot down to 14%, and the undershoot down to 12%.

Impedance Compensation

Impedance mismatching in the path of the differential signals (through the IC, PCB traces, connectors, cables etc) might result in signal reflections, thus affecting the signal integrity. The HDMI compliance test specification describes the applicable measurement method through its TDR (time domain reflectometry) measurement. The specified criterion is to maintain the 100 Ohm +/- 15% through the signal travel path (these limits shown in the chart as UL and LL values). The addition of a common mode choke can offset the mismatching condition due to the added inductance (see Figure 17).

This particular test was performed by inducing an impedance mismatch in a test PCB, measuring the mismatch condition, and then using a common mode filter to improve the matching.

Skew Compensation

Skew in the differential signals is normally presented in the form of a delay in one of the differential signals (D+ and D-). Their switching point is not at the center line, as shown in Figures 18 and 19 below.

When measured, the skew in the signal can be observed as in Figure 19 below. Furthermore, if we attempt to do the mathematical average of both signals, the resulting common mode amplitude is not zero.

The use of a common mode filter in the differential pair will reduce the skew in these signals. This corrective measure is due to the generation of a negative voltage in the opposite line of where the skewed line is, bringing both signals into synch (see Figure 20).

The effect of skew in differential signals can be a source of serious electromagnetic emissions. The following tests demonstrate this effect (see Figures 21, 22

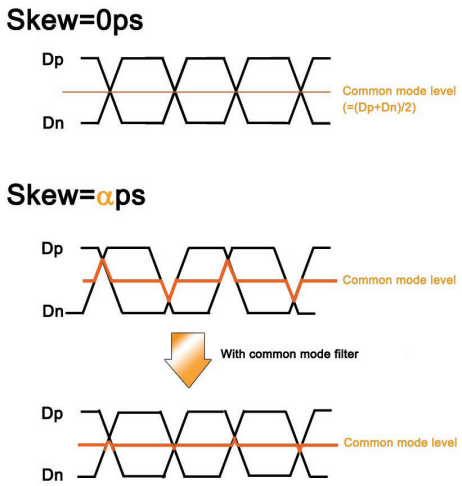


Figure 18: Simplified diagram of skew effect

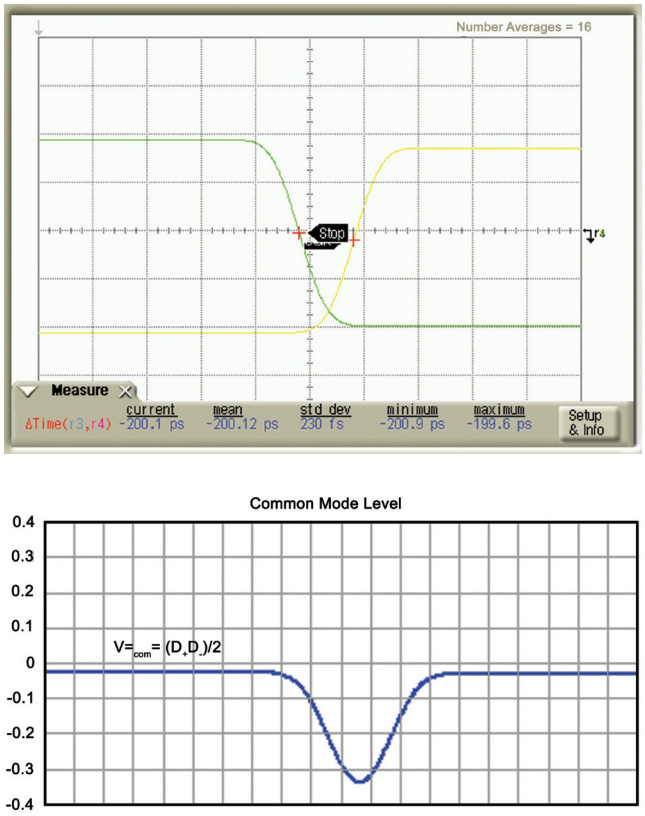


Figure 19: a) Skew measurement and b) Common mode voltage

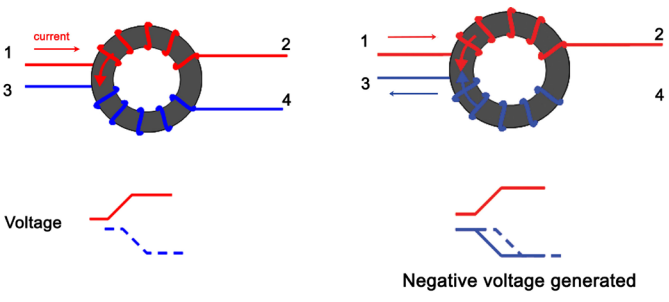


Figure 20: Skew correction mechanism through common mode filter

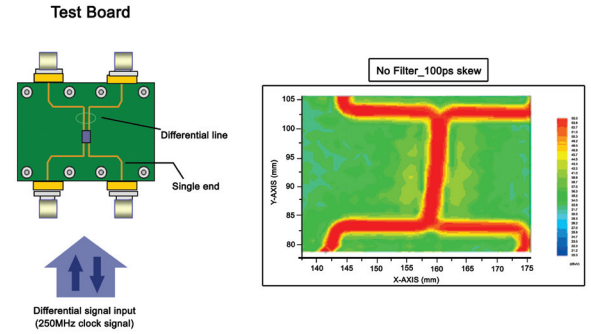


Figure 21: Original magnetic scan with skew and no filter

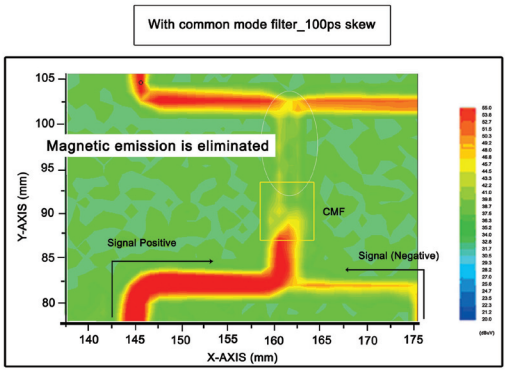


Figure 22: Magnetic scan with skewed input signal and using filter

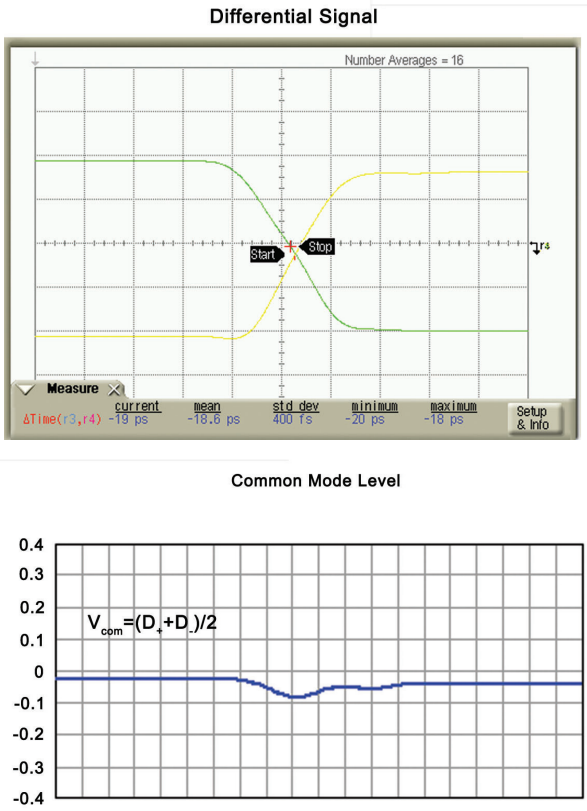


Figure 23: Effect of common mode filter in reducing the differential signals skew

and 23).

Differential Signal

Conclusions

The theoretical characteristics of the differential pair signals regarding differential and common mode noise often suggest that there will be no impact in EMI/EMC performance on the designs (that is, if there is a perfect balance in the differential signals). Good PCB design is a basic starting point to eliminate many of these problems. However, the real world implementation often experiences some level of skew, impedance mismatch, over and undershoot, etc., which is then translated into potential emissions and signal integrity problems. The intention of this article has been to illustrate alternative solutions through passive component (common mode filters) as way to minimize design cycles when the options to further improve PCB layouts become limited.

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