EPC GaN Transistor Application Readiness: Phase One Testing

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Efficient Power Conversion Corporation's (EPC) enhancement mode Gallium Nitride (GaN) power transistors offer performance well beyond the realm of silicon-based MOSFETs. Standard power converter topologies can greatly benefit from the added performance and realize improved efficiency while maintaining the simplicity of older designs.

Although similar to standard power MOSFETs, enhancement mode GaN transistors are a relatively new technology. Operating life information is not yet at the level available to users of silicon power MOSFETs. EPC's risk-reduction results to date include the placement of over 380 devices, at their maximum operating ratings on a wide variety of stress tests. Over 275,000 total device hours support our product's readiness for commercial use. The conversion of power MOSFET-based systems can begin with acceptable levels of risk.

In this paper, the suitability for reliable and commercial use of EPC technology will be addressed in detail.

GaN OVERVIEW

The fundamental properties of GaN make it an ideal starting material for high power transistors. Some of these properties are derived from the crystal's wide band-gap of 3.4 eV. This wide band-gap creates an extremely high electric breakdown field (about 10 times of silicon), making GaN an outstanding material for high voltage transistors and for operation at elevated temperatures. The electron density resulting from the polarization-induced field in the GaN structure is very high (~10^{13}/cm^2). The high two-dimensional electron gas (2DEG) density and high electron mobility make GaN **h**igh **e**lectron **m**obility **t**ransistors (HEMTs)[1] very attractive for low on-state resistance power transistors with high breakdown voltage and high current density capability.

GaN Devices Have Been the Subject of Intense Research for the Past Decade

Research and development projects sponsored by the Defense Advanced Research Agency (DARPA) including teams from Triquint, Raytheon and Northrop Grumman have resulted in estimated transistor lifetime using single failure mode Arrhenius elevated temperature testing of >100,000 hours at a junction temperature of 150°C. This represents a five order of magnitude increase in transistor lifetime, taking GaN from a laboratory novelty to being able to compete with mature technologies [2,4].

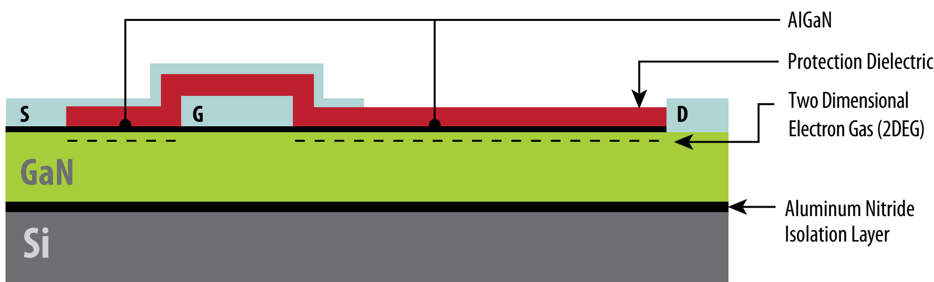

Figure 1: GaN on silicon devices have a very simple structure similar to a lateral DMOS device and are built in a standard CMOS foundry.

Commercial GaN HEMTs are already available for the RF and microwave markets from companies such as Nitronex[3], RFMD[4], and Eudyna[5].

Although the focus of research and development has been depletion-mode or d-mode (normally-on) HEMTs, enhancement-mode or e-mode (normally-off) HEMT's are strongly preferred. Enhancement-mode (normally-off) HEMTs offer safer operation, greater simplicity of circuit design, and lower energy consumption. There are numerous examples in the literature regarding enhancement-mode GaN HEMTs (HEMT can be used interchangeably with HFET, **h**eterostructure **f**ield **e**ffect **t**ransistors) including but not limited to:

- Recessed etching of the AlGaN barrier in cojunction with a Schottky gate electrode[30]
- Fluoride-based plasma treatment of the gate[31]
- E-mode HFET using p-n junction gate contact[6]
- E-mode HFET utilizing conductivity modulation[9, 10]

EPC PRODUCT INTRODUCTION

Efficient Power Conversion enhance-mode HFETs were commercialized in June of 2009. Figure 1 shows a schematic structure of an EPC device which is similar to a lateral DMOS silicon device and fabricated on silicon substrates, employing standard silicon processes. The cost of EPC products is therefore comparable to silicon technologies [11].

During 2009, EPC introduced ten part numbers covering 40, 60, 100, 150 and 200 volt enhancement-mode GaN power transistors. The voltage ratings, maximum $R_{DS(ON)}$, and product dimensions are listed in Appendix I. EPC's GaN transistors are lateral devices with all three terminals: gate, drain, and source on the front side of the chip. The active device is isolated from the substrate and fully encapsulated by

passivation layers on the front side as shown in Figure 2. This configuration allows EPC's GaN transistors to be used as bare die without additional packaging[28]. The advantages include: the elimination of plastic packages and the related performance issues, improved reliability, and cost reduction. EPC GaN transistors employ wafer-level solder line-grid-arrays as shown in Figure 3.

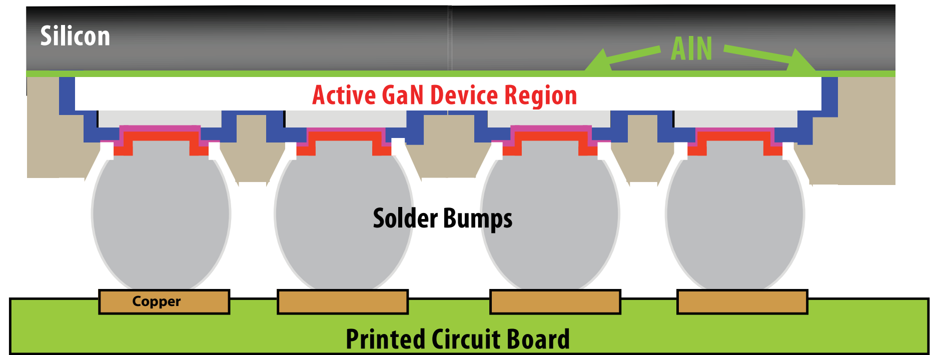

Figure 2: GaN on silicon can be used as a "flip chip". The active device is isolated from the silicon substrate and can be completely encapsulated prior to singulation. When compared to plastic packages, this design reduces cost and requires less space.

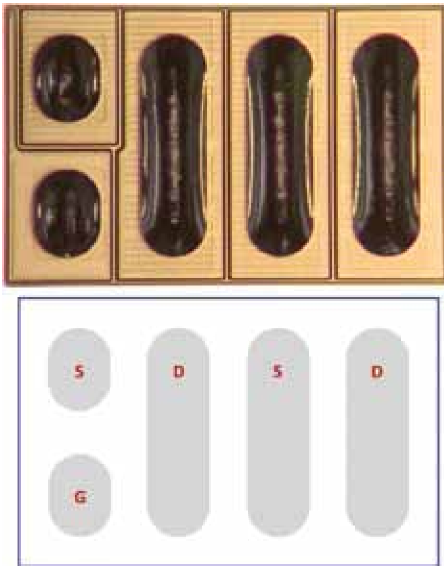

Figure 3: Front side view of EPC 1014, 40v, 16mΩ GaN transistor showing the solder line-grid-array bump design with alternating source and drain solder bars.

RELIABILITY PROGRAM OVERVIEW

The conversion of Power MOSFET-based systems to enhancement-mode GaN technology requires evidence of reliable performance. In Phase One, EPC stressed more than 380 devices for a total of more than 275,000 hours under conditions similar to power MOSFET reliability stress testing.

"Dynamic $R_{DS(ON)}$", specifically those conditions causing minimal shifting in device resistance, is extensively discussed in the literature and was a particular focus of the EPC Phase One reliability program[12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27]. EPC's devices have been designed to mitigate dynamic $R_{DS(ON)}$ and data show significantly greater stability than devices reported in the literature.

Dynamic $R_{DS(ON)}$

Dynamic $R_{DS(ON)}$ is a phenomenon whereby a device's on-resistance increases after being subjected to a drain bias. The magnitude of the increase depends on the drain-side gate edge electric field, under which electrons are accelerated and a small number remained trapped in the EPI layer, or at the EPI surface. As the trapped electrons deplete the 2DEG, $R_{DS(ON)}$ is increased. The higher the drain pre-bias voltage, the higher the $R_{DS(ON)}$ becomes post-bias. Over time, the trapped electrons de-trap (relax) and $R_{DS(ON)}$ gradually returns to the pre-bias value.

Several companies and institutions have reported suppression of dynamic $R_{DS(ON)}$ by surface passivation[20, 21]. Proper field-plating can also reduce the peak electric field, thereby suppressing dynamic $R_{DS(ON)}$[17]. It was reported that dynamic $R_{DS(ON)}$ was much improved with GaN devices built on conductive silicon substrates compared to GaN devices built on non-conductive sapphire substrates[29]. This improvement is due to the conductive substrate acting as a field plate on the back side. With GaN on a conductive substrate, dynamic $R_{DS(ON)}$ was reported being influenced by the GaN EPI layer thickness.

EPC products use an optimized EPI structure and EPI thickness on conductive silicon substrates to minimize dynamic $R_{DS(ON)}$. The EPI surface is passivated with a high quality Si_3N_4 layer.

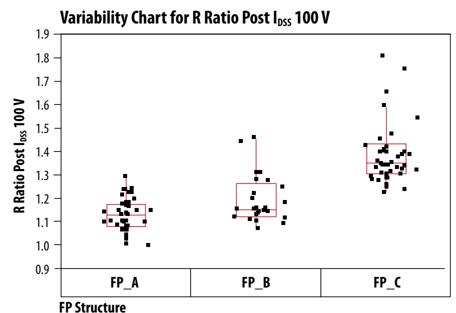

Figure 4: Field plate has big impact on dynamic $R_{DS(ON)}$. An example is shown comparing field-plate structure A, B, and C that were studied during product development.

Field plate structures are also optimized. Figure 4 shows an example comparing field-plate structure A, B, and C that were studied during EPC product development. Field-plate structure A is superior in terms of dynamic $R_{DS(ON)}$.

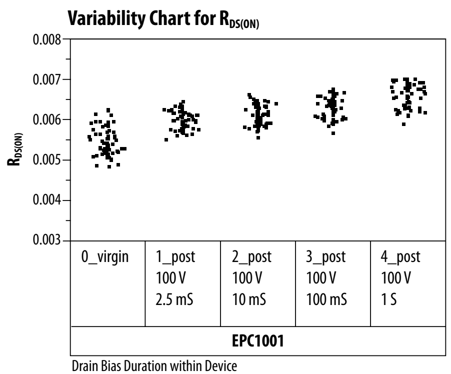

Figure 5: $R_{DS(ON)}$ values after 100V bias for various durations.

Dynamic $R_{DS(ON)}$ was evaluated on a TESEC tester. $R_{DS(ON)}$ was measured pre and post stress whilst the drain-source voltage was stepped from low voltage to 30% above the rated maximum drain-source voltage. The effect of drain bias duration was also evaluated. Figure 5 shows $R_{DS(ON)}$ values after 100V bias for various durations. Increasing drain bias duration from 2.5 mS to 1 Sec results in minimal increase in $R_{DS(ON)}$.

The $R_{DS(ON)}$ values post various drain biases for duration of 2.5 mS are shown in Figures 6, Figure 7, and Figure 8 for 40V, 100V, and 200V product, respectively. Two device types are shown in each figure for each of the voltage ratings. The 40V devices, EPC1014 and EPC1015, were biased to 40V, 48V and 52V sequentially. The 100V devices, EPC1001 and EPC1007, were biased to 60V, 100V, and 130V sequentially. The 200V devices, EPC1010 and EPC1012, were biased to 100V, 200V, and 260V

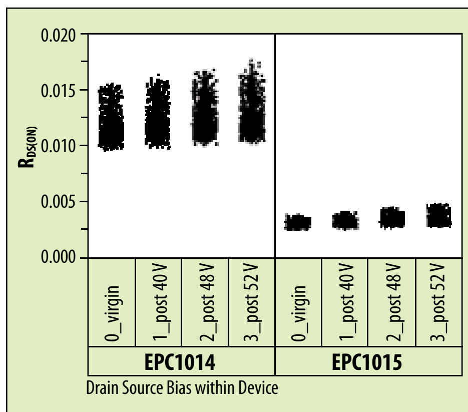

Figure 6: The $R_{DS(ON)}$ values post various drain biases are shown for EPC1014 and EPC1015, the two 40V products.

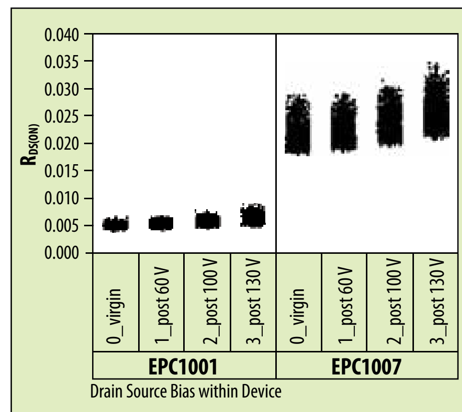

Figure 7: The $R_{DS(ON)}$ values post various drain biases are shown for EPC1001 and EPC1007, the two 100V products.

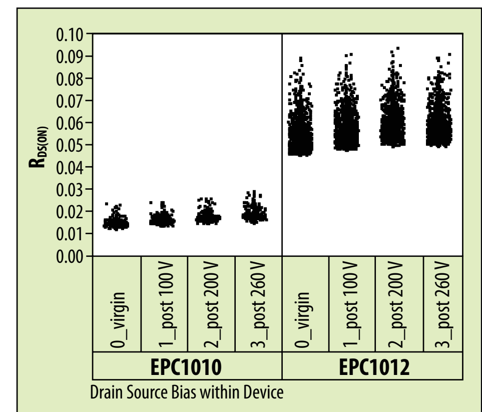

Figure 8: The $R_{DS(ON)}$ values post various drain biases are shown for EPC1010 and EPC1012, the two 200V products.

sequentially. The degree of dynamic $R_{DS(ON)}$ was similar for all product types. The increase in $R_{DS(ON)}$ for the main population was approximately 10% with a tail at higher or lower values.

RELIABILITY TESTING OVERVIEW AND RESULTS

Long term stability under high drain-source bias was evaluated by subjecting devices to DC voltage equal to the maximum drain-source rated voltage and temperature (**h**igh **t**emperature **r**everse **b**ias, or HTRB). Gate reliability was evaluated by subjecting devices to various gate stresses at elevated temperature (**h**igh **t**emperature **g**ate **b**ias, or HTGB). Environmental reliability was evaluated with **t**emperature **c**ycling (TC) and **t**emperature-**h**umidity-with-**b**ias (THB). Devices were also subjected to operating life tests involving devices in actual power supplies running at high voltage and high current.

A list of the reliability tests performed, the applicable standards, the device types evaluated, and the stress conditions are listed in Appendix II. All devices tested were soldered onto Arlon 85N printed circuit boards.

HighTemperature Reverse Bias Test (HTRB)

The impact of high drain bias on device parameters, applied for long periods of time, was evaluated with maximum rated drain-source bias applied at an ambient temperature of 125ºC. Whereas there were no parametric failures out of the parts tested, there was some degree of dynamic R_{DSON} post stress test (A 20% increase in R_{DSON} was observed for some devices).

All electric parameters remained relatively constant throughout the entire stress period of 1000 hours for EPC1001 and EPC1014. Appendix IV graphically presents the stability of various device parameters during test.

High Temperature Gate Bias Test (HTGB)

The gate stability of EPC GaN transistors was evaluated under various gate bias conditions at 5V, 5.4V, and 6V at 125ºC. EPC1001 parts were used for each of the three tests. At 5Vgs and 5.4Vgs bias, all device electric parameters stayed relatively constant over the entire burn-in period of 1000 hours. It was observed though that the drain leakage increased with 6Vgs bias. Five parts showed higher than the datasheet limit at the 168 hours pulling point (Appendix III *). These parts were put back on burn-in, and will be analyzed after the stress test is finished. Complete test results are presented in Appendix V.

Temp Cycle (TC)

Temperature cycling was conducted on EPC1001, a large device, and on EPC1014, a small device. These two part numbers have different bump designs and were used to check the bump joint reliability. Parts were all mounted on Arlon 85N printed circuit board material. Temperatures varied between -40C to 125ºC at a rate of two cycles per hour. No on-state resistance degradation was observed over the stress period of 1000 cycles. All electrical parameters remained constant during stress. Complete test results are shown in Appendix VI.

Temperature Humidity Bias Test (THB)

Device performance was also characterized with temperature and humidity with drain-source bias (THB). THB tests were conducted at 85ºC and with 85% relative humidity. EPC1014 was on test with drain biased to the rated 40 volt. At time of this writing, parts have completed 500 hours stress, and are continuing on test for 1000 hours. All device electric parameters remained relatively constant over the stress period. Complete test results are shown in Appendix VII.

Power Supply Operating Life Test

To demonstrate the performance of the GaN transistors in-circuit, and to test the reliability under high-stress operating life, EPC built 48V-1V power supply boards using a "buck converter" topology (see figure 9). For the burn-in test, EPC1001 (100V, 7 mΩ) transistors were used for both the control transistor and rectifier switches. This kind of test is particularly useful because, in a standard "buck" topology DC-DC converter operated at the high Vin/Vout ratio of 48V:1V, the control transistor is turned ON at a very low duty cycle (~2%). Conversely, the rectifier transistor is turned ON with a very high duty cycle (~98%). This test therefore stresses devices both at high drain-source voltage and high drain current under actual, fast-switching conditions. The converter was operated at 48V input voltage, 1V output voltage, 10A output current, and at a switching frequency of 250 kHz. The circuit efficiency was measured at time-zero hour, 24, 48, 72, 168, 500, 1000, and 1200 hours. The normalized efficiency vs. burn-in hours is plotted in Figure 9(a), and the power supply test circuit is shown in Figure 9(b). The efficiency of all the power supply boards stayed virtually unchanged over the entire burn-in period.

FUTURE WORK

EPC has plans for a much broader and deeper study of the reliability of enhancement mode GaN power transistors. In Phase 2, EPC will complete the 1000 hour/1000 cycle testing on all product types. Further work will also be done to develop acceleration factors and models that allow users to determine suitability for various applications beyond basic commercial use.

Dynamic $R_{DS(ON)}$ will continue to be investigated with the goal of further minimizing this characteristic of EPC GaN devices.

EPC will convert to lead free solder in the second half of 2010. This conversion will be accompanied by additional testing at 150°C to verify this change does not degrade device characteristics under stress. At that time, EPC will also conduct temperature cycling tests on a wide variety of substrate materials to validate compatibility.

SUMMARY

EPC's enhancement mode Gallium Nitride transistors bring tremendous performance and size advantages over silicon power MOSFETs. These advantages can be used to improve system efficiency, reduce system cost, reduce size, or a combination of all three. Because EPC's products were designed as power MOSFET replacements, designers can use their existing building blocks, skills and knowledge with only minor changes. Reliability testing has also demonstrated that the technology is now ready for general commercial use.

The future of GaN transistors is now.

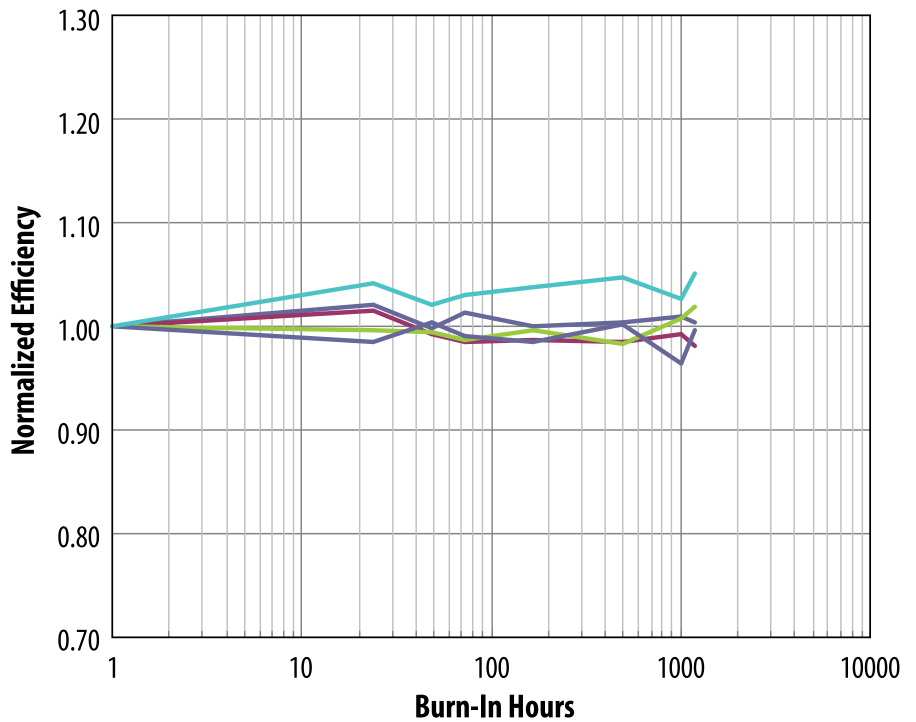

Figure 9(a): Power supply life test using EPC1001 at 30oC and 10A. The normalized converter efficiency was plotted over 1200 hours of operating life.

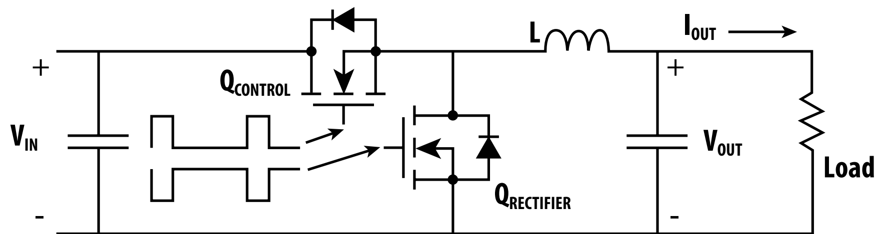

Figure 9(b): Power supply test circuit

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Appendix

APPENDIX I: . . . . .Product Matrix Table
APPENDIX II: . . . . Reliability Test Table
APPENDIX III: . . . . Reliability Results Table
APPENDIX IV: . . . . .HTRB Results
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APPENDIX VI: . . . . .TC Results
APPENDIX VII: . . . . THB Results
APPENDIX VIII: . . . . Power Supply Operating Life Results

Appendix I: Product Matrix Table

Part Number	Voltage Rating	$R_{DS(ON)}$ Max	Package Dimensions
	(V)	(mOhm)	(mm x mm)
EPC1014	40	16	LGA 1.7 X 1.1
EPC1015	40	4	LGA 4.1 X 1.6
EPC1009	60	30	LGA 1.7 X 1.1
EPC1005	60	7	LGA 4.1 X 1.6
EPC1007	100	30	LGA 1.7 X 1.1
EPC1001	100	7	LGA 4.1 X 1.6
EPC1013	150	100	LGA 1.7 X 0.9
EPC1011	150	25	LGA 3.6 X 1.6
EPC1012	200	100	LGA 1.7 X 0.9
EPC1010	200	25	LGA 3.6 X 1.6

Appendix II: Reliability Test Table

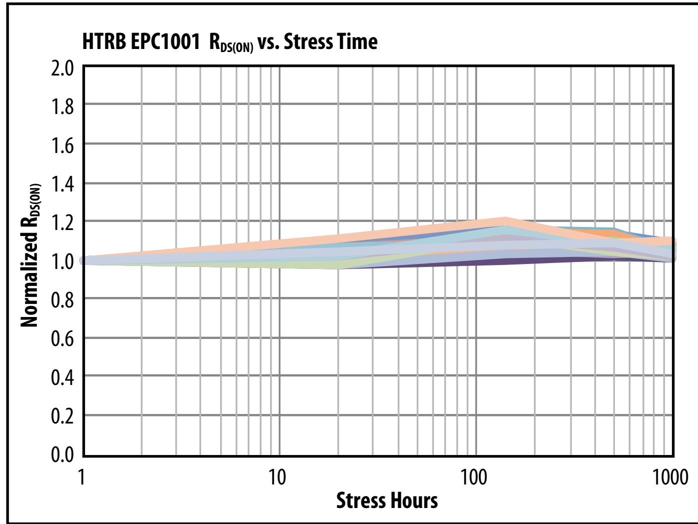
Reliability Stress Test	Applicable Standard	Product	Stress Conditions
High **T**emperature **R**everse **B**ias (HTRB)	JEDEC Std JESD22-A108	EPC1001, EPC1014	100% rated drain bias, 125˚C
High **T**emperature **G**ate **B**ias (HTGB)	JEDEC Std JESD22-A108	EPC1001	5 V, 5.4 V, 6 V gate bias, 125˚C
Temperature **C**ycling (TC)	JEDEC Std JESD22-A104	EPC1001, EPC1014	-40˚C to 125˚C, 2 cycles per hour
Temperature **H**umidity **B**ias (THB)	JEDEC Std JESD22-A101	EPC1014	85˚C/85RH, rated drain bias or max 100 V drain bias
Power Supply Operating Life		EPC1001	10A, 250 kHz, 30˚C

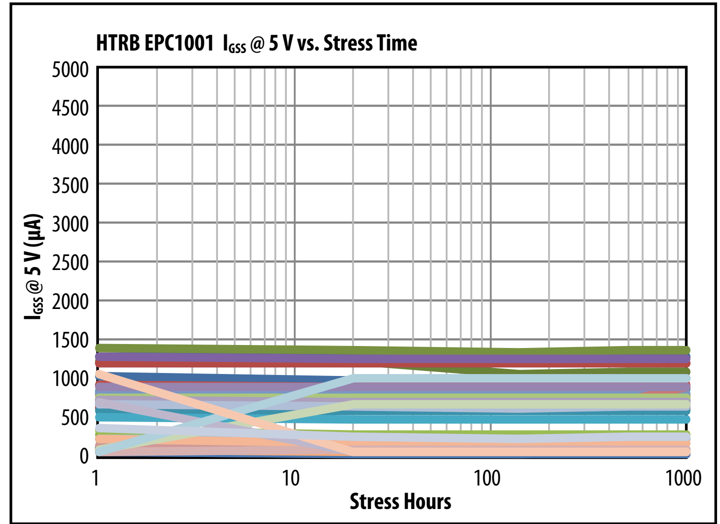
Appendix III: Reliability Results Table

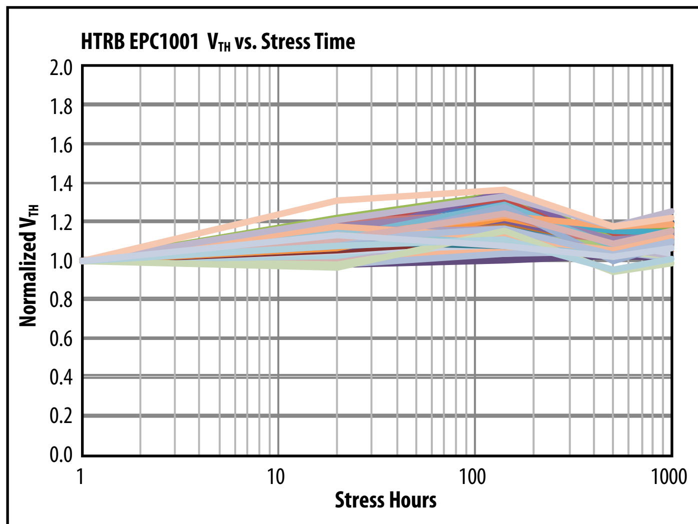
Stress Test	Part Number	Sample Size	# of Fail at Read Point			
			24HR	168HR	500HR	1000HR
HTRB	EPC1001	45	0	0	0	0
HTRB	EPC1014	50	0	0	0	0
Stress Test	**Part Number**	**Sample Size**	**# of Fail at Read Point**			
			24HR	168HR	500HR	1000HR
HTGB 5 V	EPC1001	45	0	0	0	0
HTGB 5.4 V	EPC1001	45	0	0	0	0
HTGB 6 V	EPC1001	50	0	5*		
Stress Test	**Part Number**	**Sample Size**	**# of Fail at Read Point**			
			48 cys	168 cys	500 cys	1000 cys
TC	EPC1001	45	0	0	0	0
TC	EPC1014	50	0	0	0	0
Stress Test	**Part Number**	**Sample Size**	**# of Fail at Read Point**			
			24HR	168HR	500HR	1000HR
THB	EPC1014	45	0	0	0	
Stress Test	**Part Number**	**Sample Size**	**# of Fail at Read Point**			
			24HR	168HR	500HR	1000HR
Power Supply Life Test	EPC1001	10	0	0	0	0

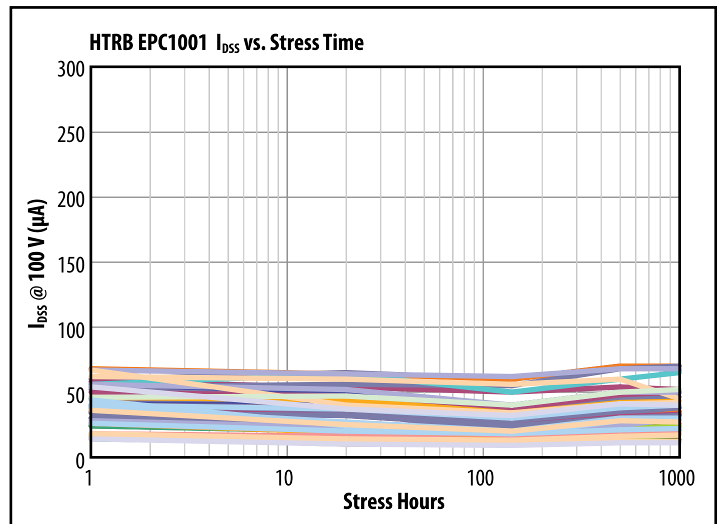
Appendix IV: HTRB Maximum Rated Voltage at 125˚C

EPC1001 HTRB 100 V at 125˚C



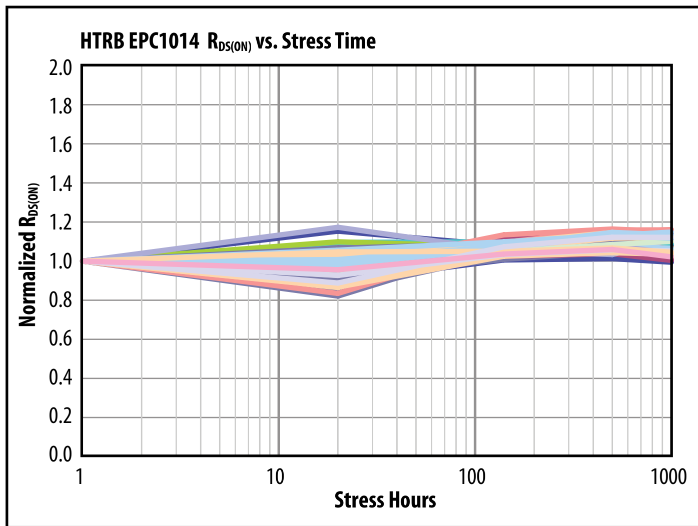


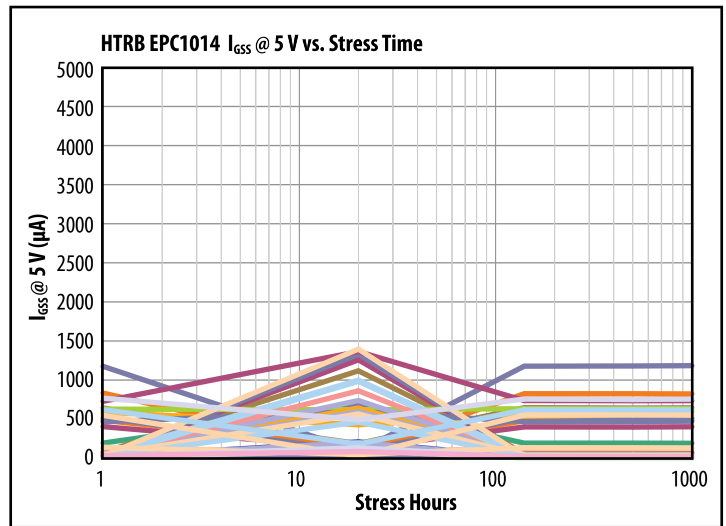


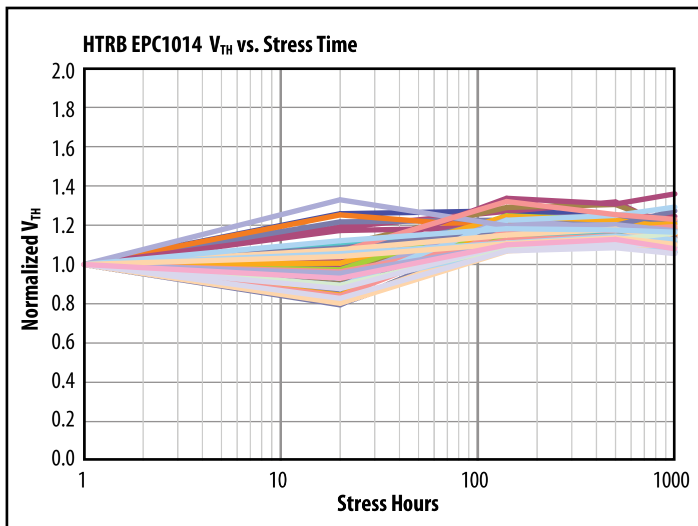


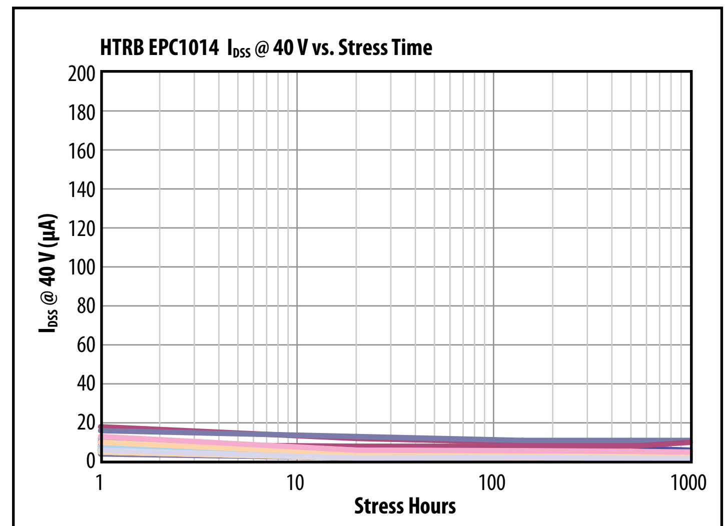
Appendix IV: HTRB Maximum Rated Voltage at 125˚C

EPC1014 HTRB 40 V at 125˚C



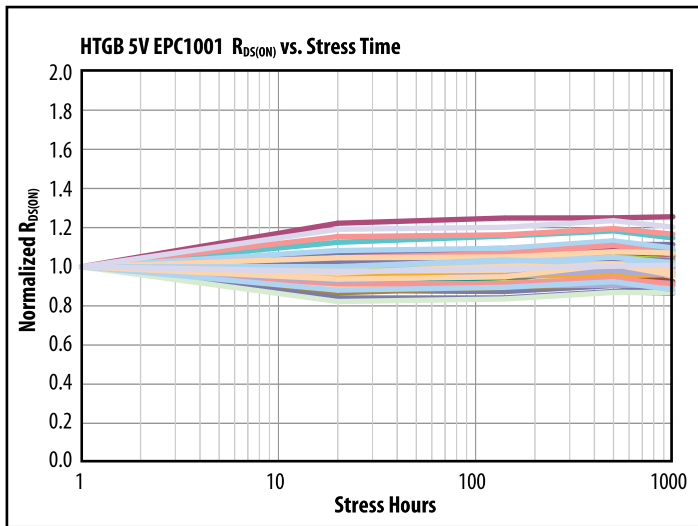


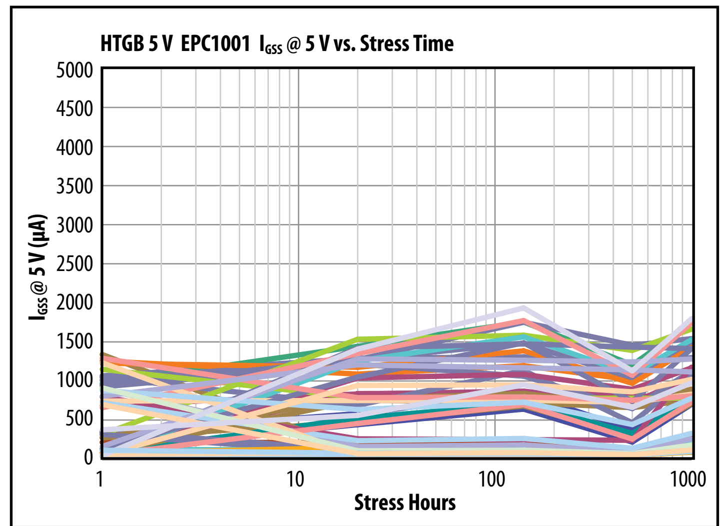


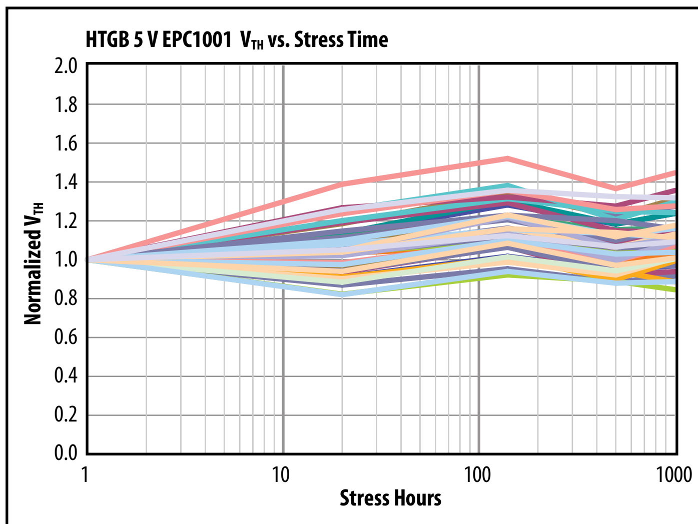


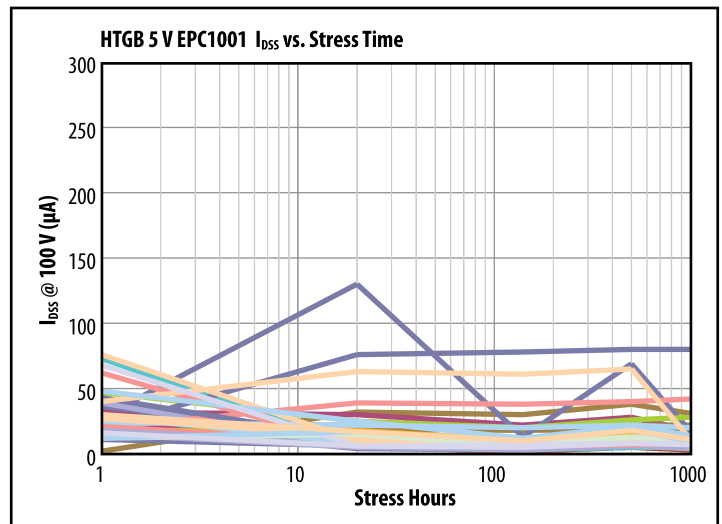
Appendix V: HTGB @ 125˚C

EPC1001 HTGB 5 V at 125˚C



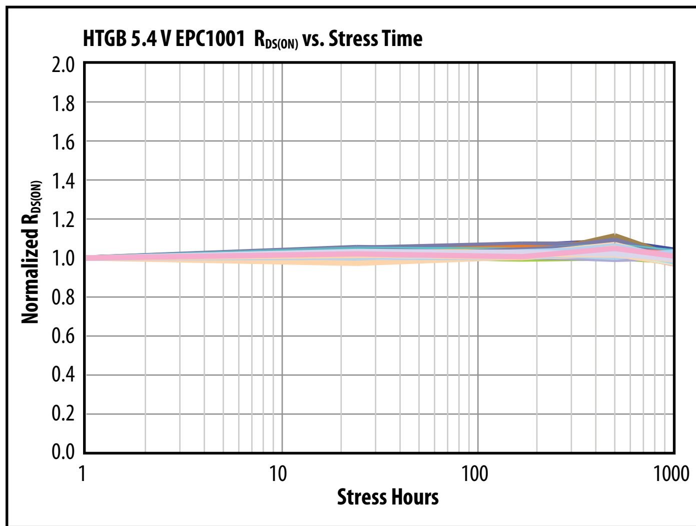


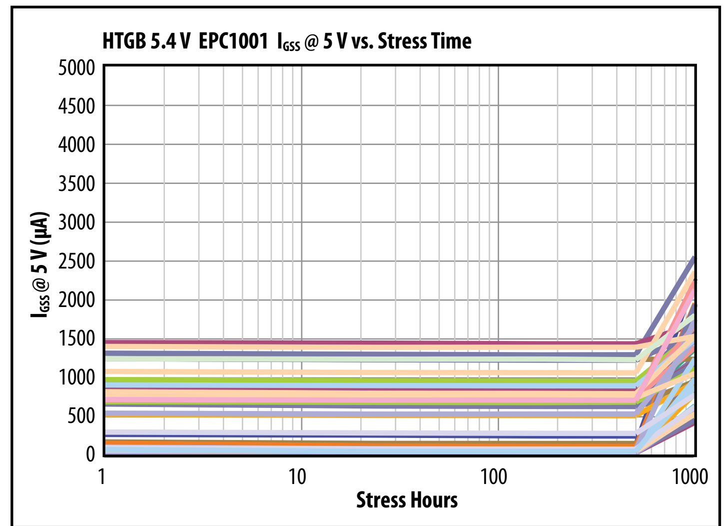


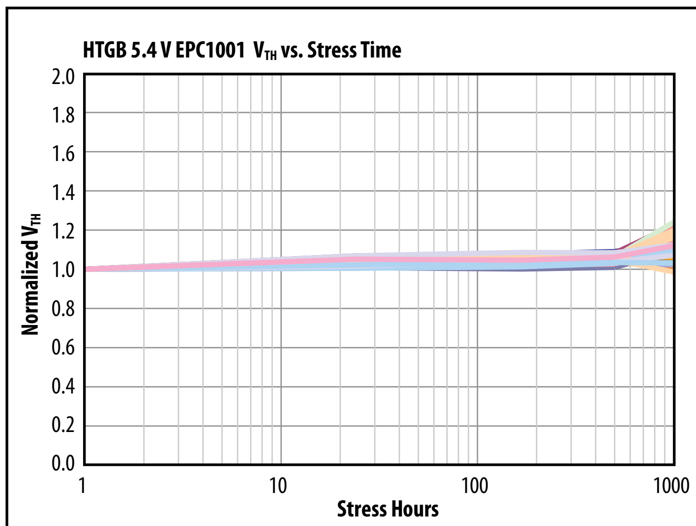


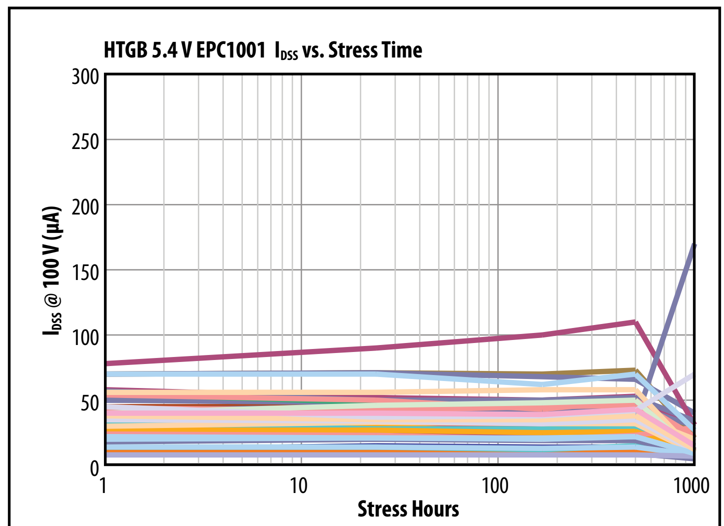
Appendix V: HTGB @ 125˚C

EPC1001 HTGB 5.4 V at 125˚C



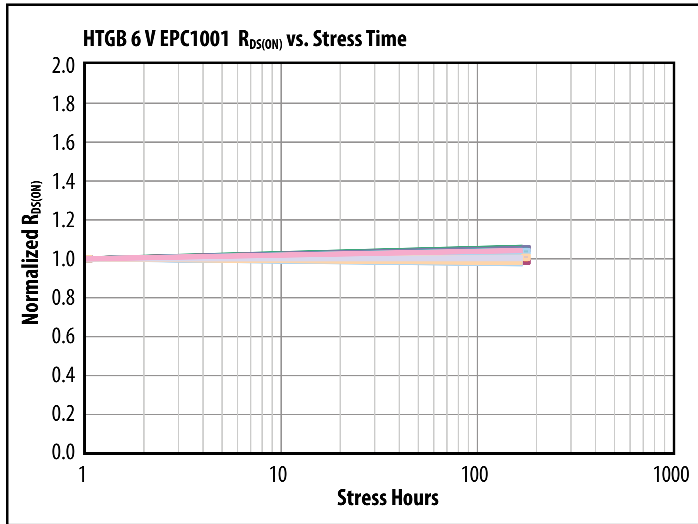


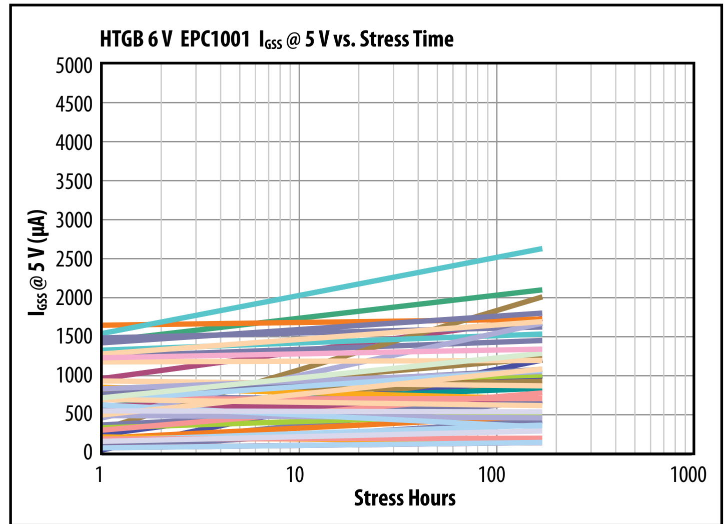


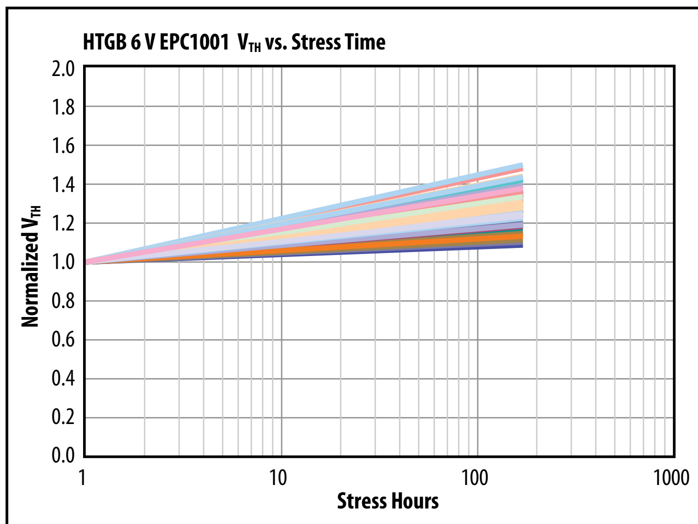


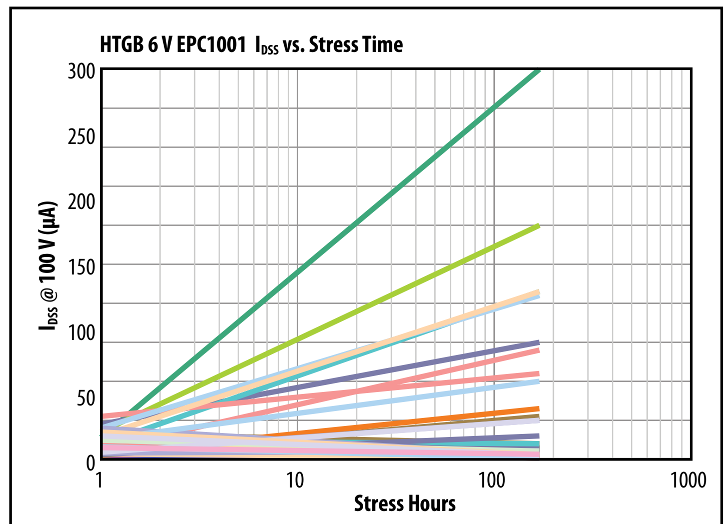
Appendix V: HTGB @ 125˚C

EPC1001 HTGB 6 V at 125˚C



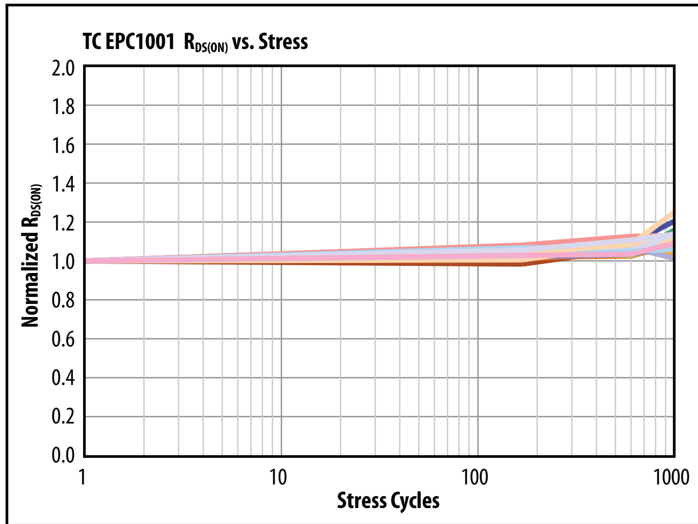


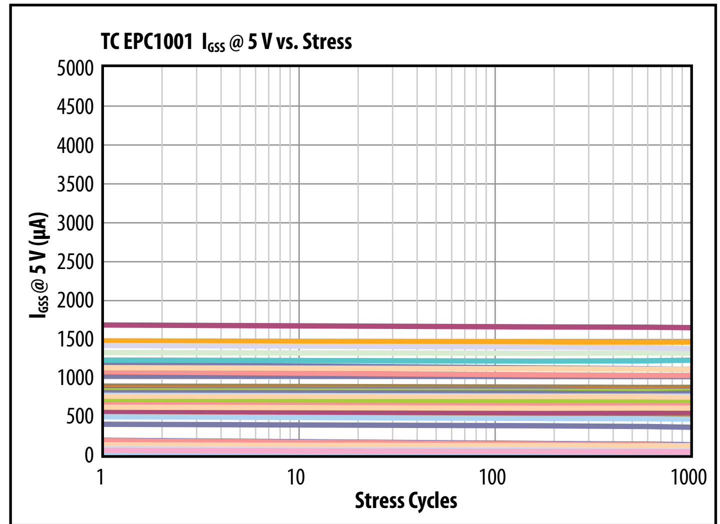


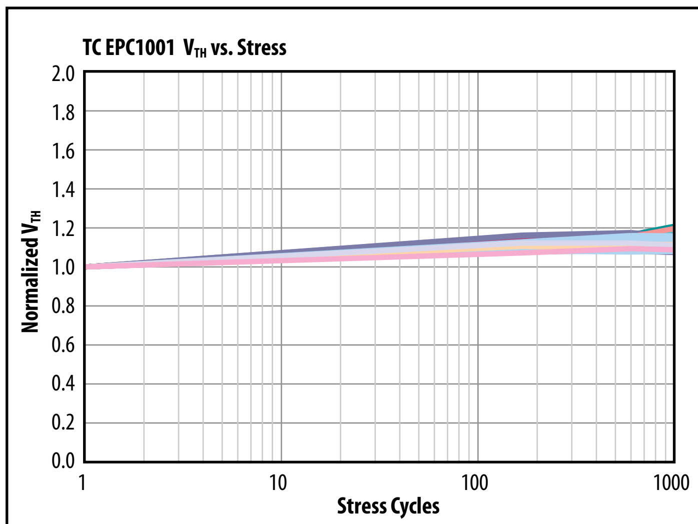


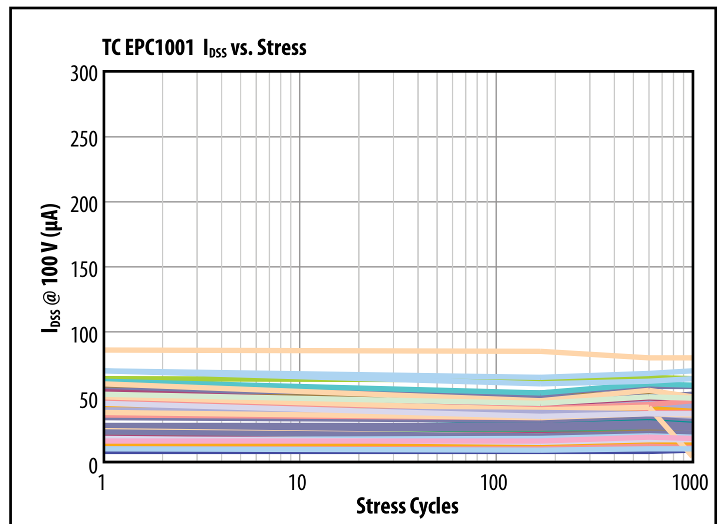
Appendix VI: Temperature Cycling -40˚C to 125˚C

EPC1001 TC -40˚C to 125˚C



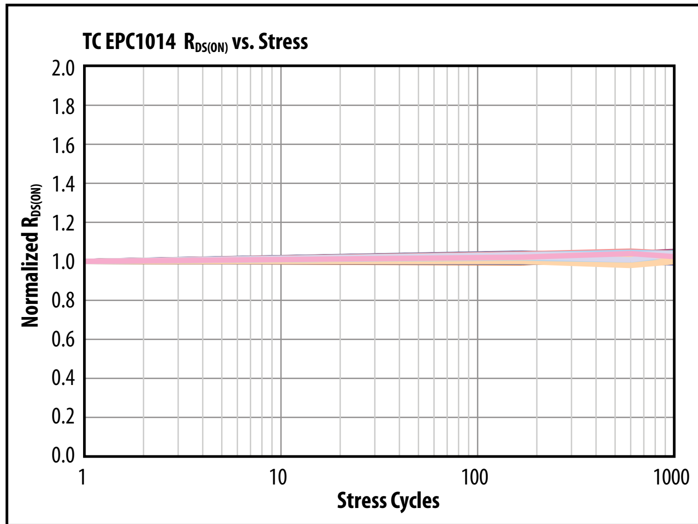


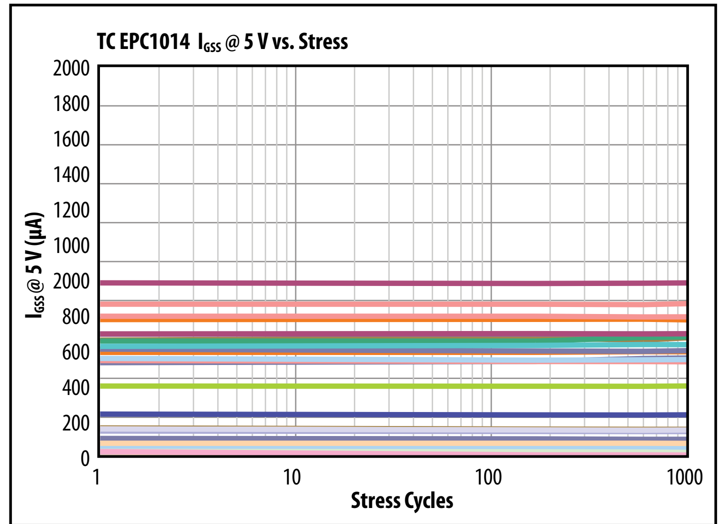


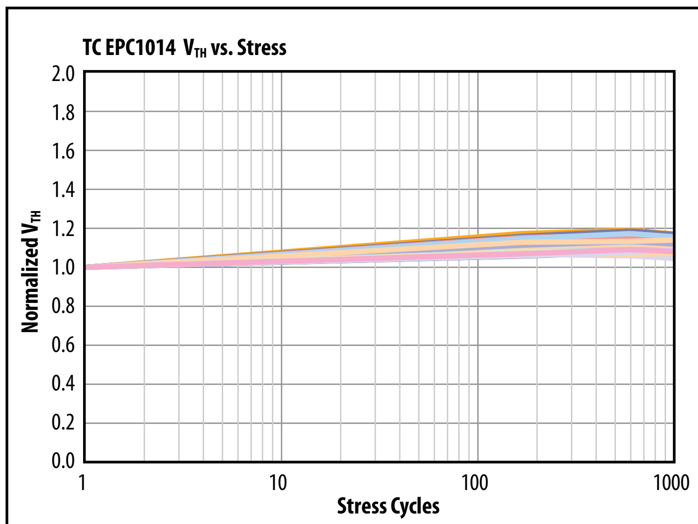


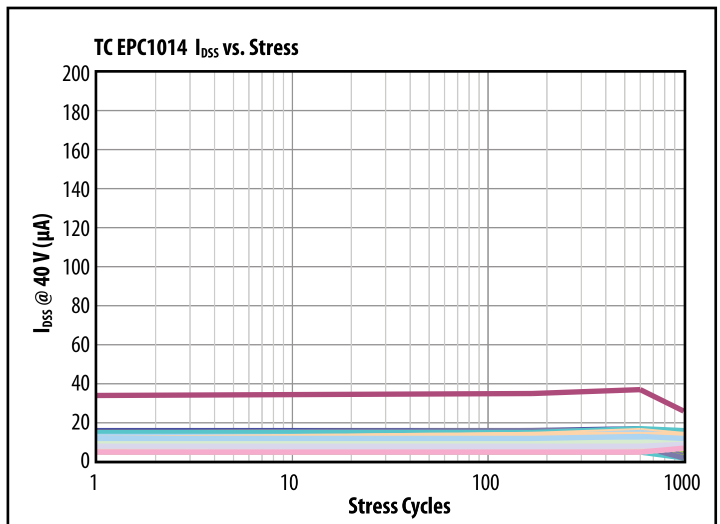
Appendix VI: Temperature Cycling -40˚C to 125˚C

EPC1014 TC -40˚C to 125˚C



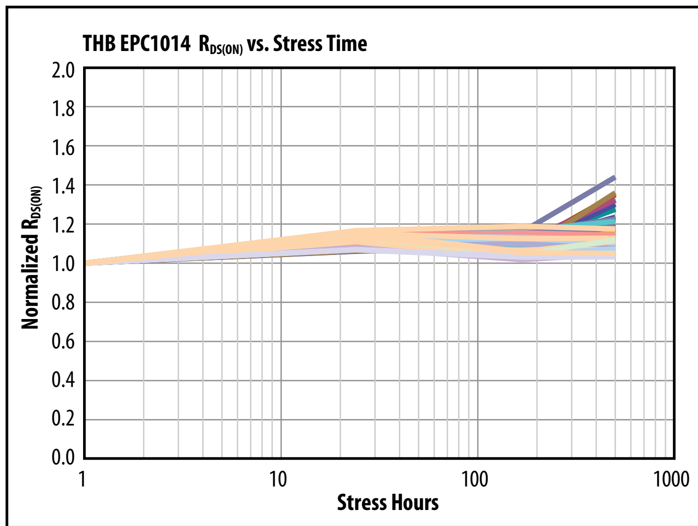


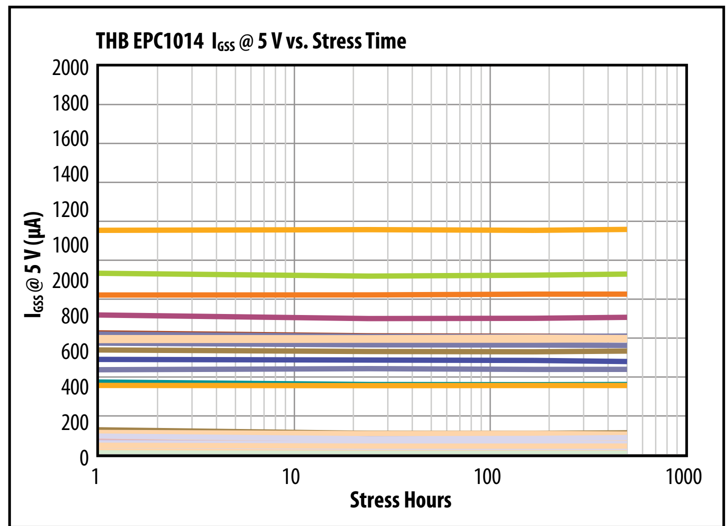


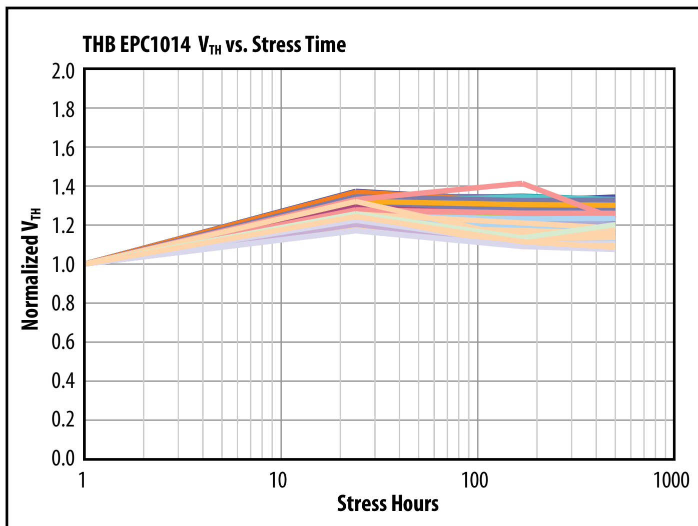


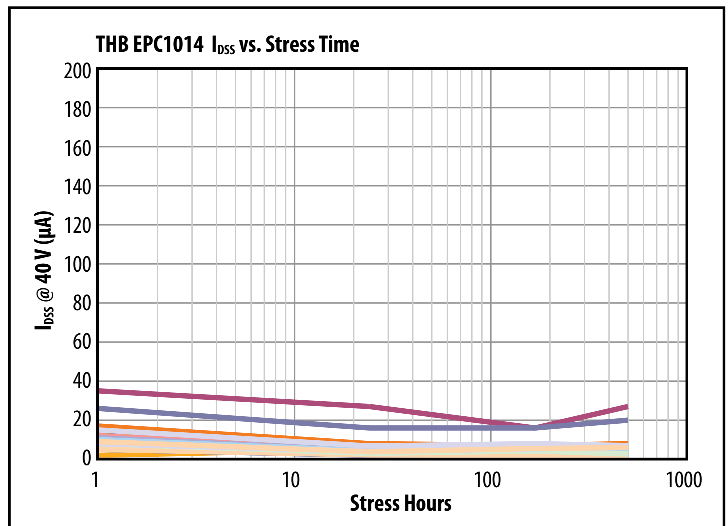
Appendix VII: THB 85˚C, 85% RH

EPC1014 THB 85˚C / 85 RH 40 V





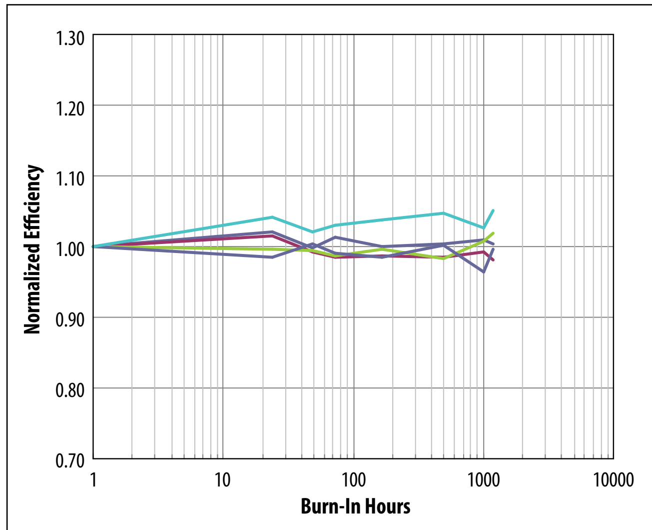


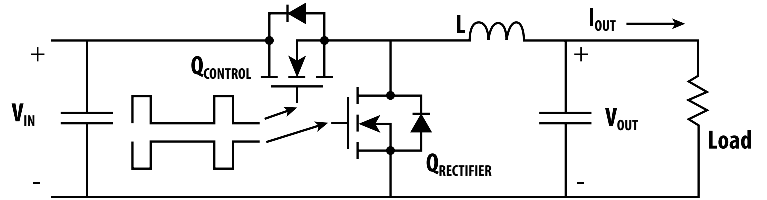


Appendix VIII: Operating Life Tests

EPC1001 Power Supply Operating Life

48 V_{IN} – 1 V_{OUT}, 10 A Load, 250 kHz





Power supply test circuit

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