

EPC eGaN® FETs Transistor Application Readiness: Phase Four Testing



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Efficient Power Conversion Corporation's enhancement mode Gallium Nitride (eGaN®) FETs, although similar to standard power MOSFETs, deliver performance unattainable by silicon-based devices [1]. EPC FETs offer common power converter topologies added performance and improved efficiency while maintaining the simplicity of older designs [2,3,4]. Joining the eGaN FETs product family introduced in 2010, EPC launched a second generation product family in March, 2011 [5]. These new products are lead-free, halogen free, and are RoHS compliant. EPC's risk-reduction results to date include the placement of over 1400 devices, at their maximum operating ratings in a wide variety of stress tests. Over 1,400,000 accumulated device hours of reliability testing validate the readiness of eGaN FETs to supplant their aging silicon cousins for most commercial power switching applications.

Parts were mounted onto FR408 or FR5 adaptor cards unless otherwise stated. Adaptor cards with two copper layers or four copper layers were used. Two ounce copper was used for the two layer cards; one ounce outer layers and two ounce inner layers were used for the four layer cards. The solder paste materials used when mounting the parts were AIM lead-free no-clean NC257-2 SAC305 [6]

RELIABILITY TEST RESULTS OVERVIEW

EPC's eGaN FETs were subjected to a wide variety of stress tests under conditions that are typical for power MOSFETs. These tests included:

- High temperature reverse bias (HTRB): Parts are subjected to a drain-source voltage equal to or near the maximum rated voltage at the maximum rated temperature
- High temperature gate bias (HTGB): Parts are subjected to gate-source voltages at the maximum rated temperature
- Operating Life: Parts are assembled onto power supply boards and the boards are subjected to actual switching power conversion operating conditions
- High temperature high humidity (H3TRB): Parts are subjected to humidity under high temperature with a drain-source voltage applied
- Temperature cycling (TC): Parts are subjected to alternating high- and low temperature extremes
- Unbiased autoclave (AC or Pressure Cooker Test): Parts are subjected to pressure, humidity, and temperature under condensing conditions
- Moisture sensitivity level test: Parts are subjected to moisture, temperature, and three cycles of reflow

The stability is verified with DC electrical tests after stress biasing. The electrical parameters are measured at time-zero and at interim readout points at room temperature. Electrical parameters such as the gate-source leakage, drain-source leakage, gate threshold voltage, and on-state resistance are compared against the data sheet specifications. A failure is defined as a part that exceeds the datasheet specifications. The eGaN FETs are typically taken to 1000 hours or 1000 cycles in stress duration. Some tests are taken up to multiple thousands of hours to check the performance over longer periods of time.

The JEDEC Standards, where applicable, are followed in the reliability testing.

and Senju Metal Industrial Co. (SMIC) lead-free M705-GRN360-K-V series [7]. A typical reflow profile using the Senju M705-GRN360 solder paste is shown in Appendix I. The underfill materials used, where applicable, were Loctite Hysol FP4549Si [8] and Shin-Etsu SMC375X7 [9].

SECOND GENERATION LEAD-FREE eGaN® FETs

The first two products in the second generation eGaN FETs are EPC2015 and EPC2001. The EPC 2015 is a 40 V, 33 A FET and the EPC2001 is a 100 V, 25 A FET. The second generation product offers improved performance over the prior generation [5]. The basic device cell construction for the lead-free product is identical to the prior generation, but there are three physical changes to the new generation of lead-free product.

The first change is that there is a connection to the silicon substrate that has been brought to the device surface. It is advised that the substrate pad be connected to source potential to get the maximum dynamic performance from the device. The substrate pad can also be left floating or connected to the gate if desired for user applications. The substrate is connected to source potential in reliability testing.

The second change is the width of the solder bars and the solder bar material. The EPC2001 and EPC2015 both have 200 μm wide solder bars compared with 250 μm in the prior generation. The solder material is lead free 95.5/4.0/0.5 Sn/Ag/Cu.

The third change is that the height of the solder bars has been increased from nominal 70 μm +/- 20 to 100 μm +/- 20. The added height allows for greater post-assembly clearance between the FET and the PCB.

In addition, the new generation 40V product has been upgraded to an operating temperature of 150°C compared with 125°C for the prior generation. This upgrade allows the users more operating headroom.

RELIABILITY TEST RESULTS

Table 1 is a summary of the testing results for the first-generation eGaN FETs, and Table 2 is a summary of the results for the second-generation product. Over 1.4 million hours of testing have been accrued through the combination of the two generations of devices (totaling over 1400 units) stress tested at their maximum rated temperature. Device electrical parameters remained stable over the stress period for all tests performed.

Detailed results analysis on earlier testing on the first generation eGaN FETs can be found in the Phase One, Phase Two and Phase Three testing reports that have been posted on the company website [10, 11, 12].

Stress Test	Part Number	Underfill	Test Condition	Results (# of Fails)	Sample Size	Duration	
HTRB	EPC1001	-	T=125°C, Vds=100V	0	45	1000	Hrs
HTRB	EPC1014	-	T=125°C, Vds=40V	0	50	1000	Hrs
HTRB	EPC1012	-	T=125°C, Vds=200V	0	50	1000	Hrs
HTRB	EPC1010	FP4549Si	T=125°C, Vds=200V	0	50	1000	Hrs
HTRB	EPC1010	-	T=150°C, Vds=200V	0	50	3000	Hrs
HTGB 5V	EPC1001	-	T=125°C, Vgs=5V	0	45	3000	Hrs
HTGB 5.4V	EPC1001	-	T=125°C, Vgs=5.4V	0	45	3000	Hrs
HTGB 5V	EPC1010	-	T=150°C, Vgs=5V	0	45	1000	Hrs
HTGB -5V	EPC1001	-	T=125°C, Vgs=-5V	0	50	1000	Hrs
TC	EPC1001	-	-40 to +125°C, Air	0	45	1000	Cys
TC	EPC1014	-	-40 to +125°C, Air	0	50	1000	Cys
TC	EPC1012	-	-40 to +125°C, Air	0	45	1000	Cys
TC	EPC1012	FP4549Si	-40 to +125°C, Air	0	45	1000	Cys
H3TRB	EPC1014	-	T=85°C, RH=85%, Vds=40V	0	45	1000	Hrs
H3TRB	EPC1015	-	T=85°C, RH=85%, Vds=40V	0	45	1000	Hrs
H3TRB	EPC1010	-	T=85°C, RH=85%, Vds=100V	0	25	1000	Hrs
H3TRB	EPC1010	FP4549Si	T=85°C, RH=85%, Vds=100V	0	25	1000	Hrs
MSL1	EPC1001	-	85°C/85RH, 168HR, 3 Reflow	0	50	168	Hrs
AC	EPC1001	-	121°C/100%RH, 29.7psia, 96HR	0	80	96	Hrs
AC	EPC1015	-	121°C/100%RH, 29.7psia, 96HR	0	80	96	Hrs
Power Supply Life Test	EPC1001	-	10A, 250 kHz, 30°C	0	10	1200	Hrs
HTOL	EPC9001	-	10A, 750 kHz, 85°C TJ	0	5	1000	Hrs
HTOL	EPC9002	-	9A, 200 kHz, 85°C TJ	0	3	1000	Hrs

Table 1. Reliability test results of the first-generation eGaN® FETs.

Stress Test	Part Number	Underfill	Test Condition	Results (# of Fails)	Sample Size	Duration	
HTRB	EPC2015	-	T=150°C, Vds=40V	0	45	1000	Hrs
HTRB	EPC2001	-	T=125°C, Vds=100V	0	45	1000	Hrs
HTGB 5V	EPC2001	-	T=150°C, Vgs=5V	0	45	1000	Hrs
TC	EPC2001	SMC375X7	-40 to +125°C, Air	0	45	1000	Cys
TC	EPC2001	-	0 to +100°C, Air	0	50	2300	Cys
H3TRB	EPC2015	SMC375X7	T=85°C, RH=85%, Vds=40V	0	145	1000	Hrs
H3TRB	EPC2015	-	T=85°C, RH=85%, Vds=40V	0	50	1000	Hrs
MSL1	EPC2015	-	85°C/85%RH, 168HR, 3 Reflow	0	25	168	Hrs
MSL1	EPC2001	-	85°C/85%RH, 168HR, 3 Reflow	0	25	168	Hrs

Table 2. Reliability test results for the second-generation lead-free eGaN® FETs.

HIGH TEMPERATURE REVERSE BIAS

During the HTRB test the devices were DC biased with maximum rated breakdown voltage at maximum rated operating temperature. EPC2015 devices were stressed at 150°C with 40 V drain-source bias, and EPC2001 was stressed at 125°C with 100 V drain-source bias. Forty five devices in each group were tested and both groups passed 1000 hours. All device parameters remained stable over the stress period. $R_{DS(ON)}$ versus the stress hours on HTRB is shown in Figure 1, $V_{GS(TH)}$ is shown in Figure 2, and I_{DSS} is shown in Figure 3.

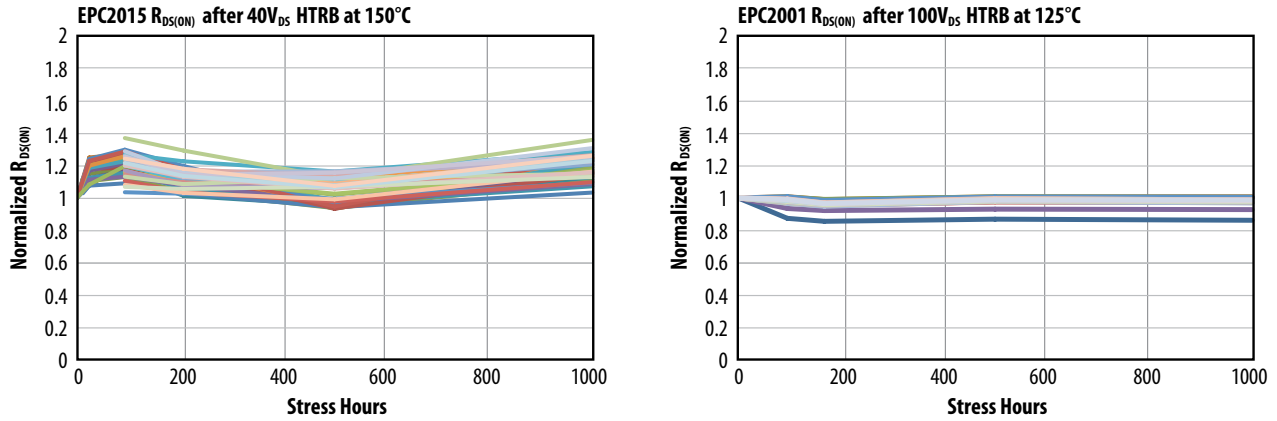


Figure 1. $R_{DS(ON)}$ remained stable after HTRB at the rated operating temperature and rated maximum drain-source bias for both EPC2015 (a) and EPC2001 (b) devices.

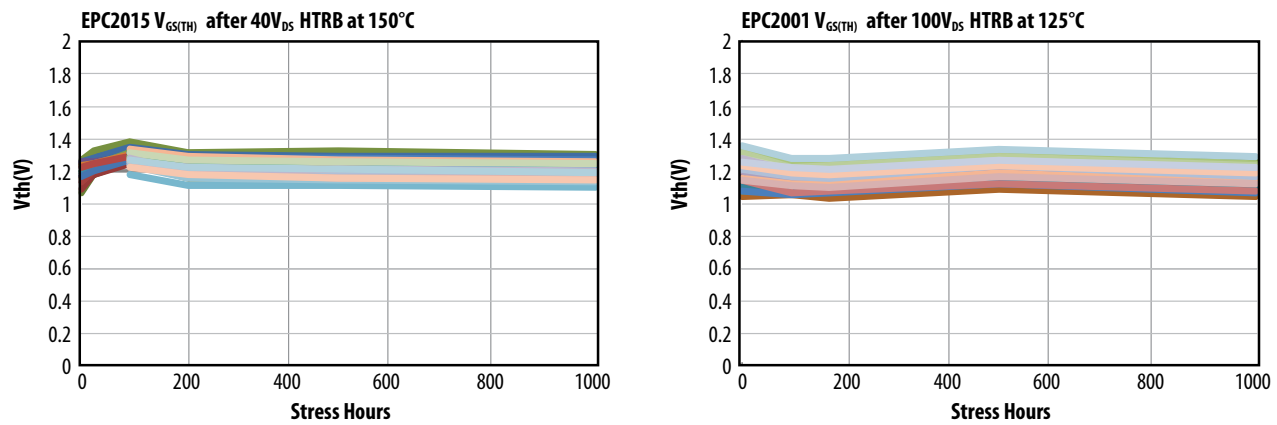


Figure 2. $V_{GS(TH)}$ remained stable after HTRB at the rated operating temperature and rated maximum drain-source bias for both EPC2015 (a) and EPC2001 (b) devices.

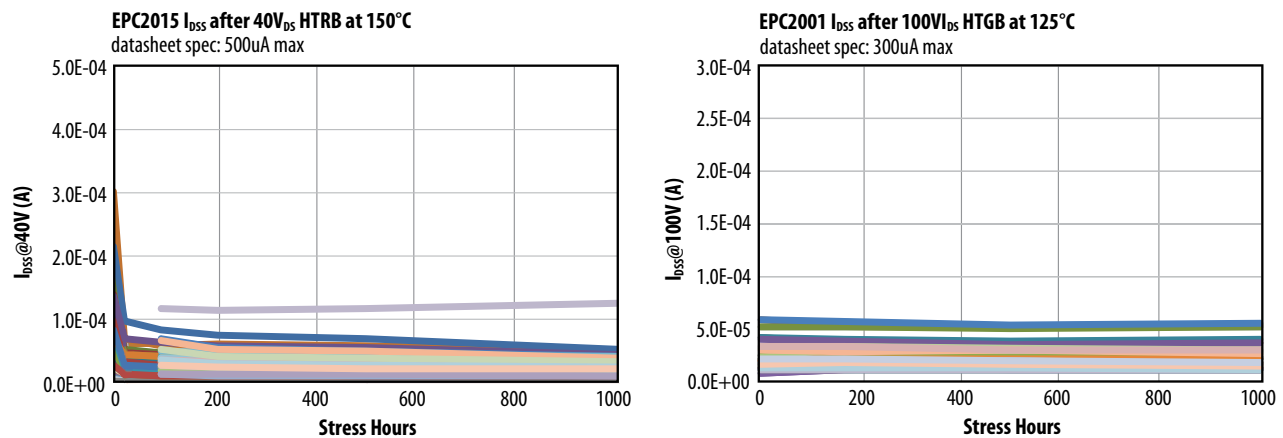


Figure 3. I_{DSS} remained stable after HTRB at the rated operating temperature and rated maximum drain-source bias for both EPC2015 (a) and EPC2001 (b) devices.

HIGH TEMPERATURE GATE BIAS

EPC2001 devices were subjected to 150°C with 5 V gate-source applied for high temperature gate bias (HTGB) test. Forty-five devices were tested and all passed 1000 hours with all electrical parameters remaining stable over the stress period as shown in Figure 4.

HIGH TEMPERATURE HIGH HUMIDITY REVERSE BIAS

EPC2015 devices were subjected to a temperature of 85°C, 85% relative humidity, and 40 volts drain-source bias for high temperature, high humidity reverse bias (H3TRB) testing. Fifty devices were tested and all passed 1000 hours as shown in Figure 5.

Underfill may be needed if the user’s manufacturing process exposes the eGaN FETs to contamination after mounting. To verify the product capability with underfill, a second group of devices was built using Shin-Etsu SMC375X7. A total of 145 parts were tested and all passed 1000 hours stress.

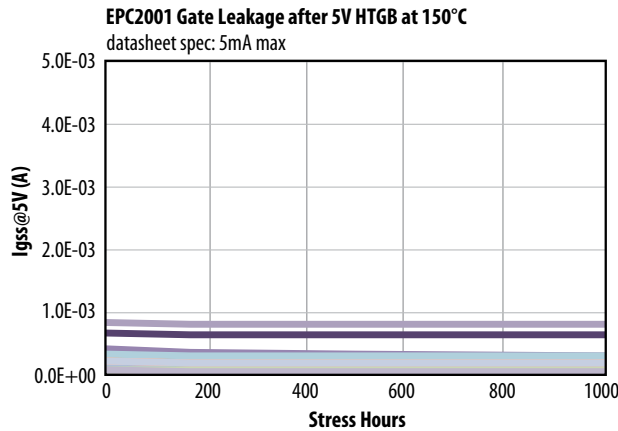


Figure 4. Test results indicating that the gate leakage current of EPC2001 remained stable after HTGB testing with 5V gate-source at 150°C.

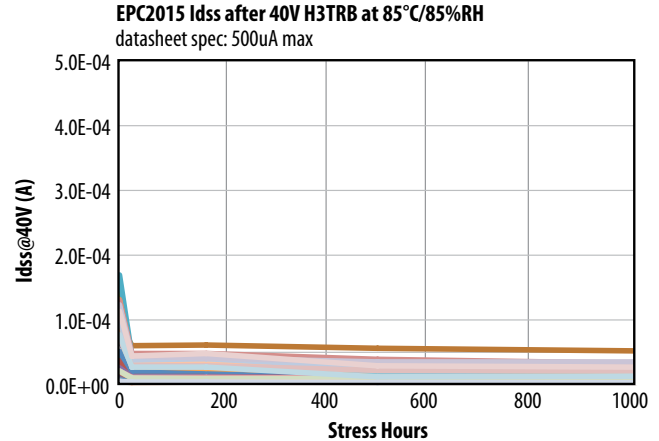


Figure 5. I_{DSS} of EPC2015 devices remained stable after H3TRB testing with 40 V drain-source bias at 85°C and 85% RH.

TEMPERATURE CYCLING

Temperature cycling tests the ability of components and solder interconnects to withstand thermal-mechanical stress. The solder interconnect stability is dependent of solder material, solder joint shape, PCB pad design, and soldering process.

One way to reduce the thermal-mechanical stress is to use underfill material between and around the solder bumps. Figure 6 shows the temperature cycling test results for EPC2001 devices where Shin-Etsu SMC375X7 underfill was used. All parts passed 1000 cycles with the temperature ranging between -40°C and 125°C.

Parts without underfill performed well with temperature cycling between 0 and 100°C. Fifty EPC2001 devices were temperature cycled between 0 and 100°C and all parts passed 2300 cycles, see Figure 7.

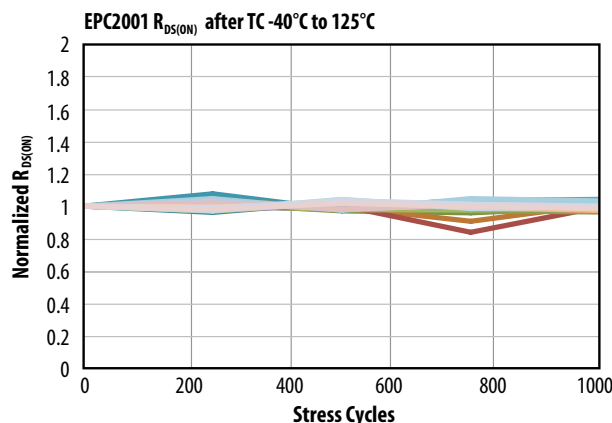


Figure 6. $R_{DS(ON)}$ of EPC2001 using underfill remained stable after temperature cycling test.

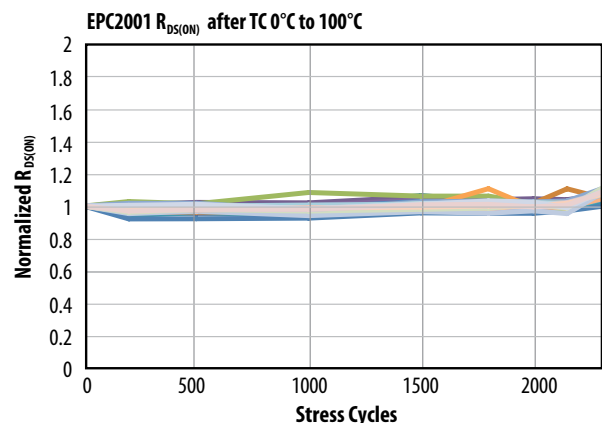


Figure 7. $R_{DS(ON)}$ of EPC2001 without underfill after temperature cycling test. Devices passed 2300 cycles with temperature cycling between 0 and 100°C.

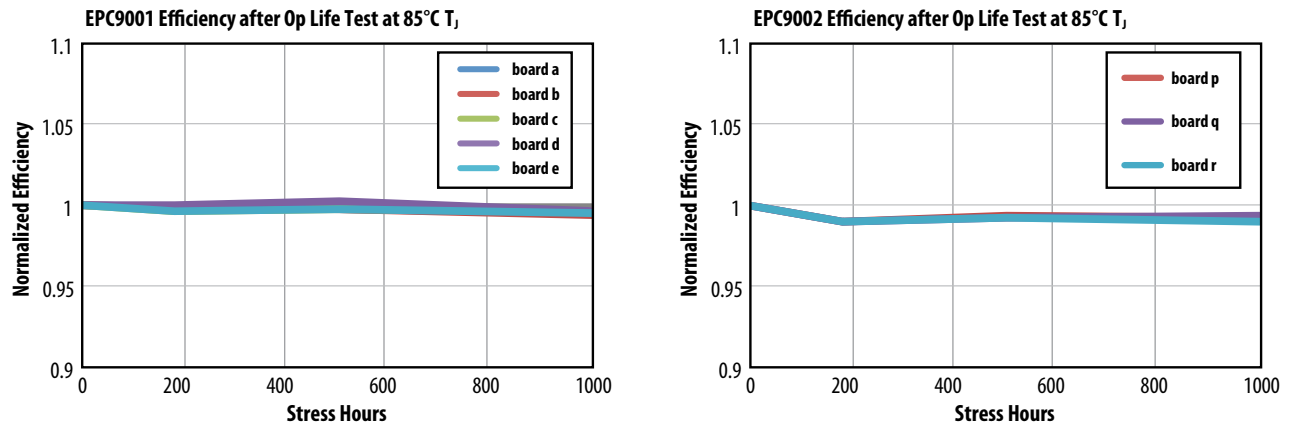


Figure 8. The normalized efficiencies of the development boards in operating test are show for EPC9001 in (a) and for EPC9002 in (b).

MOISTURE SENSITIVITY

EPC's eGaN FETs passed MSL1 classification for the lead-free assembly process. This test was done by subjecting parts to 85% relative humidity and 85°C for a period of 168 hours. Three cycles of reflow were included in the testing (the lead-free reflow temperature profile outlined in IPC/JEDEC J-STD-020 was followed). Components passing MSL1 classification rating means that the parts are non-sensitive to moisture and do not require dry pack. The floor life is considered unlimited under conditions of 85% relative humidity at temperatures not higher than 30°C.

Fifty parts of EPC1001, twenty-five parts of EPC2001, and twenty-five parts of EPC2015 were tested for the MSL1 rating. All three part numbers passed and the electrical parameters remained unchanged post the stress test.

UNBIASED AUTOCLAVE

The unbiased autoclave test is a highly accelerated test employing pressure, humidity, and temperature under condensing conditions in order to accelerate moisture penetration through the external protective material. EPC1001 and EPC1015 wafers were subjected to the autoclave test in a pressure chamber environment of 121°C, 100% relative humidity and 2 atm. (29.7 psia) of pressure for a period of 96 hours. All devices passed the test without noticeable degradation in electrical characteristics.

HIGH TEMPERATURE OPERATING LIFE

The EPC9001 is a half-bridge development board featuring EPC1015 eGaN FETs and includes on-board gate drivers [13]. The EPC9002 is also a half-bridge development board with on-board gate drivers, and features EPC1001 eGaN FETs [14]. The purpose of these development boards is to simplify the evaluation process of the eGaN FET by including all the critical components on a single board that can be easily connected to an existing circuit.

Both development boards were operated open-loop on a multi-position burn-in board with a fixed pulse width and frequency. This kind of test is particularly useful because, in a standard "buck" topology DC-DC converter operation at the high V_{IN}/V_{OUT} ratio, the control FET is turned ON with a very low duty cycle; conversely, the rectifier FET is turned ON with a very high duty cycle. This test therefore simultaneously stresses devices both at

high drain-source voltage and high drain current under actual, fast-switching conditions. Since the rectifier FET has very little switching losses, and the control FET has very little conduction losses, the effects of these two different operating conditions can be evaluated simultaneously.

The EPC9001 board was operated at 22 V_{IN} to 0.85 V_{OUT} , 10 A, at a switching frequency of 750 kHz. The EPC9002 board was operated at 60 V_{IN} to 0.9 V_{OUT} , 9 A, at a switching frequency of 200 kHz.

The board temperature was checked using an FLIR T300 infrared camera. The max temperature was about 70°C and varied from board to board and over time within a few degrees ($\pm 5^\circ\text{C}$). The junction temperature was estimated to be around 85°C taking into account of the junction-to-board thermal resistance [15].

The circuit efficiency was measured at time-zero, 180, 500, and 1000 hours. The EPC9001 efficiency was measured at 300 kHz, 20 V_{IN} to 1 V_{OUT} , 15 A, and the EPC9002 efficiency was measured at 300 kHz, 60 V_{IN} to 1.5 V_{OUT} , 10 A. Typical efficiency measured with a test fixture was about 86% for the EPC9001 and 80% for the EPC9002. The normalized efficiency was plotted in Figure 8(a) for EPC9001 and in 8(b) for EPC9002. Both EPC9001 and EPC9002 showed stable performance.

FUTURE WORK

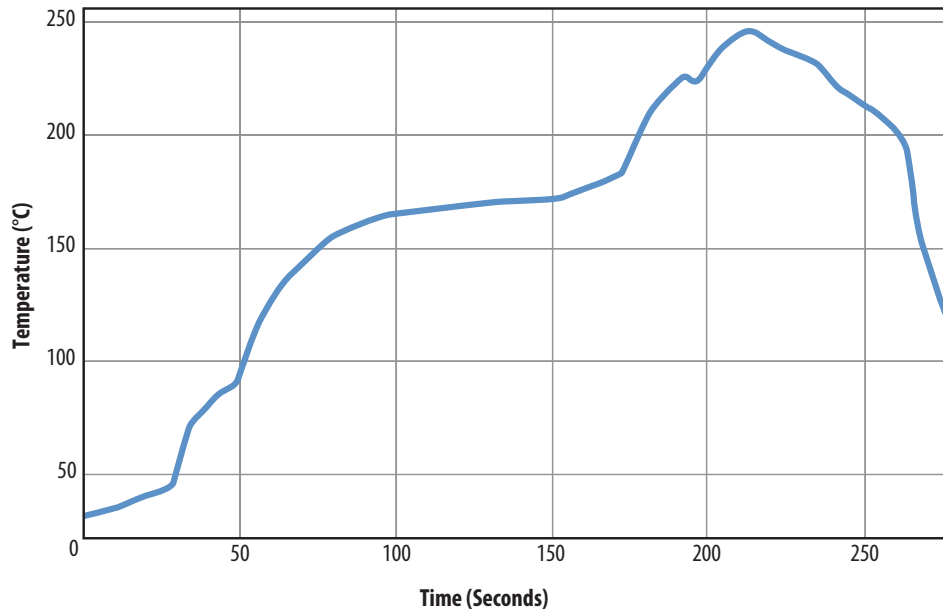
Additional lead-free products ranging between 40V and 200V are planned for introduction in 2011 along with 600 volt eGaN FETs. Additional reliability testing will be conducted as these products are introduced.

SUMMARY

EPC's eGaN transistors bring designers significant performance and size advantages over silicon power MOSFETs. These advantages can be used to improve system efficiency, reduce system cost, reduce size, or a combination of all three. Because EPC's products were designed as power MOSFET replacements, designers can use their existing building blocks, skills and knowledge with only minor changes. Reliability testing is demonstrating that the eGaN technology is robust under a wide range of accelerated life test conditions.

APPENDIX I: REFLOW PROFILE

A typical reflow profile for surface mounting parts onto the adaptor card using the Senju M705-GRN360 solder paste is shown below.

**APPENDIX II: RoHS AND HALOGEN FREE**

EPC's lead-free eGaN FETs are sold as bare die with a line grid array (LGA) of lead-free solder bars. The solder material is 95.5Sn/4.0Ag/0.5Cu. The lead-free product line follows part number nomenclature EPC2xxx.

The final product wafers with solder bumps are RoHS compliant in accordance with the RoHS Directive 2002/95/EC. Details of the test report done by SGS Taiwan Ltd, can be found in the report published by SGS, report number CE/2010/A1486.

EPC's lead-free product was also tested for halogen element levels using the method in accordance with reference BS EN 14582:2007. None of the halogen elements were detected in the test. Details of the test results can be found in the above SGS test report CE/2010/A1486.

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