Application Note: 26-03-2014

AS1744

High Speed Analog Switches

Table of Contents

Revision History

Revision	Date	Owner	Description
1.0	26.03.2014		

1 Applications and the important parameters of analog switches

Analog switches are used in a wide range of products today. From power-routing to audio and video signal routing, all these different applications require different performance parameters of the switches.

Key parameters for the analog switch are maximal ON resistance and ON resistance flatness. Both should be low as possible to have fewer losses and fewer harmonic distortions.

However, other parameters are also important:

- Switching times (high speed switching needed)
- Leakage currents (very small or no current flowing in OFF states to avoid power losses)
- OFF resistance (it should be high; defined indirect by OFF leakage currents)

The block diagram AS1744 is presented in Fig.1. There are 4 switches: COM1 to NC1, COM1 to NO1, COM2 to NC2 and COM2 to NO2.

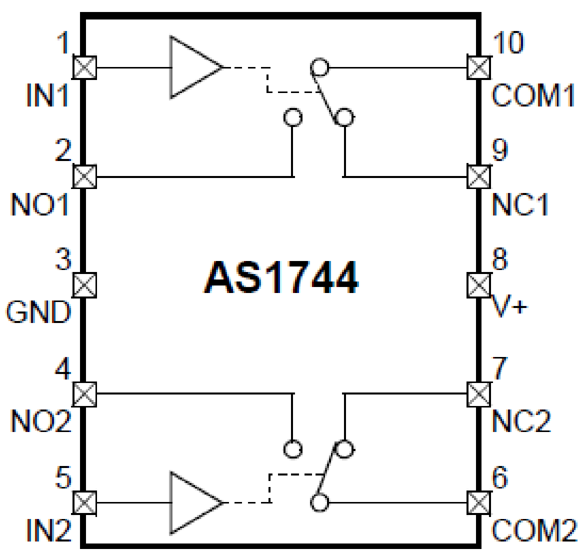

Fig.1: Block Diagram AS1744

2 High speed

Terminal COM can be connected to either NC or NO, dependent on IN terminal. Switching from NC to NO or vice versa is performed very fast. It lasts just few ns, typical Ton = 14ns and Toff = 4ns. First, after one switch is turned OFF, the second one will be turned ON. This feature is called break before make and lasts typ. Tbbm = 10ns (Ton-Toff). That is why Ton takes longer time. This is a very important feature, because otherwise the terminal NC and NO could be connected together for some time, even if they have different signals (voltages), which would cause problems and energy losses. Fig.2 presents what the break before make interval looks like.

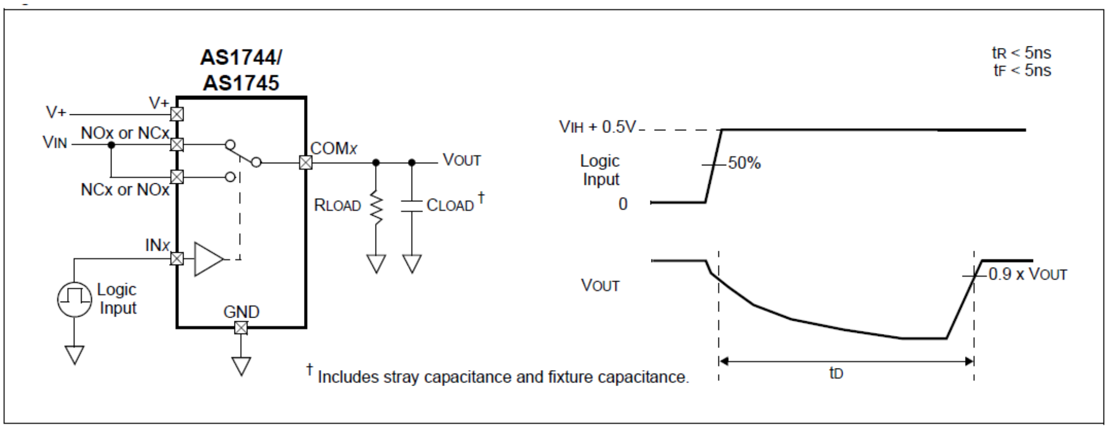

Fig.2: Break before make interval

With a bigger load capacitor, the switches' time and the break before make interval will be longer.

3 Leakage currents and OFF resistance

Leakage currents are tested on every side of the switch. So, not any of the terminals COM, NC and NO can have any high leakage currents if the different voltages are applied on the switch in OFF state. If the same voltage is applied to the terminals of the switch in ON state, there is also a very low possible leakage. The exact values are presented in Fig.3. With this any possible damage in the internal structure (like diodes of input stages is tested) is also excluded.

$I_{NOx(OFF)}$, $I_{NCx(OFF)}$	NO*x* or NC*x* Off-Leakage Current [3]	V+ = 5.5V, V_{COMx} = 1 or 4.5V, V_{NOx} or V_{NCx} = 4.5 or 1V	T_{AMB} = +25ºC	-0.1	±0.01	0.1	nA
			T_{AMB} = T_{MIN} to T_{MAX}	-0.3		0.3	
$I_{COMx(OFF)}$	COM*x* Off-Leakage Current [3]	V+ = 5.5V, V_{COMx} = 1 or 4.5V, V_{NOx} or V_{NCx} = 4.5 or 1V	T_{AMB} = +25ºC	-0.1	±0.01	0.1	nA
			T_{AMB} = T_{MIN} to T_{MAX}	-3		3	
$I_{COMx(ON)}$	COM*x* On-Leakage Current [3]	V+ = 5.5V, V_{COMx} = 4.5 or 1V, V_{NOx} or V_{NCx} = 4.5 or 1V	T_{AMB} = +25ºC	-0.4	±0.1	0.4	nA
			T_{AMB} = T_{MIN} to T_{MAX}	-4		4	

Fig. 3: AS1744 Leakage currents

The OFF resistance is needed to have good signal isolation. In the Data Sheets of analog switches there are usually no specifications for OFF-resistance. However, there is always specification about the parameter called OFF-leakage of the current switch. With this parameter, we can also calculate the OFF-resistance, if we divide the voltage that is applied on the open switch with OFF-leakage current which flows through it:

ROFF = VOFF / IOFF

As an example, analog switch AS1744 has ultra-low leakage currents for all channels, less than 0.1nA at 25°C (typ. 0.01nA), if voltage of 3.5V is applied on the open switch. This means that:

ROFF, MIN at 25C = 3.5V / 0.1nA = 35 GΩ
ROFF, TYP at 25C = 3.5V / 0.01nA = 350 GΩ

The OFF-resistance of typical 350 GΩ is a very good value, which means there are almost no losses during power down (OFF state of the switch), and the isolation of the switch channel is great.

4 ON resistance parameters

For the analog switches' realization the single transistors NMOS or PMOS are usually used. The NMOS has very low resistance for signals near ground (negative supply), and the PMOS has very low resistance for signals near positive supply.

To realize good analog switch as a standard linear product for different applications, the ideal solution is to put NMOS and PMOS parallel, so-called TGATE. So, the switch will have low resistance in the whole throughput domain from ground to supply (please see Fig.4). It is dependent on supply voltage, since the lower the supply voltage, the higher ON resistance.

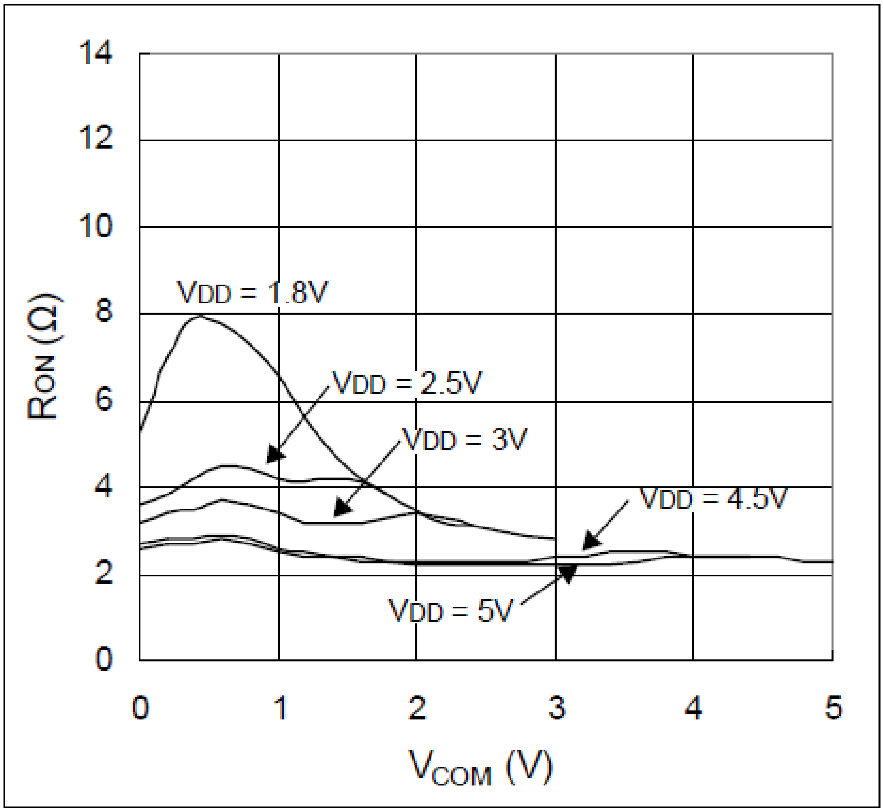

Fig. 4: ON resistance for different supply voltages

5 Results

To achieve very low ON resistance and flatness for analog switches, two parameters are important. For both PMOS and NMOS, the size should be as big as possible, and its voltage thresholds should be as low as possible. Double bigger transistors should have double smaller resistance, but it also costs double the price in production. The smaller thresholds would improve flatness. The resistance peak (maxima) on the left side in Fig.5 is caused by the NMOS threshold and the resistance peak (maxima) on the right side are caused by the PMOS threshold. However, the technology processes with lower transistor thresholds are also more expensive. AS1744 offers an ideal compromise, where the great flatness and low ON resistance are achieved in the whole voltage range and for all temperatures and process variations.

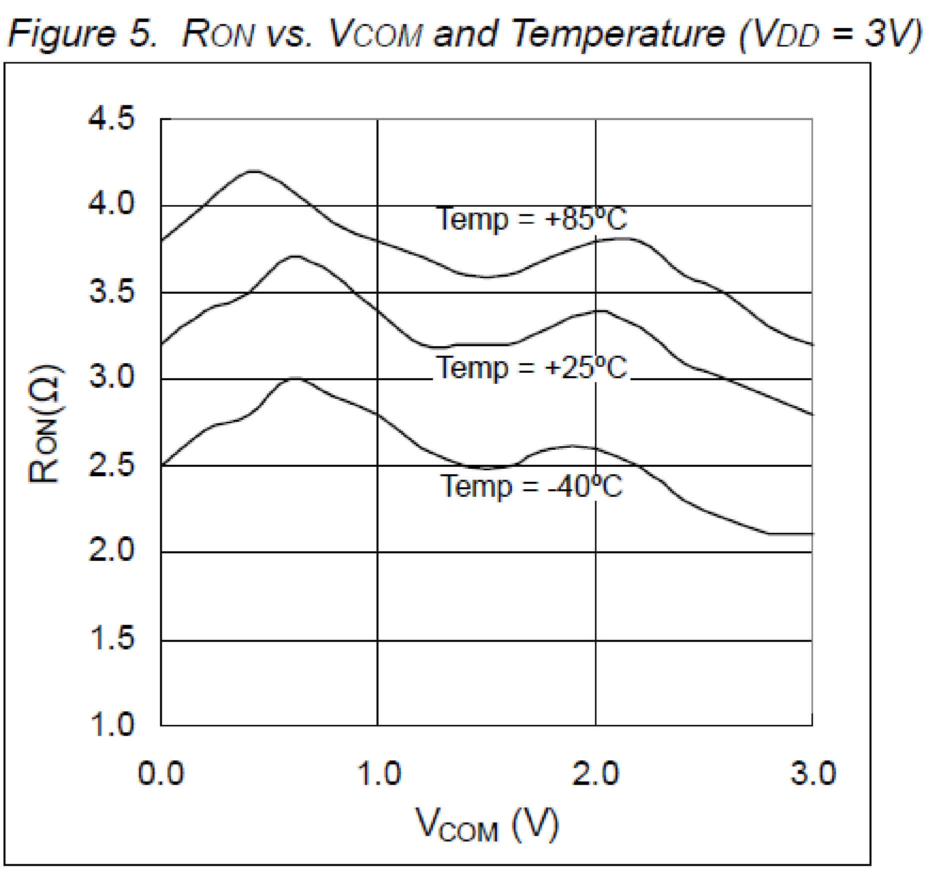

Fig. 5: On resistance flatness

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