An FPGA Approach to Implementing Time-Critical Functions in Multi-Sensor Mobile Designs

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Keeping Pace with Mobile Product Innovation

Today's massive smartphone market is often depicted as a hotbed of innovation for the continual advancement of cost-effective, power efficient solutions. Whenever smartphone developers need a new function, they inevitably find a way to build it at the lowest cost, using minimal board space and consuming as little power as possible. The lessons learned in this highly competitive market eventually trickle down to a wider array of mobile applications where the same concepts can be applied once they have been optimized for minimal cost, power and footprint.

That process is clearly evident with one of the more imposing challenges smartphone designers face today: how to manage the rapidly escalating number of sensors used in today's handsets. As users demand an ever wider array of functions, from location services to high performance cameras, developers are embedding a growing plethora of sensors, such as accelerometers, gyros, barometers, temperature, proximity and light sensors, to provide the crucial data needed to manage these new applications.

Of course this challenge is not limited to the consumer handset market. Designers across the Industrial, Scientific and Medical (ISM) markets, for example, face the same challenge. Whether they are designing scan guns, meter readers or portable scientific instruments, developers attempting to build cost-efficient, battery-powered platforms featuring an applications processor, multiple peripherals and a color display face the same challenge as they try to expand functionality without violating strict power, cost and footprint budgets.

Limited Resources

Traditionally handset designers have addressed this problem by interfacing each sensor to the computing heart of the handset, the applications processor, or in some cases to a dedicated microcontroller, ASSP or custom ASIC. However, as the number of sensors continues to climb, so, too, do the number of challenges. The first issue is limited GPIO resources. With the addition of each new sensor developers face a growing GPIO crunch. Eventually that limitation threatens to impact their ability to support exciting new applications.

Second, each sensor brings with it specific interface requirements. Some support industry standards, such as I2C or SPI, while others use proprietary solutions. This mix of interface requirements places severe constraints on the number of sensors each applications processor or controller can support and, in the process, increases design complexity and extends the product development process.

Third, as the sheer number of sensors in each handset design increases, so, too, does demand for the interrupt-driven applications processor or controller to remain operational for longer periods of time. The continual collection of time-sensitive data from the portable platform's growing array of sensors places additional overhead on the applications processor and, as one of the system's largest consumers of power, additional constraints on the handset's limited power budget.

Simple, Elegant Solution

To address these limitations and meet increasingly aggressive power, cost and footprint targets, some smartphone developers are now moving to an innovative new approach to implementing time-critical functions in multi-sensor mobile designs. Instead of interfacing sensors to an applications processor or microcontroller, an ASSP or custom ASIC, these design teams are opting to use a low density Field Programmable Gate Array (FPGA) specifically optimized for mobile applications. Unlike traditional FPGAs which have historically been too large, expensive and power-hungry for mobile applications, this new class of low density and ultra-low density devices, housed in extremely compact packages, offers designers a highly unique set of advantages that typical silicon architectures cannot match.

Using a simple yet elegant interface hub implemented in a low density FPGA expressly designed for mobile applications, designers can effectively decouple compute-intensive sensor management functions from the computing heart of their portable device. This partitioning of the design offers an ideal architecture for capturing and processing large amounts of data at speeds faster than companion processors or ASSPs while using significantly less power and board space.

At the same time designers gain tremendous design flexibility. With an FPGA optimized for sensor management, designers can easily expand I/O. Ultra low density FPGAs from Lattice Semiconductor , for instance, offer a wide range of I/O counts from 22 to over 250 with relatively linear pricing over the I/O range. Moreover, designers no longer have to juggle interface requirements to meet the limitations of the applications processor or ASSP they have elected to use. Since each I/O on the FPGA is configurable, designers can easily alter their design to support new interface needs by implementing any form of interface on the FPGA's input and supplying whatever interface the application processor requires on the output. This new freedom allows designers to quickly and easily swap out sensors with different performance capabilities regardless of their interface requirements, without worrying about altering code in the processor subsystem or redoing board lines. Engineers can now lock down the interface between the applications processor and FPGA hub early in the design cycle and still make substantial changes to their design midstream without disrupting product development schedules.

Just as important, this new approach pays formidable power dividends. Over the past two decades typical FPGA static power has dropped dramatically from 0.5W to under 50 µW today. Accordingly, an FPGA-based sensor hub operates at an order of magnitude less power than a typical applications processor. But the power savings don't stop there. By interfacing an array of sensors to an event-driven FPGA instead of an interrupt-driven processor, designers no longer need to keep the power-hungry apps processor operational at all times. As an event-driven system, the FPGA-based hub can respond instantly to incoming sensor data and effectively relieve the applications processor from time-consuming sensor management and control operations.

As an example, the block diagram below illustrates a barcode emulation application implemented by Lattice Semiconductor in a recent handset design using an iCE40 FPGA. By offloading timing critical "detect, decide, authenticate" functions from the application processor, this application helped reduce

application processor operation time and reduce power consumption. The second block diagram depicts a typical I/O expansion and sensor management application using a similar iCE40-based solution.

Conclusion

Regardless of application, power, cost and footprint continue to drive mobile markets. As designers across a wide range of mobile applications seek to add new functionality, they must find new cost-, power- and space-efficient methods for integrating and managing a wider array of sensors. A new class of low- and ultra low-density FPGAs offer designers an exciting opportunity to offload sensor management functions from power-hungry applications processors and, in the process, drive down mobile system power consumption, cost and size.