PRACTICAL LOW POWER CPLD DESIGN

A Lattice Semiconductor White Paper

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Introduction

Any engineer involved with portable or handheld products knows that minimizing power consumption is an absolute requirement for today's designs. But only the veterans understand the subtle yet important details that can stretch a systems' battery life to the maximum. In this white paper we'll focus on how those seasoned experts use ultra-low-power complex programmable logic devices (CPLDs) to wring out every last microwatt from the I/O subsystems of their embedded designs.

We'll begin by reviewing how CPLDs are commonly used to shrink power, board space and BOM costs in embedded designs. Next, we'll see how to minimize a CPLD's power consumption in its standby mode, not only by carefully selecting the device itself but also by choosing an appropriate bus parking scheme. Our exploration of power conservation during active operation will include techniques such as selective logic gating, smart I/O design and precision supply voltage management.

CPLDs – The Embedded Engineer's Edge

Although they are especially popular for patching the bleeding edge in emerging applications, CPLDs' low cost, compact size and low-power characteristics make them a great choice for nearly any handheld or portable design. In these applications, they are commonly used to consolidate logic functions, expand the host processor's I/O capabilities and monitor critical inputs so the processor can spend more time in its low-power sleep mode.

When used as I/O expansion devices, CPLDs like the ispMACH 4000ZE devices (Figure 1) give simple embedded processors the additional signal lines and addressing capabilities they need to support displays, buttons, LEDs, serial or parallel I/O, or storage interfaces. Designers also frequently use them as shims between a general-purpose processor and a more specialized chip set in designs for, among others, smart phones, GPS systems, remote industrial sensors and digital video cameras.
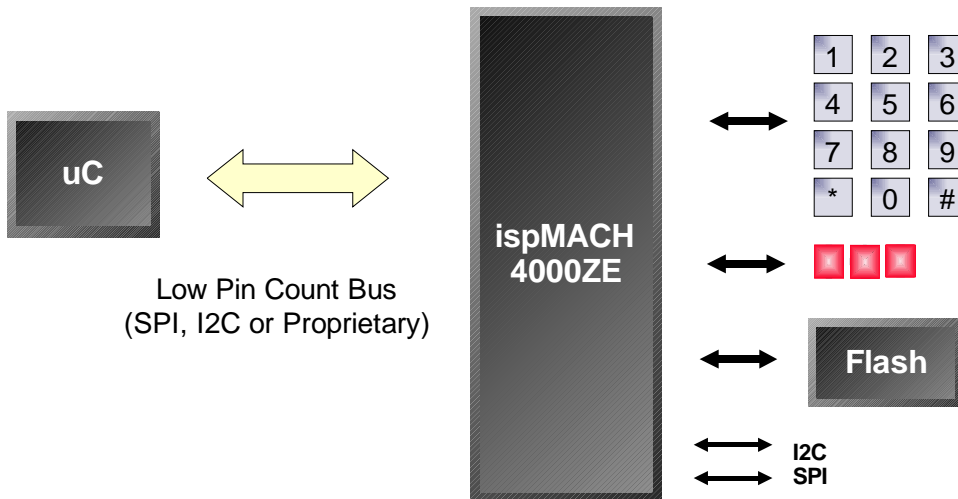
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Figure 1 – I/O Expansion Using a Lattice ispMACH 4000ZE CPLD

Standby Power Basics

The first step in mastering CPLD power consumption is to understand how the devices behave in their operating and standby (also known as static) states. Since many CPLDs spend the majority of time in standby, we'll take a closer look at this often-misunderstood mode first.

A CPLD is said to be in its standby state when the device has power applied to its inputs but its internal logic is not being clocked. In this state, the CPLD still draws some power due to its leakage and bias currents (although significantly less than when it's actually operating). Leakage currents vary as a function of temperature, operating voltage and the manufacturing process.

The bias current within a CPLD is generated by loads such as internal oscillators, pull-up/down circuits on I/O lines and other fixed overhead that are present regardless of whether the device's logical functions are being used. Unlike leakage currents, bias currents are relatively stable over temperature and voltage range, but they can be controlled by proper device configuration.

Managing Leakage with Smart Specsmanship

Since a CPLD's leakage current is primarily determined by how it's made, the first step is to take a close look at the specifications for the candidate parts provided on the manufacturer's data sheets. But simply buying the part with the lowest advertised power consumption does not guarantee that it will perform exactly like that in your design. An experienced designer understands that finding the actual relationship between the "typical" and "maximum" current

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ratings requires some interpretation based on the specifics of their application (Figure 2). In many applications, the so-called typical currents listed in the data sheet provide a very useful approximation of what the CPLD will draw. Nevertheless, there are several questions that need to be asked to insure that a design's estimated and actual power consumption remain relatively close.

Supply Current

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4032ZE						
$ICC^{1, 2, 3, 5, 6}$	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	50	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	58	—	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	60	—	µA
$ICC^{4, 5, 6}$	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	10	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	13	25	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	15	40	µA
ispMACH 4064ZE						
$ICC^{1, 2, 3, 5, 6}$	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	80	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	89	—	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	92	—	µA
$ICC^{4, 5, 6}$	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	11	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	15	30	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	18	50	µA

1. Frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. V_{CCO} = 3.6V, V_{IN} = 0V or V_{CCO}, bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified standby I_{CC}.
5. Includes V_{CCO} current without output loading.
6. This operating supply current is with the internal oscillator disabled. Enabling the internal oscillator adds approximately 15µA typical current plus additional current from any logic it drives.

Figure 2 – Supply Current Specifications

One of the first things to consider is what percentage of the overall system power budget the CPLD is responsible for. If it's a small fraction, say 5%-10%, even a worst-case situation will result in a relatively small change in overall power consumption. If the CPLD represents 20% or more of the power budget, it's probably time to start thinking about basing the design on a nominal standby current that's closer to the maximum current listed in the data sheet. You should also consider the number of CPLDs (and other devices) in your design. As the number of devices on a given board grows, so does the probability that their aggregate power consumption is close to the total of their typical current ratings. Finally, you need to consider the potential impact if one of your products ends up with components that drive it to its worst-case power level. Will the higher power dissipation simply shorten its operating life, or will it create a fire hazard?

If you looked at the data sheet in Figure 2 carefully, you probably noticed that standby power also varies according to operating temperature and Vcc (supply voltage). That's because the CPLD's leakage current tends to increase as its temperature rises. In fact, keeping your design adequately cooled will improve its standby power consumption. Since leakage current is even more strongly related to Vcc, there are even bigger power savings to be had by keeping the

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supply voltage as low as possible. But since careful supply voltage management produces even larger dynamic power savings, we'll review this when we cover operating power management.

Taming Bias Currents

Now that you've controlled your CPLD's leakage currents by choosing the appropriate device, it's time to put your engineering skills to work trimming its bias currents. The techniques used to manage these bias currents fall roughly into two kinds of activities:

1 – Making sure that the CPLD's standby configuration is not in conflict with the pull-up/pull-down or other bus parking techniques used by the other devices it's attached to.
2 – Dynamically controlling internal features (such as oscillators) so that they are only turned on as needed. Depending on the CPLD being used, this can be a great way to add a bit more to your design's standby time.

Parallel Parking 101

In many designs, the embedded host processor can use its own bus parking scheme to maintain the desired logic level on a bus or I/O line, so the only thing you'll have to do to prepare the CPLD for standby mode is to make sure that its active bus management features are disabled. In other applications, an active pull-up or pull-down circuit elsewhere on the bus can also relieve the CPLD from having to manage the bus during standby.

But just because the CPLD is not required to do anything does not mean that you don't have to either. Taking the time to verify that there is only one device driving the line is a critical task, since a logic conflict on a single pin can result in standby power consumption levels 2-15 times the nominal 10 uA idle power level of the entire chip.

In situations where the host's bus parking mechanism is not available, it's time to make use of the pull-up/down and Bus Hold functions available in most modern CPLDs. As with most devices in its class, the I/O pins of the Lattice ispMACH 4000ZE CPLD are equipped with selectable pull-up and pull-down resistors that can be used to provide the appropriate logic level during a standby state (Figure 3). The 4000ZE series is also equipped with a power-saving Bus Keeper function (also know as Bus Hold), a weak active driver circuit that can be set at either an active one or zero while drawing much less power than a simple resistor. *A note of caution: While the Bus Keeper function offers significant power savings, care must be taken to make sure it's the only active device on the line or you run the risk of turning it into a large current sink*.
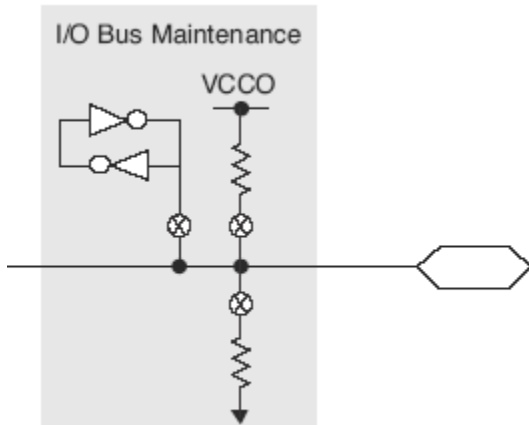
Figure 3 - CPLD Bus Maintenance Options

Managing Dynamic Power

There are two types of dynamic power a designer needs to be concerned about. The first part of the operating power budget is the power required to run the parts of the CPLD that are actually doing the work. The other part of your management strategy involves turning off the inputs to the parts of the CPLD that you don't need at the moment to keep them from toggling or, where possible, turning them off entirely.

Precision Supply Management

Although it's likely that many parts of the CPLD's logic will be in continuous use and cannot be disabled for any meaningful period of time, you can still achieve some power savings by using as low a supply voltage as practically possible. Since power consumption is a function of the square of the voltage, investing in a 1% accurate switching regulator that lets your design run towards the bottom of the CPLD's operating range allows you to save considerable power. For example, if a CPLD with a nominal 1.8V operating voltage is run at 1.65V, it consumes around 30% less power - and that's not even counting the reduced leakage current you'll see at the lower Vcc.

Selective Logic Gating

Like most CPLDs of its class, the ispMACH 4000ZE has a function (Lattice calls it "Power Guard") that can be used to disable individual inputs when the logic they are attached to is not needed. The device's Block Input Enable lines can be used by either the host processor, other external logic or other parts of the CPLD to keep selected blocks of the CPLD's logic from being clocked (Figure 4). For

example, if part of the CPLD is being used as a decoder circuit, the host processor can enable it only when that function is being used and allow it to remain dormant the rest of the time.
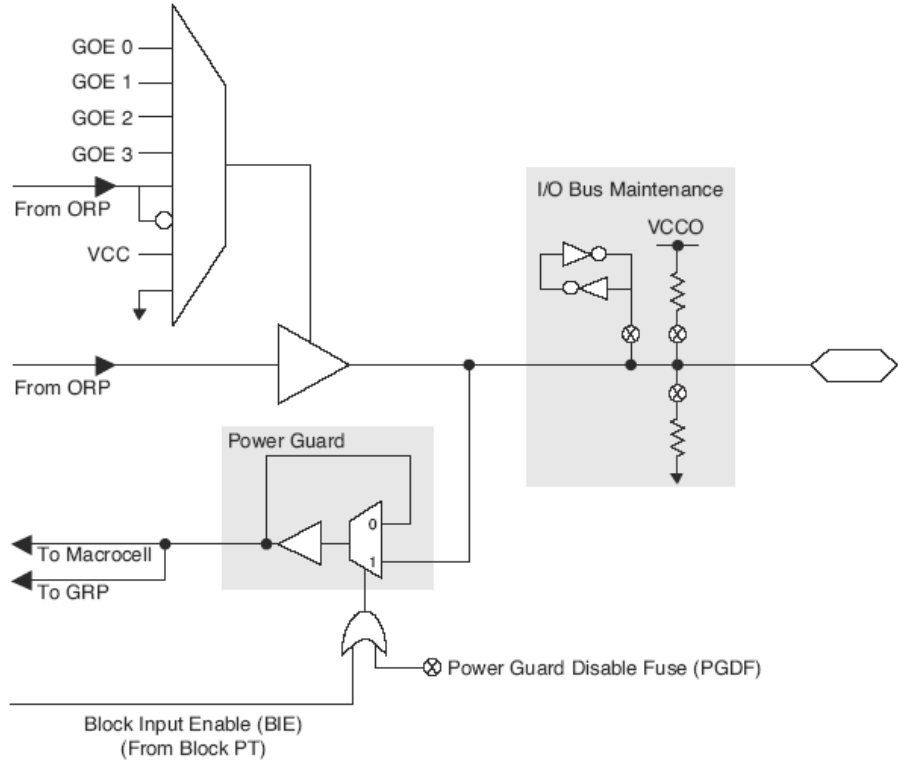

Figure 4 - Power Guard Circuitry

Depending upon the application, using Lattice's Power Guard or other techniques to disable clocking to selected CPLD input pins can dramatically reduce dynamic power consumption. This is especially true if the clock frequency of the logic signals exceeds around 30 MHz. Figure 5 illustrates the potential power savings that can be realized from selective logic clocking techniques.
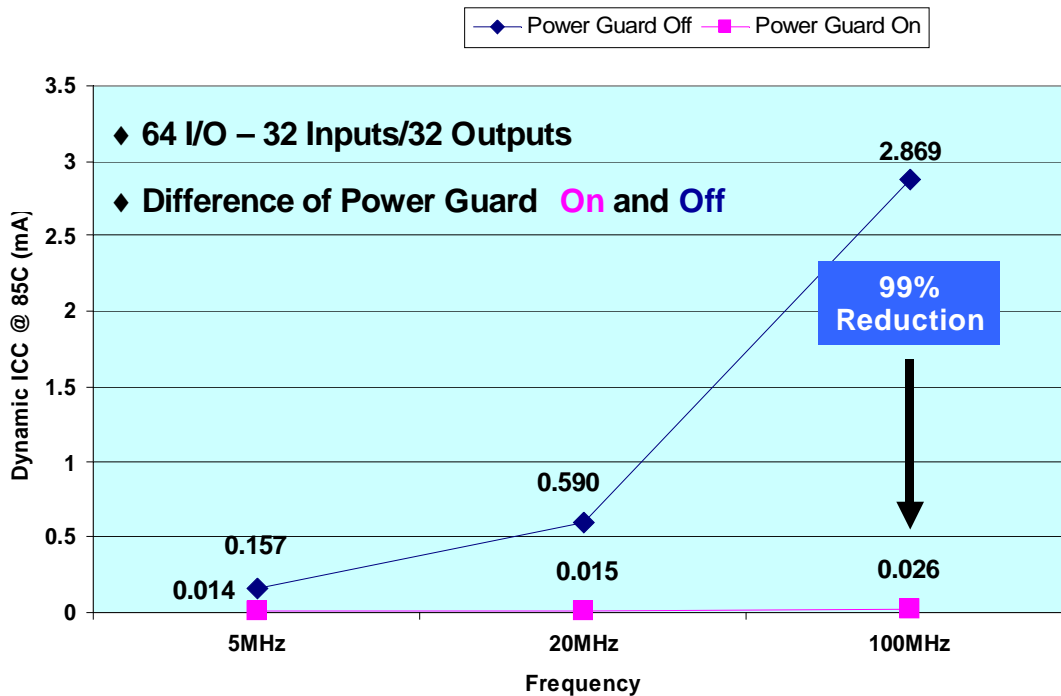
ispMACH 4064ZE-TN100 Power Guard Advantage

Figure 5 contents:
Legend: Power Guard Off (diamond), Power Guard On (square)

Y-axis: Dynamic ICC @ 85C (mA), scale 0 to 3.5
X-axis: Frequency

- ♦ 64 I/O – 32 Inputs/32 Outputs
- ♦ Difference of Power Guard On and Off

Data points:
- 5MHz: 0.157 (Off), 0.014 (On)
- 20MHz: 0.590 (Off), 0.015 (On)
- 100MHz: 2.869 (Off), 0.026 (On)

99% Reduction

Figure 5 – Power Guard Energy Savings

I/O Design for Low Power

In addition to using the techniques already described, most projects present the savvy engineer with additional opportunities to save the odd microwatt – if he or she is willing to look closely for the tiny energy vampires that lurk within many designs. One great example is the ubiquitous pull-up resistors that provide a sense voltage for switches and relays attached to a CPLD's input lines (Figure 6). By using a CPLD output or some other control line to supply voltage to the sense lines only when they are being read, a designer can eliminate the small but steady current that occurs when the sense line is grounded.
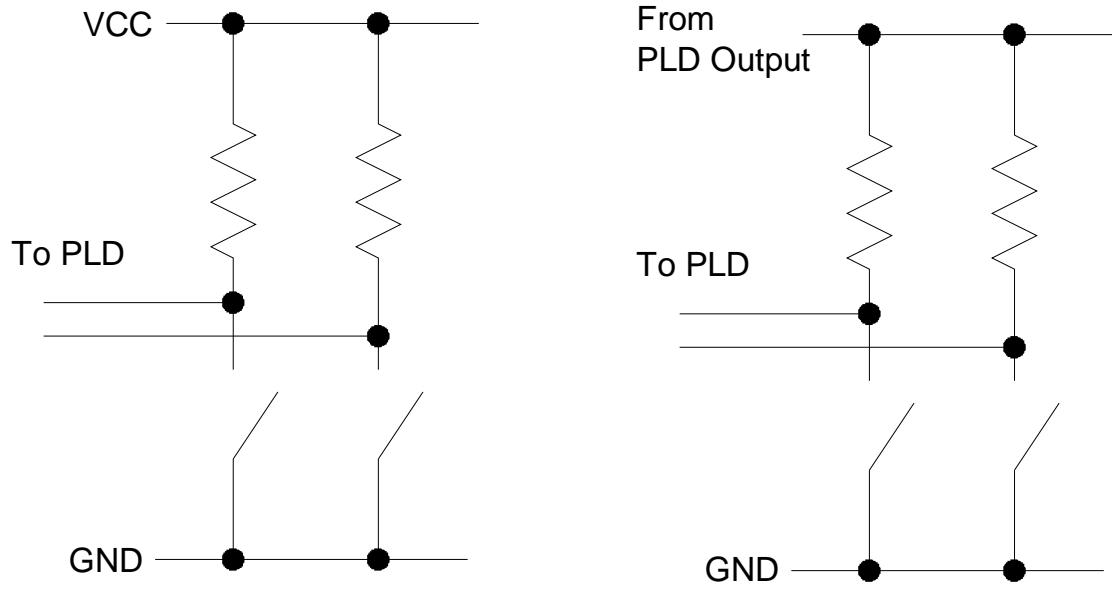
DIP Switch Sense -- Option A   DIP Switch Sense -- Option B

Figure 6 - Passively and Actively-Powered Switch Sense Lines

Other Tips

- Configure the CPLD's JTAG interface pins to float to avoid leakage current.
- Keep VCCO I/O rail levels above VCC. The closer in the voltage, the more current is drawn.
- Use slow slew rate I/Os when possible.

Conclusion

Most CPLD-based designs include at least a few dark corners where energy-hungry vampires can lurk while they quietly drain batteries of power. Fortunately, the careful application of a few important principles can put an end to these pesky parasites:

- When choosing CPLDs and other components pay careful attention to both their static and dynamic power consumption ratings: they vary according to supply voltage, temperature and operating frequency.
- Apply equal care to interpreting how the "min," "max' and "typical" power consumption specifications will affect your design.
- Minimize a CPLD's bias currents by making sure its standby configuration is not in conflict with the other devices it's attached to and that any unneeded internal features are disabled.
- Manage dynamic power by clocking only the parts of the CPLD that are needed at the moment. Lattice's Power Guard feature provides a simple way

- Additional dynamic power savings can be realized using precision supply control to drive logic using as low a supply voltage as practically possible.
- Check the I/O connections to see if there are any unnecessary power-robbing pull-up/down resistors that can be eliminated, or selectively powered only when needed.

If you carefully apply these tools of the trade to your next project, not even the stealthiest power vampire can hide from your vengeful grasp, and your products will enjoy the long life they deserve. ###

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