ispMACH® 4000ZE - Enabling CPLDs in Ultra High Volume, Low Power Applications

A Lattice Semiconductor White Paper

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Introduction

Design engineers are constantly challenged to develop new products with improved features and functionality over previous generation and competitive products. The increasing demand for smaller, lower power and lower cost products with each subsequent generation adds another layer of complexity to the engineer's already difficult job. Design engineers are always looking for enhanced solutions to satisfy low power, small size and quick time to market requirements for consumer products. This white paper will discuss some of the factors design engineers consider when developing a consumer product. Next it will discuss how Lattice Semiconductor's ispMACH® 4000ZE family of zero-power Complex Programmable Logic Devices (CPLDs) enables the use of CPLDs in ultra high volume, low power applications, a market that was once dominated by Application Specific Integrated Circuits (ASICs) and Application Specific Standard Products (ASSPs).

Design Considerations

Traditionally, ASICs and ASSPs were the optimal solutions for high volume, low power, cost sensitive consumer products, and CPLD use was limited to only the prototyping phase. Examples of these consumer products include mobile phones, PDAs, digital still cameras, camcorders, handheld GPS devices and personal media players, just to name a few. Recent advances in CPLD technology, however, have opened the door for designers to standardize on the CPLD as an integrated solution for random logic and various programmed functions in these products. Some of the most important considerations for an engineer when choosing components for a new design are power consumption, time to market, form factor and component cost.

The ispMACH 4000ZE Solution

In order to compete in the consumer products market, CPLD manufacturers introduced zero-power CPLD families. Zero-power means that the CPLD uses a number of internal features along with core logic that are designed to substantially reduce device power requirements in most applications.

Several new features in Lattice's ispMACH 4000ZE family make it ideal for use in ultra high volume, low power applications. Features unique to the ispMACH 4000ZE family, which are not available in Lattice's original zero-power ispMACH 4000Z family, include per-pin Power Guard I/O control, input hysteresis, an on-chip oscillator and timer, per-pin programmable termination and ultra-small space-saving packages. Each of these new features is explained in detail below.

Achieving Low Power with Power Guard

When designing a handheld, battery operated system, designers will do everything feasible to reduce power consumption and increase battery life. There are a number of ways engineers can architect their design to reduce power consumption including reducing clock speeds, adding bus terminations, designing for low voltage operation and limiting the bus loadings. All of these design practices, when implemented, can extend battery life by lowering the overall system power

requirements. Nonetheless, even with power-reducing design techniques implemented, a standard CPLD's power requirement can be prohibitive for use in handheld battery-powered devices.

Disconnecting the CPLD array logic from external input signal changes is an excellent way to reduce power and increase battery life. This feature, called Power Guard in the ispMACH 4000ZE family, provides current levels close to standby current in the system. As shown in Figure 1, Power Guard consists of an enabling multiplexer between an I/O pin and input buffer, and its associated circuitry inside the device. If the enable signal (E) is held low, all inputs (D) can be optionally isolated (guarded), such that, if any of these were toggled, it would not cause any toggle on internal pins (Q). In other words, a toggling I/O pin will not cause any internal dynamic power consumption.

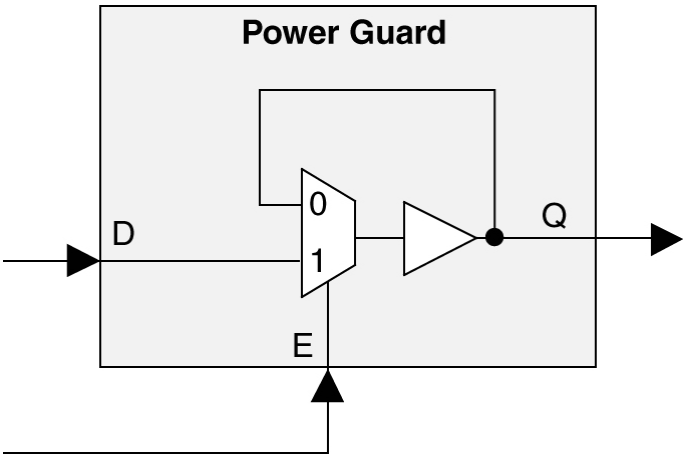

Figure 1. Power Guard Signals

ispMACH 4000ZE devices contain between two and 16 I/O blocks. All the I/O pins in a block share a common Power Guard Enable signal. For a block of I/Os, this signal is called a Block Input Enable (BIE) signal. BIE can be generated internally using logic, or could come from external sources using one of the user I/O or input pins. Any number of I/O pins in the block can be programmed to ignore the BIE signal. Thus, the feature can be enabled or disabled on a pin-by-pin basis.

Using the 64-macrocell ispMACH 4064ZE device as a reference, enabling Power Guard on all but the two active inputs effectively reduces the dynamic I_{CC} by 99%. In this example the two inputs fully utilized all 64-marocells of the device's internal logic. Dynamic I_{CC} was reduced from 2.9 mA to 26 µA, as shown in Figure 2.

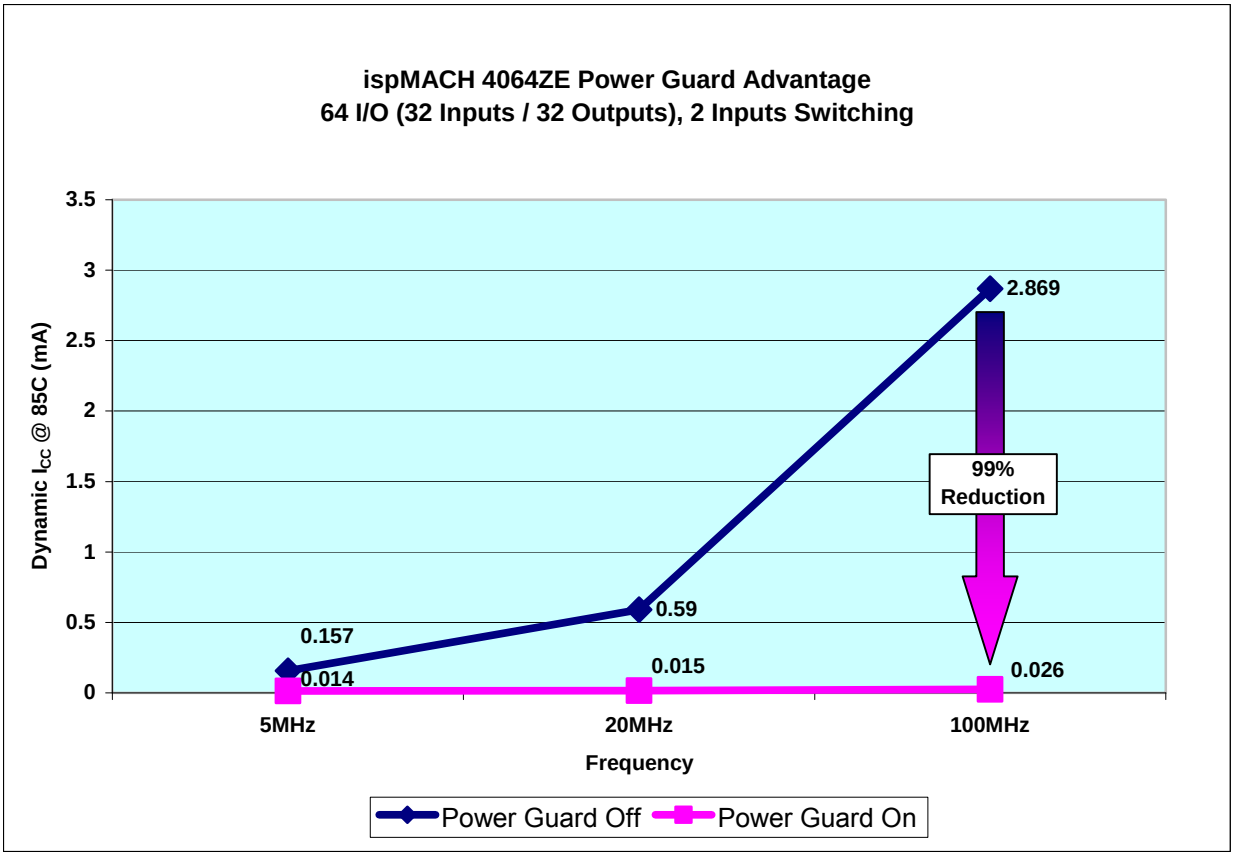

Figure 2. Reduced Dynamic ICC with Power Guard

Ultra-Small Space-Saving Packaging

The trend with each progressive generation of hand-held devices is to fit additional product functionality into a smaller board space. This is accomplished through circuit integration, and CPLDs are a fundamental part of the solution. CPLDs allow quick implementation of fixes for problems that occur in ASSP and ASIC devices. They also enable the integration of discrete logic solutions and special functions such as; memory controllers, interface bridges, LCD/touch screen interfaces, watchdog functions and power management.

As end products get smaller, board space becomes increasingly more valuable. Lattice offers the ispMACH 4000ZE family of CPLDs in a wide variety of low-cost packages that are as small as 5x5mm. The number of I/Os ranges from 36 to 112 I/Os. The highest ratio of available I/O lines to package size is found in chip scale BGA (csBGA) packages, shown in Figure 3. The 64-macrocell ispMACH 4064ZE provides 52 I/O lines in a 5x5mm csBGA package; the 256-macrocell ispMACH 4256ZE provides 112 I/O lines in a 7x7mm csBGA package.

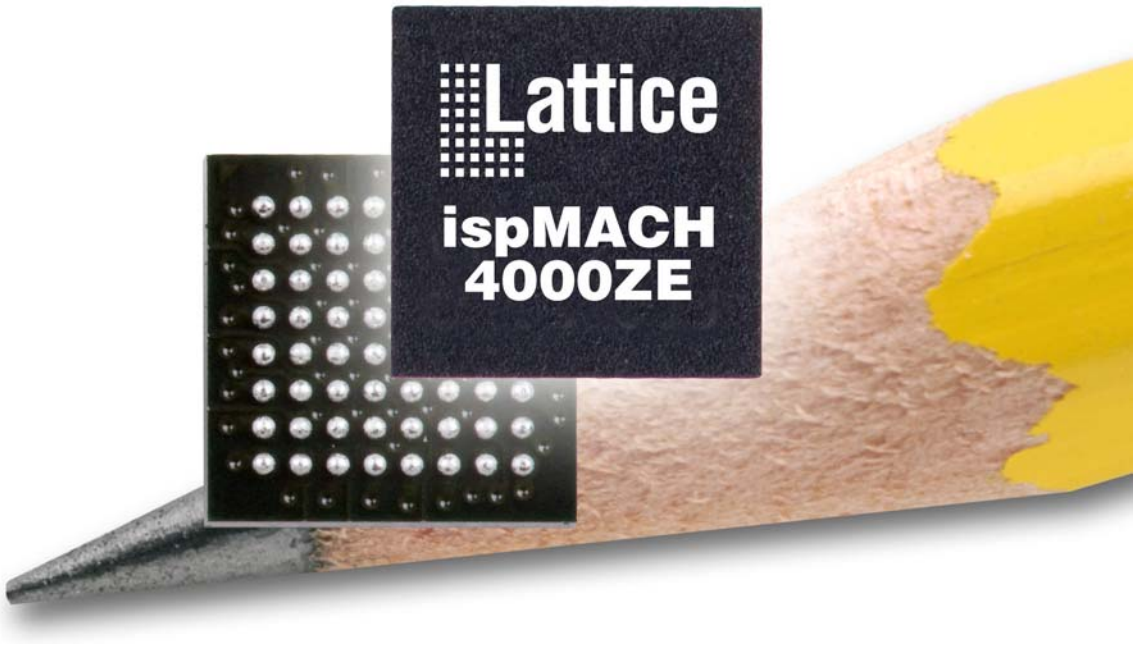

Figure 3. 5x5mm Chip Scale BGA Packages

On-Chip Oscillator and Timer

Oscillators are typically used for power up sequencing, keypad scanning or display controller applications in a system. On-chip oscillators have been integrated within FPGA devices for several generations. To help reduce overall system costs, on-chip oscillators have recently been integrated into advanced CPLDs. The CPLD's on-chip oscillator can be used for miscellaneous housekeeping functions such as watchdog heartbeats, digital de-glitch circuits and to control state machines. Integrating the oscillator in the CPLD allows a reduction in the total system device count and eliminates the cost of a dedicated oscillator chip. In designs that do not need the on-chip oscillator, the block may be disabled so as not to draw any additional power. Every member of Lattice's ispMACH 4000ZE family, including the smallest 32-macrocell device, includes an on-chip oscillator and timer. The nominal frequency of the oscillator is 5 MHz, whereas the timer output of the oscillator can be configured to provide an output clock frequency as low as 5 MHz.

Programmable Termination

Most zero-power CPLDs provide some form of programmable I/O termination to reduce power consumption of I/O due to externally tri-stated busses. Non-terminated or floating inputs can use an inordinate amount of power as the signal moves between high and low logic levels. Programmable termination options include the following four settings: bus-keeper latch, pull-up, pull-down or no termination. The Lattice ispMACH 4000ZE family provides all four of these options, and any one of the termination options can be assigned to each individual input pin. The default in both hardware and software

is such that when the device is erased or if the user does not specify, the input structure is configured to be a pull-down resistor.

Input Hysteresis

Input hysteresis improves I/O noise immunity when the device receives slow transitioning input signals or it is operating in a noisy environment. Older, less efficient CPLDs provide the option to turn input hysteresis on or off to save power and improve I/O response time. The newest families of CPLDs have very efficient I/O cells and input hysteresis that is always on with 3.3 V and 2.5 V I/O standards. The ispMACH 4000ZE family has an always on, 250 mV input hysteresis for each input at 3.3 V and 2.5 V I/O standards.

Combining Quick Time to Market with Low Cost

With today's rapidly changing market requirements, a quick time to market is becoming a top priority. Standardizing on a CPLD instead of an ASIC or ASSP can dramatically improve the time between a product's development cycle and its release to market. CPLDs have a quick development time from prototyping to final production, whereas, ASICs and ASSPs have a lengthy development time. In addition, ASIC and ASSP development requires significant NRE charges. With the 32 macrocell ispMACH 4032ZE available for around $0.70 in 100,000 piece quantities, the ASIC and ASSP ROI are becoming less and less attractive.

Conclusion

Consumers' demands for new and improved products will continue to push engineers to find innovative design solutions. The addition of Power Guard I/O control, input hysteresis, an on-chip oscillator, per-pin programmable termination and smaller packages to Lattice's original zero-power ispMACH 4000Z family, the new ispMACH 4000ZE family of CPLDs truly enables the use of CPLDs in ultra high volume, low power applications.

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