LONG-TERM SUPPORT
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# 4Mbit Latched SRAM

## 256Kx16 HIGH SPEED ASYNCHRONOUS CMOS STATIC RAM with LATCHED ADDRESS & ECC

## KEY FEATURES:

- High-speed access time: 12ns, 15ns
- Single power supply
  –2.4V-3.6V VDD
- Ultra Low Standby Current with ZZ# pin
  -IZZ = 80uA @ 125°C
- Error Detection and Correction per individual 8-bits (byte) with optional ERR1/ERR2 output pin:
  -ERR1 pin indicates 1-bit error detection and correction.
  -ERR2 pin indicates multi-bit error detection
- ALE# pin to latch Address & CS# signals.
- Industrial and Automotive temperature support
- Lead-free available

## BGA PINOUT:

48-Pin mini BGA (6mm x 8mm) with ZZ# and ERR1/2

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| A | LB# | OE# | A0 | A1 | A2 | ZZ# |
| B | I/O8 | UB# | A3 | A4 | CS# | I/O0 |
| C | I/O9 | I/O10 | A5 | A6 | I/O1 | I/O2 |
| D | VSS | I/O11 | A17 | A7 | I/O3 | VDD |
| E | VDD | I/O12 | ERR1 | A16 | I/O4 | VSS |
| F | I/O14 | I/O13 | A14 | A15 | I/O5 | I/O6 |
| G | I/O15 | ERR2 | A12 | A13 | WE# | I/O7 |
| H | NC | A8 | A9 | A10 | A11 | ALE# |

## DESCRIPTION:

The ISSI IS61/64WV25616LEBLL are high-speed, low power, 4M bit Latched static RAMs organized as 256K words by 16 bits. It is fabricated using ISSI's high-performance CMOS technology and implemented ECC function to improve reliability.

Our highly reliable process coupled with innovative circuit design techniques including ECC (SEC-DED: Single Error Correcting-Double Error Detecting) yields high-performance and highly reliable devices.

When CS# is High (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels. Especially Ultra Low Standby Power at Snooze mode with ZZ# Low.

ALE# pin enables Address and CS# signals to be latched by asserting ALE# input Low
When ALE# is High, the address and CS# latches are in the transparent state. If ALE# is tied High, the device can be used as an Asynchronous SRAM.

When ALE# is Low, the address and CS# latches are in the latched state.

This input latch simplifies read and write cycles by guaranteeing address hold time in a simple fashion.

The IS61/64WV25616LEBLL are packaged in the JEDEC standard 48-pin mini BGA (6mm x 8mm), and 44-pin TSOP (TYPE II).

## Serving Major Market Segments with Quality and Long-Term Support


Automotive | Communications | Medical | Industrial

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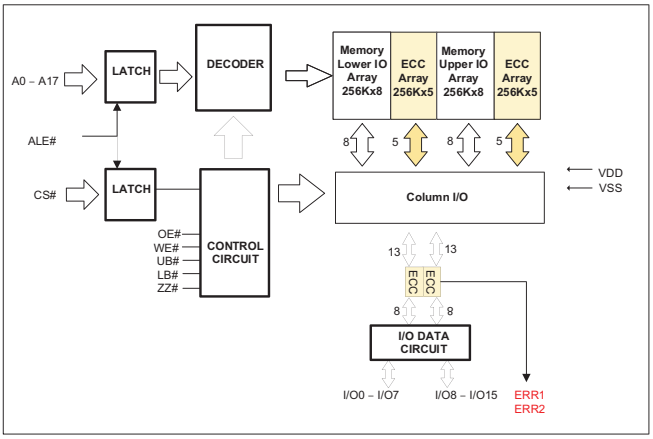
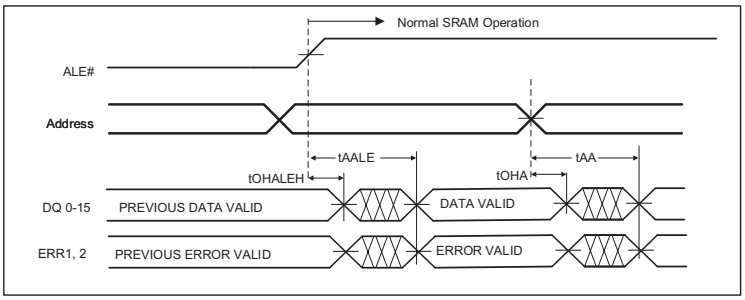
# IS61WV25616LEBLL
# IS64WV25616LEBLL

## FUNCTIONAL BLOCK DIAGRAM:




## TIMING DIAGRAM:

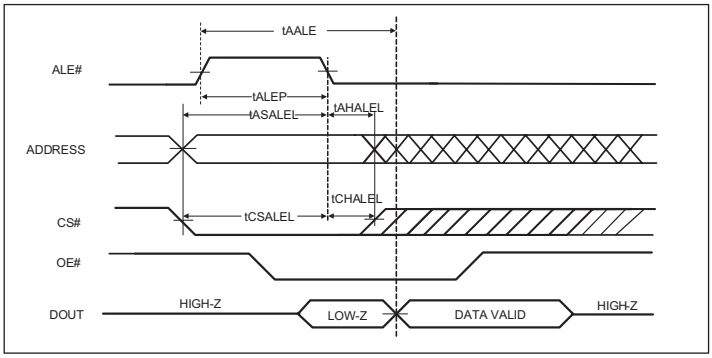
READ CYCLE NO. 1[1,2] (ADDRESS CONTROLLED , CS#, OE#, UB#, LB# = LOW, WE# = HIGH)




Notes:
1. Normal SRAM Operation when ALE# = HIGH
2. ERR1, ERR2 signals act like a Read Data Q during Read Operation.

## TIMING DIAGRAM:

READ CYCLE NO. 2 (ALE# AND OE# CONTROLLED, UB#, LB# = LOW, WE# = HIGH)




## TIMING DIAGRAM:

WRITE CYCLE NO. 1 (ALE# and WE# CONTROLLED, OE# = HIGH, UB#, LB# = LOW)