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Quality & Reliability Data

Section 1 - Introduction

The major influence, within Syfer Technology Limited, is to provide its Customers with 'World Class' capacitors.

Syfer has developed its own unique 'Wet Process' for the manufacture of Multilayer Ceramic Chip Capacitors. This has been in operation for some 30 years, significantly increasing the reliability levels obtained today, over those that were the expectation then.

Syfer's 'Wet Process' is based upon the principle of Screen Printing, both ceramic and electrode layers, in a single operation. This gives a more consistent deposition and greater accuracy of electrode alignment. In contrast to parts made by 'Tape Methods', it reduces stresses within the components.

At all manufacturing stages, well defined controls are in place. Statistical Process Control (SPC) techniques are used extensively to monitor and to reduce process variability.

Microsections are prepared from each batch of product built. Destructive Physical Analysis (DPA) is conducted on each microsection to verify structural integrity and the absence of voids, delaminations or other defects.

After the fabrication cycle, 100% testing is conducted for:

(1) Capacitance
(2) Dissipation Factor
(3) Insulation Resistance
(4) Voltage Proof

Syfer's Quality Control Function audits each process stage and the outgoing products, to ensure strict conformity to internal, customer, national and international specifications.

Syfer holds IECQ-CECC, TUV, UL, ISO9001, ISO14001 and OHSAS18001 approvals.

In addition to its advanced construction methods, and sophisticated Quality Controls, Syfer carries out regular long term accelerated tests on its products to prove their reliability.

The Capacitor Industry accepts that no single test, in isolation, is an effective measure of total reliability and, therefore, accelerated testing, directed at selected capacitor performance factors, is conducted, by Syfer, on a regular basis. This includes:

(1) 125°C Endurance Testing
at 1.5 times rated voltage

(2) 85°C/85% Relative Humidity Testing
at stress voltages of 1.5, 5 and 50 vdc

Syfer maintains its rigorous test regime, to give its customers useful and detailed data on the reliability of its products. There is a continuing trend toward higher value capacitors in all major dielectric categories as circuit designers have demanded even greater volumetric capacity. This has prompted an increase in the number of 'high' value lots tested; now approximately 20% of such parts are tested compared with 10% for standard product. The results presented here reflect this change in product mix.

Each section of this document describes the methodology of test and includes a summary of the results obtained. F.I.T. Rate Data is shown, based upon Endurance Test results.

The aim of this document is to confirm that Syfer continues to maintain its reputation for the manufacture of products that meet, and exceed, customer's expectations of reliability.

Syfer's Quality and Technical personnel are available to discuss this information, on request.

Section 2 - Test Conditions

Endurance

Duration	1000 Hours
Intermediate Check Time	168 Hours
Voltage	1.5 x Rated Voltage
Current Limitation	Each component stressed via a 100kΩ resistor
Temperature	C0G125°C
X7R125°C	
Post Test Limits	
Insulation Resistance C0G	≥ 4000MΩ or 40s
	X7R ≥ 2000MΩ or 50s (whichever is the less)

85°C / 85%RH

Duration	168 Hours
Voltage Bias	Rated voltage up to a maximum of 50 volts dc, however, when specified, 1.5Vdc or 5Vdc may be required
Current Limitation	Each component stressed via a 100kΩ resistor
Temperature	85°C
Relative Humidity	85%
Post Test Limits	
Insulation Resistance	C0G ≥ 4000MΩ or 40s
	X7R ≥ 2000MΩ or 50s (Whichever is the less)

Section 3 - F.I.T. Rate Data

Acceleration Factor Calculations

$$\text{Acceleration Factor (AF)} = AF_{voltage} \times AF_{temperature}$$

where

$$\text{Acceleration Factor}_{voltage} = \left[\frac{V_{stress}}{V_{use}}\right]^{2.7}$$

and

$$\text{Acceleration Factor}_{temperature} = e^{\left(\frac{E_a}{k}\left[\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right]\right)}$$

where E_a = Activation energy (1.0 eV for M.L.C's)
k = Boltzmann' Constant (8.617 x 10^{-5}eV/K)
T = Temperature in K (273 + Temperature in ^{o}C)

Failure Rates at the Specified Confidence Level (60%) are derived from:

$$FR = \frac{X^2}{2} \times \frac{1}{AF \times H}$$

where FR = Estimated Failure Rate at Use Stress
X^2 = Chi Square calculated for number of rejects at test stress
H = Component test hours

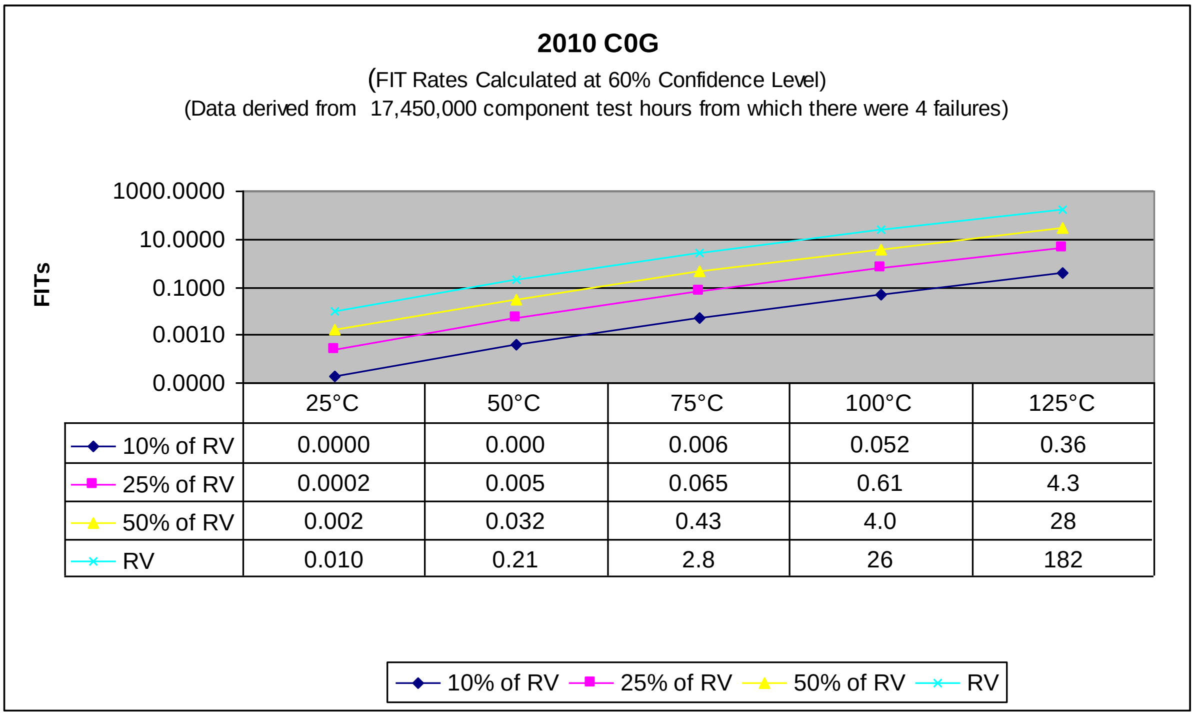
Conversion Factors

From	To	Operation
FITS	MTBF (Hours)	$10^9 \div$ FITS
FITS	MTBF (Years)	$10^9 \div$ (FITS $\times$ 8760)

C0G Capacitor Reliability Data

Product type:	C0G capacitors.
Time period analyzed:	1st January 2010 to 31st December 2010
Test laboratory:	Syfer Technology Reliability Test Department
Number tested:	17,450
Test conditions:	1000 hours with 1.5x rated voltage applied at 125°C
Results:	4 failures in 17,450,000 component test hours

FIT (Failure In Time) Rate Graph



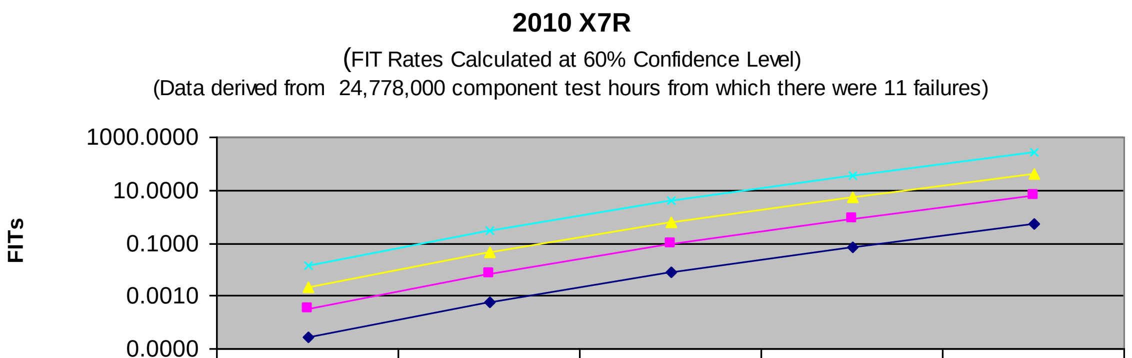
	25°C	50°C	75°C	100°C	125°C
10% of RV	0.0000	0.000	0.006	0.052	0.36
25% of RV	0.0002	0.005	0.065	0.61	4.3
50% of RV	0.002	0.032	0.43	4.0	28
RV	0.010	0.21	2.8	26	182

The FIT (Failure In Time) rate graph provides an indication of component reliability in relation to a customer's application with respect to temperature and voltage being applied. For example, at 25ºC and 50%RV (Rated Voltage), the FIT rate graph indicates 0.002 FITs. As a comparison, an automotive customer specifies maximum of 0.1 FITs at 25ºC and 50%RV (Rated Voltage).

X7R Capacitor Reliability Data

Product type:	X7R capacitors.
Time period analyzed:	1st January 2010 to 31st December 2010
Test laboratory:	Syfer Technology Reliability Test Department
Number tested:	24,778
Test conditions:	1000 hours with 1.5x rated voltage applied at 125°C
Results:	11 failures in 24,778,000 component test hours

FIT (Failure In Time) Rate Graph



	25°C	50°C	75°C	100°C	125°C
10% of RV	0.0000	0.001	0.008	0.071	0.50
25% of RV	0.0003	0.007	0.091	0.85	6.0
50% of RV	0.002	0.045	0.59	5.5	39
RV	0.014	0.29	3.8	36	252

The FIT (Failure In Time) rate graph provides an indication of component reliability in relation to a customer's application with respect to temperature and voltage being applied. For example, at 25ºC and 50%RV (Rated Voltage), the FIT rate graph indicates 0.002 FITs. As a comparison, an automotive customer specifies maximum of 0.1 FITs at 25ºC and 50%RV (Rated Voltage).