Analog Latch, One-Shot Circuits Operate with Close to Zero Power

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Getting serious about power consumption in small, battery-powered wake-up circuits means dropping the clunky old 555s and baling wire in favor of some modern low-voltage analog building blocks. Yes, these same functions can be jury-rigged from AUP logic gates, but the penalty will be high shoot-through supply currents as the gate input voltages hover around the threshold level. The circuits presented here are designed with slow-moving analog signals in mind and don't exhibit that problem.

The building block chosen for these designs is a multipurpose chip containing a reference and two gain blocks (op amp and latching comparator) from Touchstone Semiconductor. There are two versions, one having a push-pull output (TS12011) or open-drain output (TS12012) on the comparator.

Three of these four circuits (the three one-shots) take advantage of the way the comparator latch works. When the latch is enabled, the comparator monitors its input state, capturing and holding the high (TS12011) or low (TS12012) state when the inputs cross. This leads to some interesting design possibilities and, in this case, the ruthless elimination of external components.

All these circuits work at seriously low voltages. Although the datasheet specifies a minimum VDD for the ICs of 0.8V, and the max VGS(th) on the FETs is given as 1.1V, these circuits all continued to function well below half a volt when tested in the lab (albeit with degraded accuracy since the reference was dropping out). And when they finally failed, they did so gracefully, the outputs settling to a logic low, without unexpected supply currents or flailing output states.

A. An SR Latch with an Accurate Trip Point

The TS12012 comparator block can latch itself in the LOW state by feeding the output into the LHDET latch input. The super low-threshold Pch FET pulls up the latch input when it's time to reset it. The series resistor keeps the output from causing crowbar currents with the P-channel FET.

An internal reference generator provides the comparison voltage for the latch, keeping the error down to +/-5.7% over temp, which is much better than can be achieved with a logic gate, and not bad for a chip that draws just 1.1µA total (some of which is used to power an extra op amp gain block not needed in the design).

B. An Ultra-Simple One-Shot Timer

This inverting retriggerable one-shot circuit capitalizes on the fact that the latched condition of the TS12011 leaves the comparator output responsive to input signals, at least until the output goes high.

When the input TRIG signal goes high, the external FET turns on and discharges the timing cap. OUT is driven low, since the comparator is enabled and the capacitor voltage is less than VREF. When TRIG goes low again, the timing cap starts charging up; the comparator is nominally in

the latched state but with the output low, it's still looking for the inputs to cross. When the timing cap voltage hits VREF after a millisecond or so, the output latches in the high state and the timing cycle is done. “Look, Ma, (almost) no parts needed!”

C. A Non-Retriggerable One-Shot Timer

This circuit is similar to the simple inverting one-shot above, but uses a stacked-transistor AND gate to lock out the TRIG input from resetting the timing cap during the timing cycle. Like the previous circuit, the timer pull-up resistor R1 is tied to VDD, resulting in the time delay having strong VDD dependence. This may not be a problem at all, if VDD comes from an accurate source such as an LDO. Other solutions include gaining up the internal reference of the TS12011 using the on-board op amp to create a higher-voltage source, or adopting a ratiometric approach as shown in the following circuit.

D. A Ratiometric One-Shot Timer

This circuit differs from the previous in two respects: first, the output is non-inverted with respect to the trigger input (the TS12012 latches low rather than high), and second, the comparison voltage is generated by a resistor divider off of VDD instead of the internal reference. As a result, the comparison voltage tracks the changes in capacitor charging current caused by varying VDD. In this way, the one-shot time period is kept relatively constant despite variable battery voltages. One could easily apply this same trick to the inverting configuration as well.

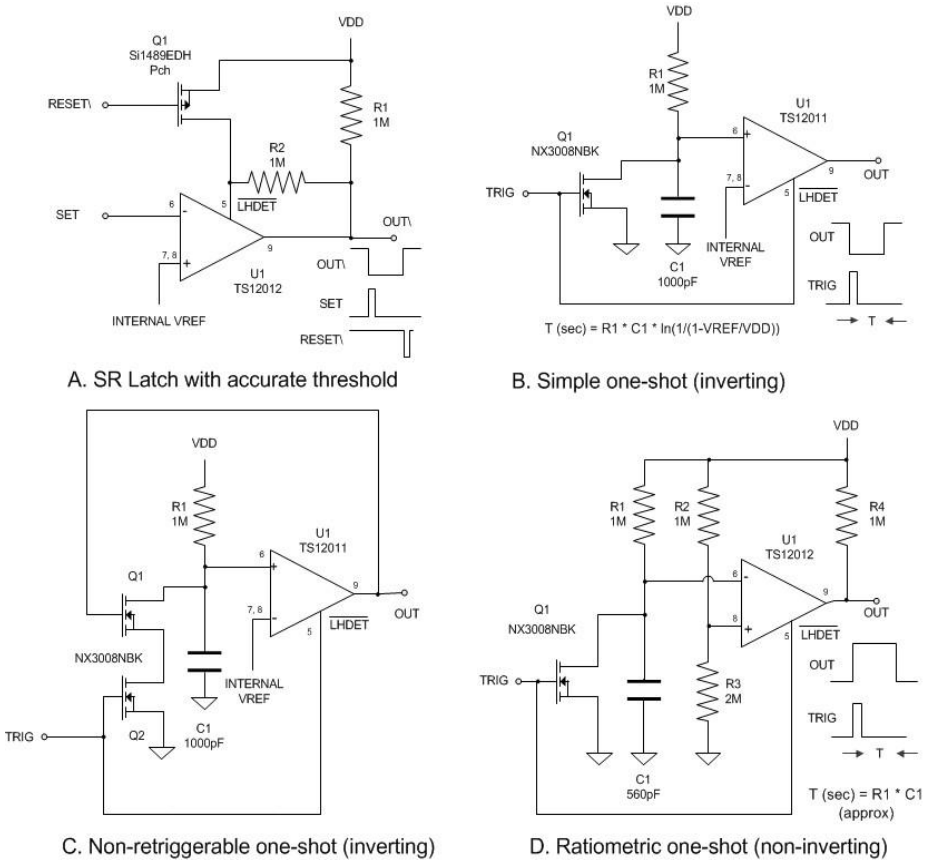

Figure 1. Low-power latch and timer circuits via analog building blocks

Summary

These four simple circuits show that peripheral functions populating the “ecology” of microcontroller-based systems needn’t be built from logic gates or legacy ICs requiring high supply currents or voltages. The TS12011 and TS12012 super-low-current, multi-function building blocks exhibit such low power consumption and low voltage operation that they can be liberally sprinkled onto a circuit board and stay “always on” without impacting battery life. Although simple, these examples point the way toward solving a wide range of design needs such as waveform generators, signal conditioners, and detectors.

For additional information, please visit the corresponding product pages:

- TS12011 Product Information
- TS12012 Product Information

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