Jitter Budget for 10 Gigabit Ethernet Applications with SiTime SiT9120/1 Oscillators

1 Introduction

The 10 Gigabit Ethernet (10GbE) specifications are defined in clauses 44 through 54 of the IEEE 802.3-2005 standard. It contains critical timing specifications governing electrical implementations such as 10GBASE-X4 as well as optical interfaces such as the 10GBASE-R. Although the standard specifies jitter limits for the transmitter and the receivers, it does not impose explicit restrictions on the interface reference clock.

This application note analyzes the impact on the system jitter budget when SiT9120/1 devices are used as the clock source. An analysis shows that SiT9102/1 MEMS-based oscillators perform better than most competing quartz based devices, providing more than 98% of the system jitter budget to be used by other system devices and interconnects for the 10BASE-X4 and 10GBASE-R interfaces.

2 10GBASE-X4 and 10GBASE-R

2.1 Jitter Specifications

The 10BASE-X4 and XAUI interfaces share the same jitter budget specifications. This section analyzes the jitter requirements of the electrical interface using the XAUI as the example.

The XAUI interface includes four serial lanes. For each lane, the transmitter typically includes a 8b/10b encoder and a serializer to convert a number of parallel data streams with an aggregate data rate of 2.5 Gb/s into a single differential lane with a baud rate of 3.125 Gbps. The receiver uses a clock/data recovery (CDR) circuit to extract clocking information from the data stream and uses it to sample the data. The impact of the clock source on the link performance is determined by the TX PLL and the RX CDR. According to clause 47 of the IEEE 802.3-2005 standard, the TX PLL is modeled as a second order PLL with a bandwidth of 20 MHz, while the CDR is modeled as a PLL with a corner frequency of 1.875 MHz. The combination of these two PLLs reduces the low frequency and the high frequency jitter components, leading to a band pass filter (BPF) jitter response. Therefore, the clock timing jitter impact can be estimated by passing the clock timing jitter or phase noise through the filter response shown in Figure 1.

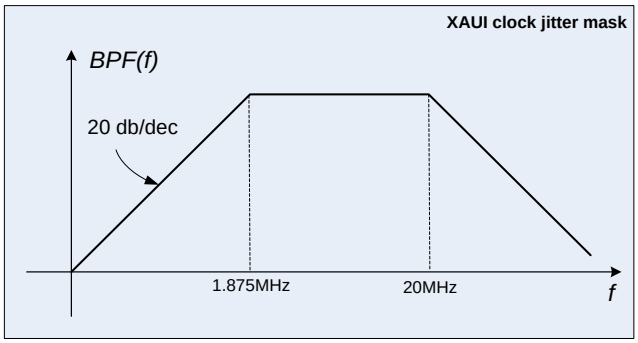

Figure 1. 10GBASE-X4 timing jitter mask

10GBASE-R, typically used for optical 10 GbE, uses 66b/64b encoding to transmit and receive data with a baud rate of 10.3125 Gbps. The reference clock used to clock the XAUI link may also be used to clock the 10 Gbps serial link. Because the 10 Gbps serial link also uses TX PLL and RX CDR circuits to send and recover data, a band-pass jitter filter similar to Figure 1 can be used to estimate the clock jitter impact, except that the lower frequency cutoff is 4 MHz instead of 1.875 MHz (IEEE 802.3-2005, clause 52). The timing jitter filter response is shown in Figure 2.

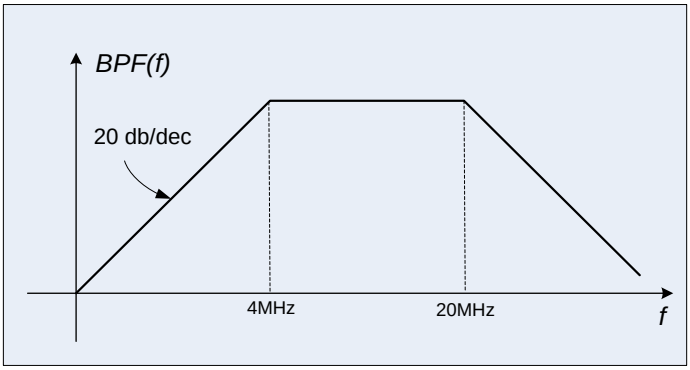

Figure 2. 10GBASE-R timing jitter mask

Table 1 shows the IEEE 802.3 standard transmitter jitter budget for 10GBASE-X4 and 10GBase-R.

Table 1: IEEE 802.3-2005 Jitter Budget

Serial Interface	Random Jitter (RJ)	
	RMS, ps	Pk-Pk, ps
10GBASE-X4	4.1	56
10GBase-R	1.55	21.75

2.2 Jitter Calculations for 10GBASE-X4 and 10GBase-R

To analyze the clock jitter impact, we examined random jitter (RJ) contributions from different elements of the 10GBASE-X4 link. The jitter sources in a 10GBASE-X4 transmitter are as follows.

1. Transmitter chipset driver
2. Reference clock (RefClk) source
3. Physical interface between the TX driver and the connector, including the driver termination components, the board traces and the connector

Jitters from the different sources can be represented by an overall RJ:

$$RJ_{RMS\_dev} = \sqrt{RJ_{RMS\_drvier}^{\ 2} + RJ_{RMS\_RefClk}^{\ 2}} \qquad \text{Equation 1}$$

where RJ_{PMS_dev}, RJ_{RMS_driver}, and RJ_{RMS_RefClk} are the RMS random jitters of the overall device, the driver, and the reference clock, respectively.

RMS RJ is calculated as the square root of the sum of squares (RSS) of the individual components due to the statistically independent random nature of the RJ components. It is important to note that the peak-to-peak values of the RJ components should not be summed directly to compute the overall RJ peak-to-peak value. Instead, the RMS value should be computed first using Equation 1, and then the peak-to-peak RJ can be calculated using the following equation.

$$RJ_{PP} = (14.07)RJ_{RMS} \quad \textit{for BER=10e-12} \qquad \text{Equation 2}$$

3 Phase Jitter Measurements

A high bandwidth low noise floor real-time digital oscilloscope, Agilent DSA91304A was used to measure the RJ of SiT9120/1 MEMS-based oscillators and five other LVPECL quartz oscillators, listed in Table-2, running at 156.25 MHz. The RJ for each oscillator was measured under the following 3 settings.

- Integrated from 12 kHz to 20 MHz without additional filter
- Integrated from 12 kHz to 20 MHz plus 1st order high pass filter (HPF) with 1.875 MHz corner frequency (see Figure 1)
- Integrated from 12 kHz to 20 MHz plus 1st order high pass filter (HPF) with 4 MHz corner frequency (see Figure 2)

Note that the 1.875 MHz corner frequency high pass filter is used to determine jitter margin for 10GBASE-X4 whereas the 4 MHz filter is used for 10GBASE-R applications.

The results of the RJ measurements with filters applicable to 10GBASE-R and 10GBASE-X4 are shown in Figure 3.

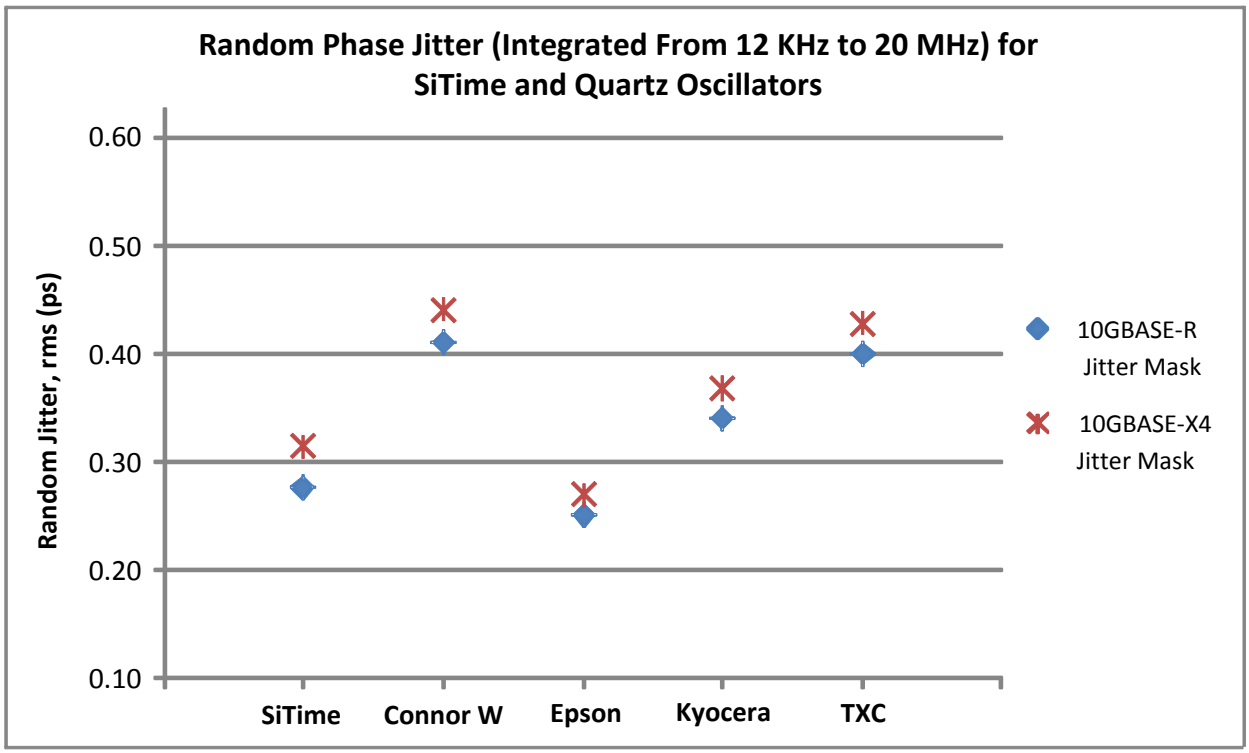

Figure 3: Measured RJ RMS for SiTime and quartz oscillators with 10GBASE-R (4 MHz) and 10GBASE-X4 (1.875 MHz) high pass filter (HPF)

4 Jitter Margin Estimations

Applying the analysis and equations stated in sec 2.2 to the phase jitter measurements and the jitter budget per the IEEE 802.3-2005 standard (Table 1), the jitter margins given in Table 2 are obtained.

Table 2: RJ Margin for 10GBE for SiTime and quartz oscillators

Vendor	Manufacturer Part Number	10GBASE-X4 %	10GBASE-R %
SiTime	SiT9121AC-1D2-33E156.250000	99.70	98.41
Connor Winfield	P123-156.25M	99.42	96.44
Epson	EG-2102CA 156.2500M-PHPAL3	99.78	98.69
Kyocera	KC7050T156.250P30E00	99.60	97.56
TXC	BB-156.250MBE-T	99.45	96.61

As listed in row 1 of Table 2, 99.7% (10GbASE-X4) and 98.41% (10GBASE-R) of total jitter in the system would be allocated to the Phy TX path and the transmission medium when using a

SiT9120/1 as a reference clock. This result shows that the SiT9120/1 oscillator meets the 10GbE interface clock jitter requirements with a high margin.

5 Conclusion

The reference clock impact on the serial interfaces within 10GbE systems can be determined by applying the appropriate filter mask to the clock phase noise. These masks typically have band-pass characteristics, as shown in Figures 1 and 2.

Analysis of system level jitter margins for 10GBE applications using SiT9120/1 clock devices shows that 99.7% (for 10GBASE-X4) and 98.41% (for 10GBASE-R) of the total jitter budget are available to the transmitter and transmission media. Such margins give designers a great deal of flexibility in choosing system components, making the SiT9120/1 devices an excellent choice as the clocking source for 10GbE implementations.

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