SiT9102 Jitter Performance for PCI-Express Applications

1 Introduction

Embedded clocking and common reference clocking are the primary clocking methods used in serial IO applications. PCI-Express, which is widely used in computing applications, can use both embedded or reference clocking. The latter is more common due to lower power consumption and cost of implementation. In this application note, we discuss the common reference clocking architecture and the clock jitter requirements for PCI-Express applications as defined by the PCI-Express specifications v1.1, v2.0, and v3.0. We report the jitter performance of the SiT9102 differential oscillator and show data indicating that the SiT9102 meets the requirements of all versions of PCI-Express.

2 Common Reference Clocking

In the reference clocking architecture shown in Figure 1, the reference clock (RefClk) is routed to both the transmitter and the receiver. The transmitter includes a PLL (TX PLL) to generate a high frequency signal for clocking out serial data. This TX PLL is modeled as a second order system with a given level of peaking on the frequency response. The receiver uses another PLL (RX PLL) to synthesize the correct data sampling clock frequency from the reference clock and employs one clock/data recovery (CDR) circuit for each lane of the data bus to align the locally synthesized clock edge with the center of the bit period of incoming data stream. The common reference clocking architecture replaces the CDR PLLs per lane on the receiver side with a single PLL for all lanes and one DLL per lane. This effectively reduces the receiver IC silicon area and power.

This architecture reduces the impact of phase noise spectrum of the clock signal at low frequency offsets, i.e. frequency range that falls in the pass-bands of the TX PLL and RX PLL, because such noise is common in the transmitter and receiver and is tracked closely by the receiver PLL. The dominant phase noise is concentrated in the region that falls in the pass-band of the TX PLL and in the stop-band of the receiver PLL. The phase noise that falls in stop-bands of both PLLs is also attenuated significantly. The resulting jitter filter responses are defined in the PCI-Express specification documents [1-4].

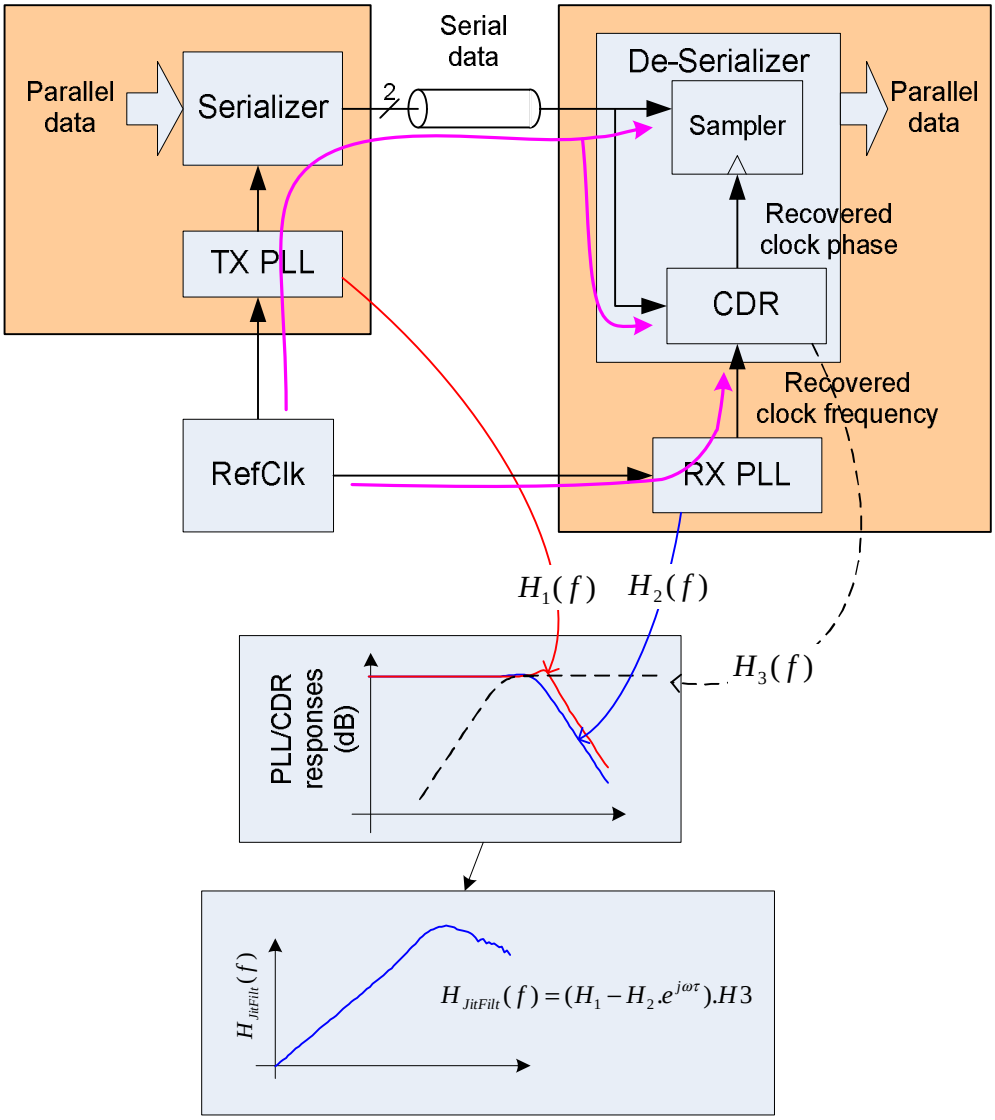

Figure 1: Reference clocking for serial IOs

3 SiTime Oscillator Jitter Performance for Reference Clocking

The SiTime SiT9102 differential oscillator supports the HCSL output signaling required for the reference clock in PCI-Express applications. In this section, we report the jitter performance of this device as specified in the PCI-Express specifications v1.1 [1] , v2.0 [2, 3], and v3.0 [4].

An Agilent DSA90604A oscilloscope with an N5380A SMA probe adaptor and a 1169A 12 GHz active probe is used to capture the clock waveform. The waveform data are processed by the PCI-SIG clock analysis tool version 1.5, and the results are listed in Table 1 and Table 2 for PCI-Express v1.1 and v2.0 specifications, respectively. The RefClk jitter filters specified in PCI-Express v3.0 specifications are applied to the phase noise of the oscillator signal to compute RefClk jitter for PCI-Express Gen3. The results are listed in Table 3. The data clearly show that SiT9102 meets all the jitter requirements for PCI-Express Gen1, Gen2, and Gen3 applications.

Table 1: SiT9102 phase jitter for PCI Express revision v1.1

Jitter filter response	Pk-to-pk phase jitter (ps)	
	SiT9102	**Maximum specification (ps)**
V1.1 (1.5 MHz to 22 MHz)	30	84

Table 2: SiT9102 phase jitter for PCI Express revision v2.0

Jitter filter response	Max. high frequency jitter (ps rms)		Max. low frequency jitter (ps rms)	
	SiT9102	**Max. specification (ps)**	**SiT9102**	**Max. specification (ps)**
5 MHz PLL with 1.5 MHz and first order data recovery DLL	2.1	3.1	1	3.0
5 MHz PLL with 1.5 MHz zero order data recovery DLL	2.1	3.1	0.8	3.0
8 MHz PLL with 1.5 MHz first order data recovery DLL	2.1	3.1	0.7	3.0
8 MHz PLL with 1.5 MHz zero order data recovery DLL	2.1	3.1	0.5	3.0

Table 3: SiT9102 phase jitter for PCI Express revision v3.0

PCI-E Gen3 Jitter Filter						SiT9102 random phase jitter after filter (ps rms)	Common REFCLK architecture random jitter limit (ps rms)
TX PLL		RX PLL		CDR	REF CLK path delay delta (ns)		
3dB HP BW (MHz)	Peaking (dB)	3dB HP BW (MHz)	Peaking (dB)	3dB LP BW (MHz)			
2	0.01	2	0.01	10	12	0.052	1.0
2	0.01	2	1.00	10	-12	0.052	
2	0.01	5	0.01	10	12	0.060	
2	0.01	5	1.00	10	-12	0.068	
2	0.01	2	0.01	10	12	0.142	
2	0.01	2	1.00	10	-12	0.106	
2	0.01	5	0.01	10	12	0.137	
2	0.01	5	1.00	10	-12	0.111	
2	2.00	2	0.01	10	12	0.089	
2	2.00	2	1.00	10	-12	0.081	
2	2.00	5	0.01	10	12	0.057	
2	2.00	5	1.00	10	-12	0.055	
2	2.00	2	0.01	10	12	0.165	
2	2.00	2	1.00	10	-12	0.131	
2	2.00	5	0.01	10	12	0.154	
2	2.00	5	1.00	10	-12	0.122	
4	0.01	2	0.01	10	12	0.086	
4	0.01	2	1.00	10	-12	0.115	
4	0.01	5	0.01	10	12	0.096	
4	0.01	5	1.00	10	-12	0.127	
4	0.01	2	0.01	10	12	0.120	
4	0.01	2	1.00	10	-12	0.102	
4	0.01	5	0.01	10	12	0.106	
4	0.01	5	1.00	10	-12	0.110	
4	2.00	2	0.01	10	12	0.099	
4	2.00	2	1.00	10	-12	0.111	
4	2.00	5	0.01	10	12	0.098	
4	2.00	5	1.00	10	-12	0.119	
4	2.00	2	0.01	10	12	0.140	
4	2.00	2	1.00	10	-12	0.095	
4	2.00	5	0.01	10	12	0.115	
4	2.00	5	1.00	10	-12	0.083	

4 References

[1] PCI-SIG, “PCI-Express Base Specification Revision 1.1”

[2] PCI-SIG, “PCI-Express Base Specification Revision 2.0”, December 20, 2006

[3] PCI-SIG, “PCI-Express Card Electromechanical Specification Revision 2.0”, April 11, 2007

[4] PCI-SIG, “PCI Express Base Specification Revision 3.0”, November 10, 2010

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