

MEMS Timing-Keeper Extends Standby Life of Mobile Devices

With increasingly sophisticated Smartphones and mobile devices offering more features and un-tethered instant access to data, news and entertainment, consumers are spending more time using their devices. Users are demanding faster connectivity, multi-core GHz+ application processors and HD resolution touch screens, while at the same time, expecting to last longer on a single battery charge. Mobile device designers must carefully consider how to meet the conflicting demands of extending battery life while supporting faster, more power-hungry processors and LCD screens. Design options typically fall into two main categories: 1. reduce overall power consumption, or 2. increase battery capacity.

Battery and display technologies have not kept up with the exponential progress in semiconductor design and processes over the last decade. With the space and weight constraints of MIDs, only incremental increases in battery capacity are possible using current battery technologies. Designers are left to employ creative ways to reduce overall power consumption.

One technique to reduce power consumption is to shut down the functional blocks with the highest current drain and switch to the lowest power suspend/sleep state when devices are inactive. However, during the low power state, the always-ON clocks continue to draw battery power. New MEMS-based time-keeping solutions offer unique power saving strategies with programmable output frequencies and output drive swing levels. Drawing a mere 750 nA core current, these timing devices can run off of an unregulated Li-Ion or regulated power, thus bringing more options to mobile device designers.

Mobile Device Power Management Overview

The basic architecture of a mobile wireless device is shown in Figure 1. Depending on the implementation of the mobile device architecture, the power management function is distributed across the application and RF baseband processors and/or a dedicated PMIC (power management IC). Given their size constraints and performance demands, these blocks are implemented in CMOS sub-micron technology.

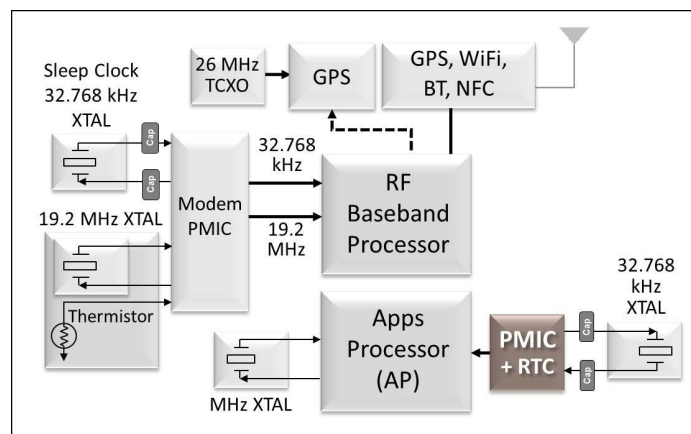


Figure 1: Block diagram showing high-level architecture of a smart phone

Power dissipation in a CMOS SoC (system on chip) can be quantified by the following formula:

$$P = C \cdot V^2 \cdot F \quad (1)$$

Where; P is the power in watts; V is the DC voltage of the individual power rail (VDD) of the SoC ; C is the intrinsic capacitance hanging off the VDD power bus. The complex blocks implemented inside each SoC are powered from multiple VDD rails ranging in values from 1.0V to 4.3V.

The basic power management function is implemented as:

- Monitor system processing load
- Switch the system between one of the following states:
 - Active
 - Suspend
 - Sleep

Active State

Power consumption can be optimized during the active state by using a technique called dynamic voltage and frequency scaling (DVFS). From equation (1), power dissipation is reduced as the square of the lower VDD rail voltage. Likewise, depending on the process node deployed in the fabrication of the SoC, the operating frequency is throttled down to linearly scale back the power dissipation.

The application processor (AP) and RF baseband processor are the main processing units and consume the highest amount of battery power. These processing SoCs achieve the highest efficiency possible by communicating commands with the PMIC or the on-chip power-management module to control the DVFS functionality. The basic functional block of a PMIC is shown in Figure 2. The PMIC function can be implemented as a stand-alone chip or can be distributed as embedded blocks within the processing units in a mobile phone.

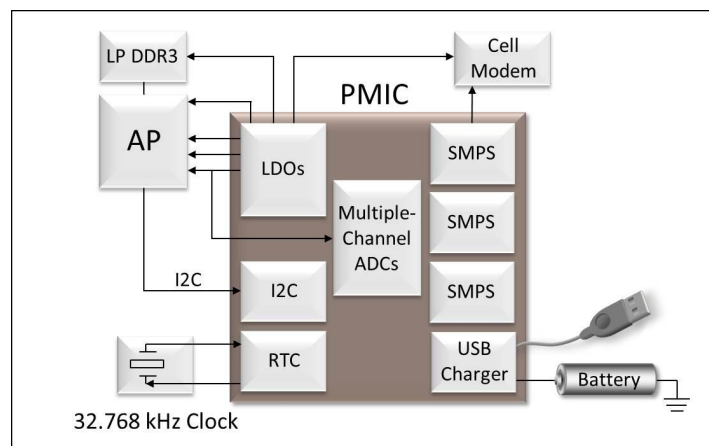


Figure 2: Figure-2: Functional block diagram of a PMIC

The processing modules/SoCs communicate system status to the PMIC over an I2C bus or similar bus such as a SM bus. The PMIC LDO and SMPS blocks provide programmable regulated voltages required by the system power needs.

Suspend State

The suspend state is entered when a mobile device is inactive for a pre-determined (user configured) time or when initiated by the user:

- No user interface interaction with touch screen or buttons
- No incoming phone calls or data communication
- User pushed power/suspend key to force suspend state

In this state the main processing unit(s) operate at the lowest permissible VDD core voltage and clock frequency down to zero hertz. The LCD screen is shut off and the touch sensor wakes up every hundred milliseconds to detect user touch interaction. Communication peripherals such as cell modems are in their lowest power state which can be interrupted by an external event. The PMIC running off a 32.768 kHz clock source is the only device that is fully active in this low power state. One of the functions of the 32 kHz clock is to serve as a timer to wake up the peripheral devices at pre-determined times as dictated by the wireless LAN requirements or the power management scheme.

In suspend state the system power dissipation is due to:

- Leakage current of the main processing SoCs
- Suspended state power dissipation of peripherals (touch screen, WiFi RF front-end, etc.)
- Power dissipation of the PMIC running off the 32 kHz clock

The major contributors to the overall power budget in suspend state is the power consumption of the PMIC, 32 kHz crystal oscillator, the RTC block and wireless LAN connectivity.

Sleep State

This is the lowest power state. All devices are shut down except for the monitoring circuitry clocked by the 32 kHz device in the PMIC and the real-time clock (RTC) block.

To extend the standby life of the battery, creative strategies must be deployed to shave off micro-watts of power from the active blocks in the suspend and sleep states. Regardless of the power state, the 32 kHz oscillator is always ON to clock power, battery management blocks and wireless LAN. In suspend state, the current draw is typically in the micro-amps. Lithium-chemistry batteries lose more battery capacity during long periods of low-current drain typical of suspend/sleep state scenarios compared to short bursts of peak current during the active state.

Mobile Device Clocking Schemes

A typical mobile device, depending on the choice of the applications processor, partitioning and other functions it supports, can contain several timing devices including one or more 32 kHz clocks as shown in Figure 2. The power consumed by a 32 kHz oscillator is usually 2 to 3 micro-watts with a typical current draw of 1 to 2 uA from a 3V DC regulated power supply. The power consumed by the 32 kHz oscillator circuit, whether it is part of the PMIC crystal oscillator or an external oscillator feeding on the XIN pin of the PMIC, plays a significant role in the longevity of battery life during the suspend/sleep states. The SiT15xx family is a new generation of silicon MEMS 32 kHz oscillators from SiTime that offer a power-saving alternative to traditional on-chip oscillators, external quartz oscillators or quartz crystals (XTALs).

In mobile devices, the 32.768 kHz XTALs can be replaced with SiT15xx oscillators to further lower power consumption. These MEMS oscillators have a low power output with 750nA core supply current (typical). The SiT15xx have additional power savings features such as operation down to 1.2V, programmable frequency down to 1 Hz and programmable output swing.

Programmable Frequency

MEMS-based oscillators are based on a programmable architecture that allows customization of features including frequency and supply voltage. These programmable features can be used to optimize system design including lowering power consumption. For example, the frequency of SiT15xx MEMS oscillators is programmable from 1 Hz to 32.768 kHz in powers of two. Reducing the frequency significantly reduces the output load current ($C \cdot V \cdot F$). As an example, reducing the frequency from 32.768 kHz to 10 kHz improves load current by 70%. Similarly, reducing the output frequency from 32.768 kHz down to 1Hz reduces the load current by more than 99%. (See examples below.) Quartz XTALs, due to the physical size limitations of the resonator at low frequencies, cannot offer frequencies lower than 32.768 kHz.

Programmable Output

Another new power saving feature available with the latest generation of MEMS-based oscillators is NanoDrive™, a programmable output swing. This feature allows the output swing to be programmed to a lower voltage swing and match the PMIC/chipset as shown in Figure 3. This programmable output stage minimizes power and maintains compatibility with the downstream oscillator input. The output swing is programmable from full swing down to 200 mV, to consume up to 40% less power than full swing LVCMOS.

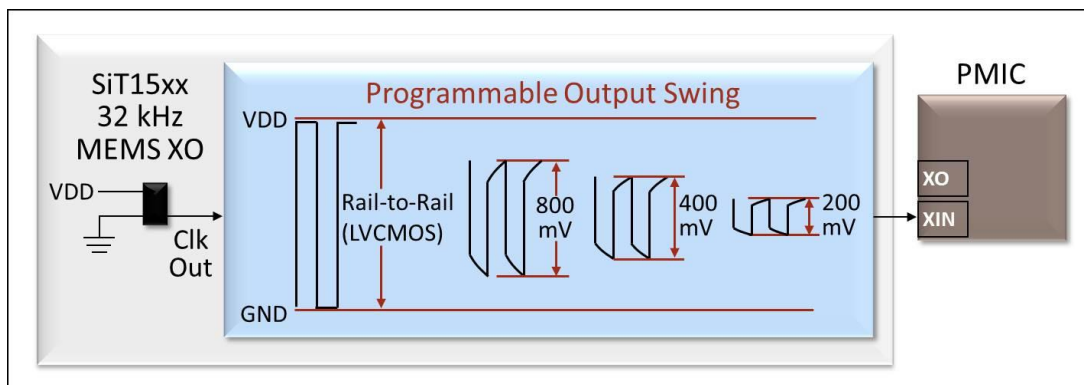


Figure 3: NanoDrive™ output swing is programmable down to 200 mV to minimize power

Lowering Frequency and Output Swing to Reduce Current Consumption

The following examples illustrate how reducing the output swing and frequency impact current consumption.

No Load Supply Current – When calculating no-load power for SiT15xx devices, the core and output driver components need to be added. Since the output voltage swing can be programmed for reduced swing between 200 mV and 800 mV, the output driver current is variable. Therefore, no-load operating supply current is broken into two sections, core and output driver. The examples below illustrate the low-power benefits of reducing swing output. For example, no load current is improved by over 20% when compared to an LVCMOS (2.1V) swing.

The equation is as follows:

Total Supply Current (no load) = Idd Core + Idd Output Stage

Where,

- Idd Core = 750nA
- Idd Output Stage = (165nA/V)(Voutpp)
- For NanoDrive reduced swing, select the output voltage swing, or VOH/VOL

Example 1: Full-swing LVCMOS

- Vdd = 3.3V (Avg)
 - Voutpp = 2.1V (max output of device)
 - Idd Core = 750nA
 - Idd Output Stage = (165nA/V)(2.1V) = 347nA
- No Load Supply Current = 750nA + 347nA = 1097nA

Example 2: NanoDrive™ Reduced Swing

- Vdd = 3.3V (Avg)
 - NanoDrive Output Selection:
 - Voutpp = VOH – VOL = 0.6V
 - Where, VOH = 1.1V, VOL = 0.5V
 - Idd Core = 750nA
 - Idd Output Stage = (165nA/V)(0.6V) = 100nA
- No Load Supply Current with NanoDrive = 750nA + 100nA = 850nA

Total Supply Current with Load – To calculate the total supply current, including the load, follow the equation listed below. The additional load current comes from a combination of the load capacitance, output voltage, and frequency (C*V*F). Since the SiT15xx includes NanoDrive reduced swing output and a selectable output frequency down to 1 Hz, these two variables will significantly improve load current.

The benefits of NanoDrive really become significant when the load current is considered. Power is reduced by greater than 40% with NanoDrive as shown in Example 4. Reducing the output clock frequency reduces the load current significantly as shown in Example 5.

Total Current = Idd Core + Idd Output Driver + Load Current

Where,

- Idd Core = 750nA
- Idd Output Stage = (165nA/V)(Voutpp)
- Idd Load = CLoad * Vout * Frequency
- Assume load capacitance is 10p

Example 3: Full-swing LVCMOS

- Vdd = 3.0V (Avg)
- Voutpp = 2.1V (max output swing for this device)
- Idd Core = 750nA
- Idd Output Driver: $(165\text{nA/V})(2.1\text{V}) = 347\text{nA}$
- Load Current: $(10\text{pF})(2.1\text{V})(32.768\text{kHz}) = 688\text{nA}$
- Total Current with Load = $750\text{nA} + 347\text{nA} + 688\text{nA} = \underline{1785\text{nA}}$

Example 4: NanoDrive™ Reduced Swing

- Vdd = 3.0V (Avg)
- NanoDrive Output Selection:
- Voutpp = VOH – VOL = 0.5V
- Where, VOH = 1.1V, VOL = 0.6V
- Idd Core = 750nA
- Idd Output Stage = $(165\text{nA/V})(0.5\text{V}) = 83\text{nA}$
- Load Current: $(10\text{pF})(0.5\text{V})(32.768\text{kHz}) = 164\text{nA}$
- Total Current with Load = $750\text{nA} + 83\text{nA} + 164\text{nA} = \underline{997\text{nA}}$

Example 5: NanoDrive™ Reduced Swing and 1Hz Output Frequency

- Same conditions as above example 2, but with output frequency = 1Hz. This will significantly reduce the current consumption from the output stage and the load.
- Idd Core = 750nA
- Idd Output Stage = $(5.04\text{pA/V})(0.5\text{V})(1\text{Hz}) = 2.52\text{pA}$
- 1Hz Output Frequency impacts the load current as shown below:
Load Current = CVF = $(10\text{pF})(0.5\text{V})(1\text{Hz}) = 5\text{pA}$
- Total Supply Current with Load = Core Current + Output Stage Current + Load Current = $750\text{nA} + 0.00252\text{nA} + 0.005\text{nA} = \underline{750\text{nA}}$

Summary

The battery in a mobile device loses more capacity during long suspend/sleep states than during its active state. The major contributors to battery drain in low power states are the power and battery management circuits clocked by a 32 kHz time-keeping oscillator. The best solution for conserving battery capacity during suspend/sleep states is to leverage power saving schemes offered by new micro-power consuming programmable 1 Hz to 32 kHz silicon MEMS oscillators. By programming the frequency and output voltage of this new class of oscillator, current consumption can be significantly lowered depending on the specific power management implementation in the mobile device.