Selection of MOSFETs for DC/DC Synchronous Buck Controllers: SiP12201 Single 10 A Controller and SiP12203 Triple Step Down Controller IC for 2 Synchronous and 1 Linear Power Rail

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This application note is intended to help designers select the best MOSFETs to use with the SiP12201 and SiP12203 synchronous buck dc-to-dc controller ICs.

The SiP12201 is a single 10 A controller (fig. 1a). The SiP12203 is a triple step down controller IC for 2 synchronous and 1 linear power rail (fig. 1b). Both a have an input voltage range of 4.2 V to 26 V, an output voltage range of 0.6 V to 20 V, and a 500 kHz fixed switching frequency. The dead time and MOSFET driving capabilities of both ICs are similar as well. Thus the choice of MOSFETs for a particular dc-to-dc conversion application will be similar for each IC.

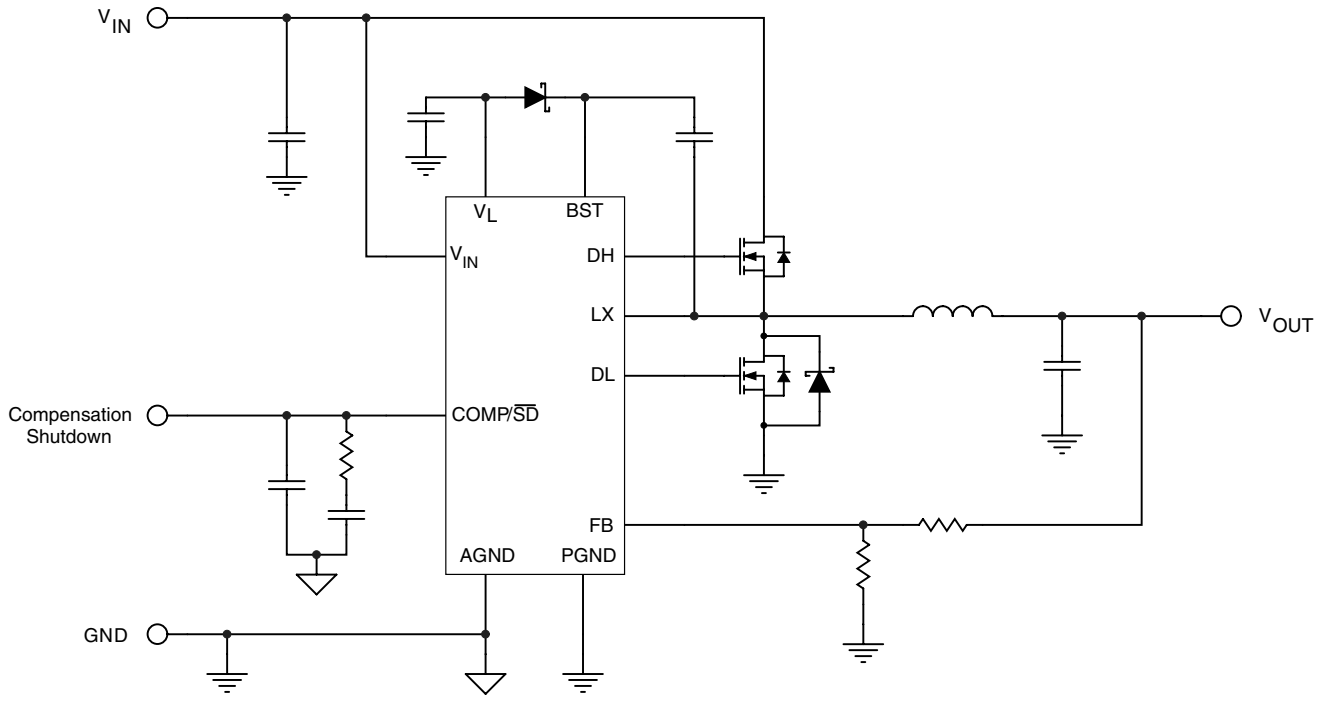

Fig. 1a

Selection of MOSFETs for DC/DC Synchronous Buck Controllers: SiP12201 Single 10 A Controller and SiP12203 Triple Step Down Controller IC for 2 Synchronous and 1 Linear Power Rail

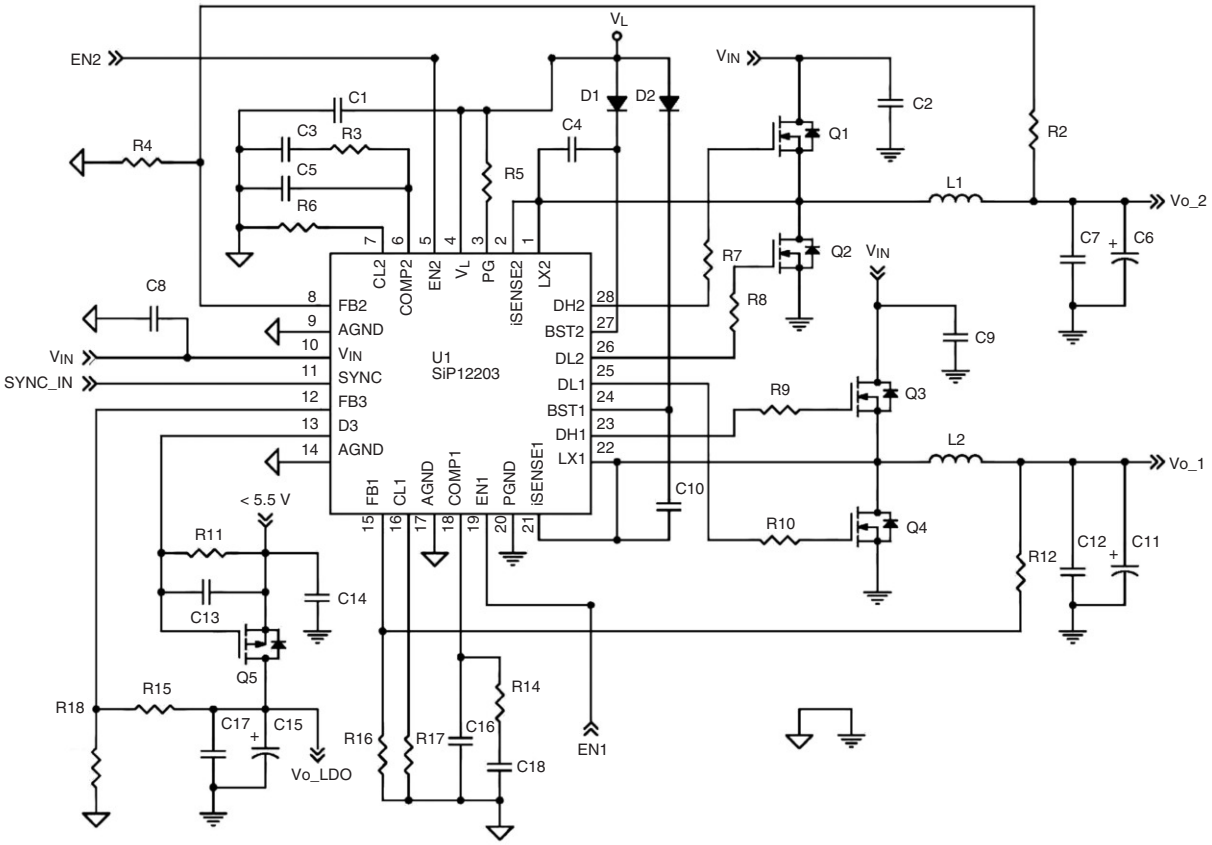

Fig. 1b

For the most efficient solution (duty cycle (δ) < 0.5), the high-side MOSFET would have the lowest Q_g and Q_{gd} rating (for the lowest VI power losses) and the low-side MOSFET would have the lowest $R_{DS(on)}$ and Q_{rr} rating (for the lowest I^2R losses). When the duty cycle is 0.5 then the $R_{DS(on)}$ and Q_g values would be the same. However, this is not always practical, and the selection of high- and low-side MOSFETs thus depends on five key factors - input voltage, efficiency, size, output current, and cost. **AN607** and **AN608** covers gate losses and the switching characteristics of MOSFETs extensively.

1. **Input voltage** - this determines the max. V_{DS} of MOSFET needed.
   5 V input - V_{DS} = 12 V or 20 V needed
   12 V input - V_{DS} = 20 V, 25 V, or 30 V needed etc…..
2. **Efficiency** - switching loses VI losses (Q_{gd}) and conduction losses I^2R losses ($R_{DS(on)}$). This is covered comprehensively in Vishay's application note **AN607**.
3. **Size** - this depends on the current output, duty cycle and thermal properties of the MOSFET ($R_{th(j-c)}$) and pcb board ($R_{th(c-a)}$).
4. **Output current** - this determines the package and $R_{DS(on)}$ needed and is covered below in "Choosing the Correct MOSFET" below.
5. **Cost** - this depends on the package, die size, and production volume.

CHOOSING THE CORRECT MOSFETS

Once the MOSFET V_{DS} is chosen from the input voltage range, there is now a huge range of MOSFETs to choose from. To narrow the choice, follow these steps, each of which is described in further detail below:

1. Calculate the current requirement of the high- and low-side MOSFET. This will give an idea of smallest package needed.
2. Consider and calculate the thermal values from junction to ambient.
3. Calculate the maximum $R_{DS(on)}$ for the MOSFET at the required V_{GS}, for the current handling required.
4. Considering Q_g, Q_{gs}, Q_{gd} ratings for the high side MOSFET Q1.

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5. Determine requirements for shoot-through immunity.
6. Choose a device that improves efficiency at higher switching frequencies and light loads.

1. Calculating the Current Requirement of the MOSFET: High Side (Q1) and Low Side (Q2)

Consider 12 V is converted to 3 V out at 10 A.

A. Calculating the Duty Cycle:

$V_{OUT} = V_{IN} \times t_{(on)}/T = V_{IN}\ \delta$

e.g. a 12 V input with 3 V output would have a $\delta = 0.25$

B. Calculating the Current Requirement of the MOSFET:

High-side (controlling MOSFET) Q1 RMS current requirement = $Io\sqrt{\delta}$
e.g. RMS current = 10 A x $\sqrt{0.25}$ = **5 A**

Low-side (freewheel MOSFET) Q2 RMS current requirement = $Io\sqrt{1-\delta}$
e.g. RMS current = 10A x $\sqrt{1 - 0.25}$ = **8.66 A**

From this we can see that the smaller the duty cycle, the less RMS current the high-side MOSFET and the more the low-side MOSFET needs to handle.

The RMS current requirement will give you an idea of the package needed. The following specifications are package limited:

60 A = PowerPAK® SO-8 and PolarPAK®50 A = PowerPAK 1212-8

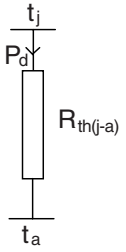
12 A = PowerPAK ChipFET®

2. Consider and Calculate the Thermal Values from Junction To Ambient

Junction to ambient thermal rating ($R_{th(j-a)}$) is the sum of the thermal rating junction to case ($R_{th(j-c)}$ and case to ambient ($R_{th(c-a)}$). $R_{th(j-c)}$ can be found on the MOSFET datasheet. This rating is fixed. However, the $R_{th(c-a)}$ depends on the pcb and amount of copper used. The lower the $R_{th(j-a)}$, the more current and more power dissipation the MOSFET can handle.*

*The only figures that are "arbitrary" are when manufacturers use different $R_{th(j-a)}$ for calculations. Although nominally based on the data sheet on a 1" copper PCB variation in this value is often seen. The only true thermal (R_{th}) figurers to compare different MOSFETs is the junction to case rating ($R_{th(j-c)}$).

$$P_d = \frac{t_j - t_a}{R_{th(j-a)}}$$



3. Calculating the Max. $R_{DS(on)}$ at the required V_{GS}

The choice of $R_{DS(on)}$ value will depend on your requirements for efficiency, cost, and size. The lower the $R_{DS(on)}$, the higher the cost of the MOSFET, but the more efficient the dc-to-dc conversion. The bigger the package, the bigger the die which can fit into the package and therefore the bigger packages have the lowest $R_{DS(on)}$ ratings.

We first need to calculate the highest $R_{DS(on)}$ for the application and consider that a lower $R_{DS(on)}$ will offer a more efficient solution.

$$R_{DS(on)}\ \text{max.} = \frac{t_j - t_a}{I^2\ \text{max.} \times RK \times R_{th(j-a)} \times \delta\ K\ \text{(duty cycle constant)}}$$

For a rough $R_{DS(on)}$ this calculation can be used:

$$R_{DS(on)}\ \text{max.} = \frac{t_j - t_a}{I^2\ \text{max.} \times 1.7 \times R_{th(j-a)}}$$

A. T_{amb} = ambient temperature (usually 25 °C for calculation)

B. RK = increase in $R_{DS(on)}$ factor with respect to temperature (normally 1.6 to 1.8) (fig. 2).

C. $R_{th(j-a)}$ = thermal impedance junction to ambient for the MOSFET - controlled by package type and pcb ($R_{th(c-a)}$).

There is a typical $R_{th(j-a)}$ depending on the package preferred (fig. 3). Vishay recommends using the max. $R_{th(j-a)}$ steady-state, to allow a safety margin.

D. Max. junction temperature of the MOSFET (normally 150 °C).

E. δ K = normal thermal impedance duty cycle constant depending on pulse duration (fig. 4).

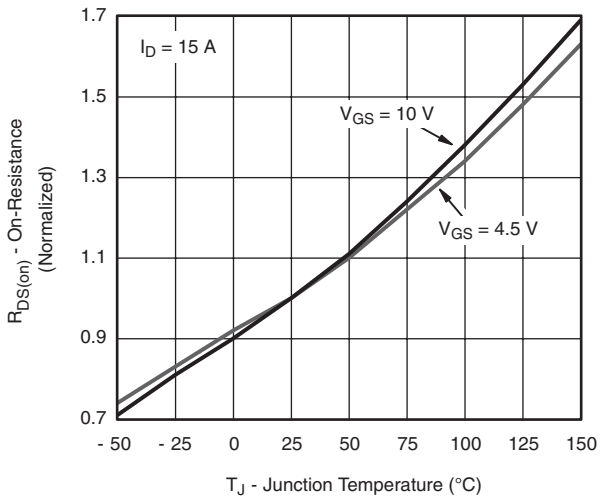


Fig. 2

APPLICATION NOTE

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THERMAL RESISTANCE RATINGS					
PARAMETER		**SYMBOL**	**TYPICAL**	**MAXIMUM**	**UNIT**
Maximum Junction-to-Ambient	$t \leq 10$ s	R_{thJA}	19	24	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.2	1.8	

Fig. 3

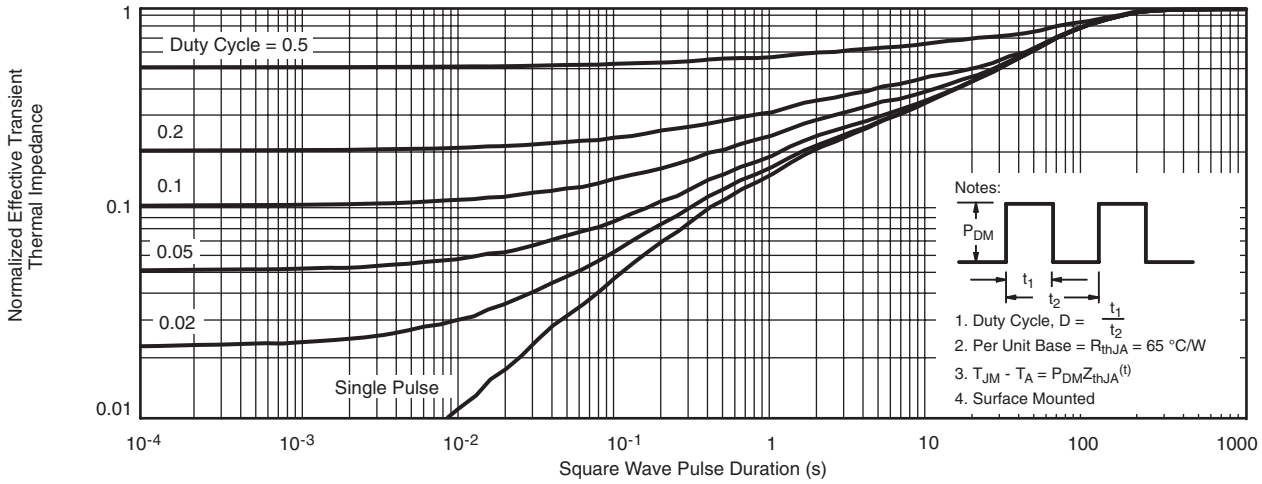

Fig. 4

Considering 12 V is converted to 3 V out at 10 A (50 °C ambient) and the low-side (freewheel MOSFET) RMS current requirement is 8.66 A

$$R_{DS(on)}\ \text{max.} = \frac{150 - 50}{75 \times 1.7 \times 24}$$

$R_{DS(on)}$ max. = 32.7 mΩ

4. Using Gate Charge to Determine Switching Time

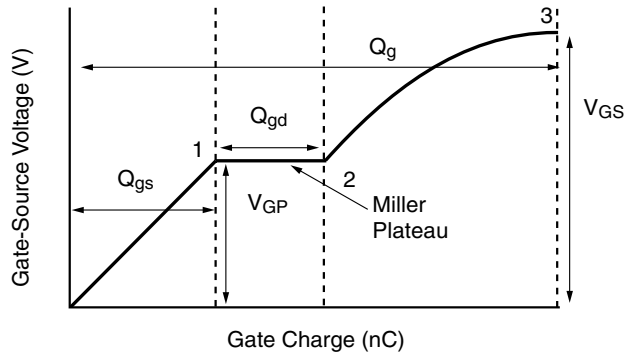

Fig. 5

Looking at the gate charge waveform in fig. 5, Q_{gs} is defined as the charge from the origin, to the start of the Millar Plateau V_{GP}. Q_{gd} is defined as the charge from VGP to the end of the plateau. Q_g is defined from the origin, to the point on the curve at which the driving voltage equals the actual gate voltage of the device.

The rise in V_{GS} during t_2 (fig. 5) is brought about by charging C_{gs} and C_{gd}. During this time V_{DS} does not change and as such C_{gd} and C_{gs} stay relatively constant, since they vary as a function of V_{DS}. At this time C_{gs} is generally larger than C_{gd} and therefore the majority of the drive current flows into C_{ds} rather than into C_{gd}. This current through C_{gd} and C_{ds} depends on the time derivative of the product of the capacitance and its voltage. The gate charge can therefore be assumed to be Q_{gs}.

The next part of the waveform is the Miller Plateau. It is generally accepted that the point at which the gate charge figure goes into the plateau region coincides with the peak value of the peak current. However, the knee in the gate charge depends on the product of $C_{gd}V_{gd} = Q_{gd}$, with respect to time. This means that there is a very small value of drain current and a large value of output impedance; thus the I_{DS} can actually reach its maximum value after the knee occurs.

Once the plateau is finished (when V_{DS} reaches its on-state value), C_{gd} becomes constant again and the bulk of the

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current flows into C_{gs} again. The gradient is not as steep as it was in the first period (t_2), because C_{gd} is much larger and closer in magnitude to that of C_{gs}.

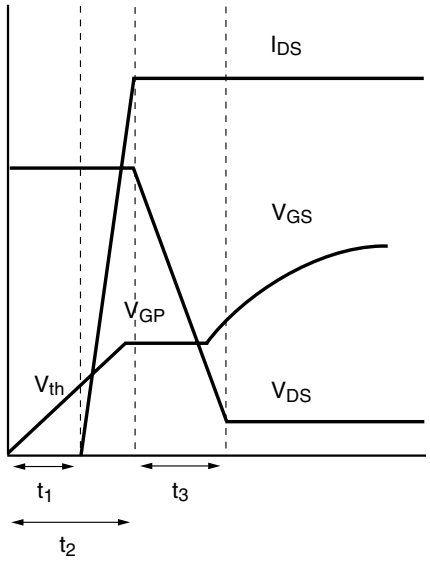

Fig. 6

5. Shoot-Through Immunity

The lower the Q_{gd}/Q_{gs} ratio in the low-side MOSFET, the more robust the synchronous buck will be to dV/dt shoot-through. A ratio of < 1 is a good indicator.

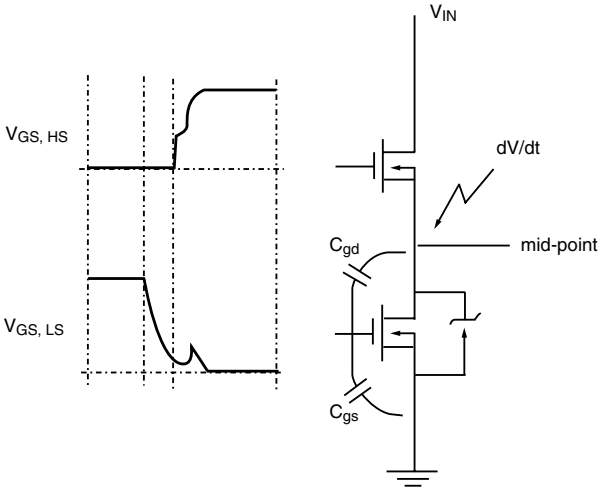

Fig. 7

6. Improving Efficiency at Higher Switching Frequencies and Light Loads

There is a demand for higher efficiency in point-of-load (POL) converters, especially at higher switching frequencies and light loads. One solution is to use a low-side MOSFET in parallel with a Schottky diode. This allows the current to flow through the diode before the low-side MOSFET turns on, reducing the losses of the body drain diode (bdd) in the MOSFET.

Vishay's SkyFET® Power MOSFETs combine the MOSFET and Schottky in one monolithic die, with two major benefits over two-component (MOSFET and Schottky) solutions. First, the power losses associated with the reverse-recovery current in the low-side MOSFET are defined as $V_{IN} \times Q_{rr} \times fsw$. Therefore a reduction in Q_{rr} (reverse recovery charge) reduces the power losses, proportional to the switching frequency. The Q_{rr} of Vishay Siliconix SkyFETs is about 40 % lower than traditional trench MOSFETs.

Second, there is a time when the transformer current travels through the bdd, before the low-side MOSFET turns on. At this time, there will be power losses in the diode (P = VI). Reducing the V_F of the body drain diode, reduces this power loss. Vishay's SkyFETs offer a 38 % reduction in V_F to 0.44 V, compared to 0.72 V for a standard TrenchFET.

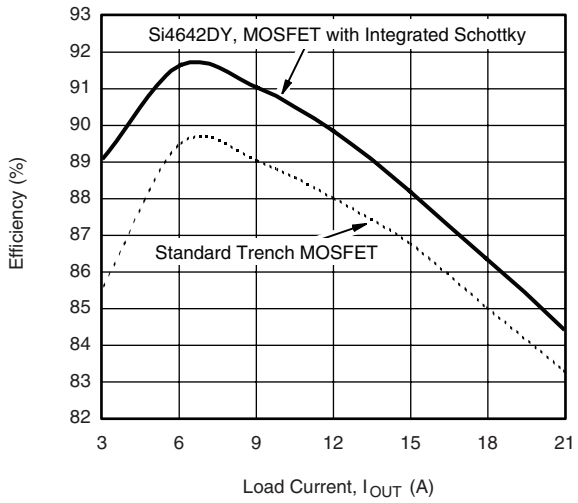

Fig. 8 MOSFET with Integrated Schottky as Low Side Switch Efficiency Performance Comparison, 300 kHz
V_{IN} = 19 V, V_{OUT} = 1.3 V

At a 300 kHz switching frequency, the Si4624DY SkyFET, used as a low-side MOSFET, delivers improved efficiency compared to a standard trench MOSFET. (Fig. 8).

Figure 9 highlights the improvement of efficiency at 550 kHz.

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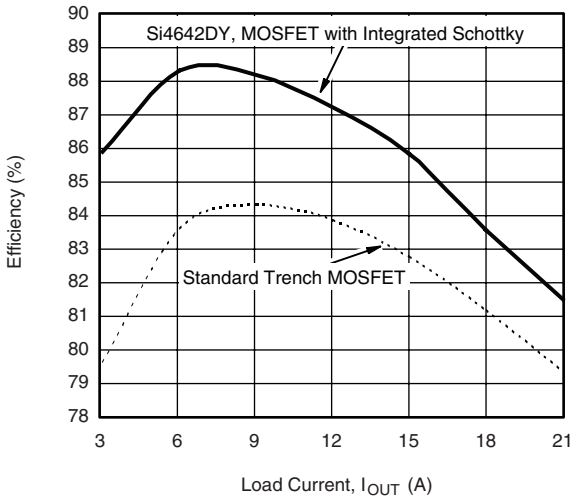

Fig. 9 - MOSFET with Integrated Schottky as Low Side Switch
Efficiency Performance Comparison, 550 kHz
V_{IN} = 19 V, V_{OUT} = 1.3 V

SUGGESTED DUAL V_{DS} = 30 V MOSFET FOR < 6.5 A OUTPUT (PER CHANNEL)									
DEVICE	**PKG**	**POL**	**CONFIG.**	**V_{DS} (V)**	**V_{GS} (V)**	**$R_{DS(ON)}$ MAX. AT V_{GS} (mΩ)**	**Q_G TYP. AT 4.5 V (nC)**	**Q_{GS} TYP. (nC)**	**Q_{GD} TYP. (nC)**
Si7994DP	PowerPAK SO8	Dual N	High Side	30	20	33	5	2.3	1.6
			Low Side						
Si7218DN	PowerPAK 1212-8	Dual N	High Side	30	20	33	5	2.3	1.6
			Low Side						
Si4816BDY	SO8	Dual N	High Side	30	20	22.5	7.8	2.9	2.3
			Low Side and Schottky	30	20	16	11.4	4.8	3.7
Si4618DY	SO8	Dual N	High Side	30	12	19.5	12.5	4.1	3.4
			Low Side and Schottky	30	12	11.5	17	5.6	4
Si4622DY	SO8	Dual N	High Side	30	20	18.6	19	8	6
			Low Side SKYFET	30	16	29	6	2.1	1.4
Si4618DY	SO8	Dual N	High Side	30	20	22	10.5	5	2.5
			Low Side and Schottky						