Switching Analysis of Synchronous Rectifier MOSFETs With Phase-Shifted Full-Bridge Converter and Current Doubler

By Patrick Chiang and Mark Hu

Abstract

This application note will analyze the switching behavior of synchronous rectifier MOSFETs in a phase-shifted full-bridge converter topology with a current doubler. Figure 1 shows the basic circuit of this application. An overview will describe the timing diagram of a phase-shifted full-bridge converter for achieving zero voltage switching (ZVS). Two topologies are introduced for gate driving of synchronous rectifier (SR) MOSFETs. The timing diagrams will introduce the SR MOSFET operations during every stage for both topologies. The body diode will be highlighted, and the operational phenomena that occur when the SR MOSFET turns off will be described. The power dissipation of SR MOSFETs will be presented as equations to assist in designs, while test results of waveforms will help in understanding the application. A summary will include the advantages of SR MOSFETs, an efficiency comparison, and other design considerations.

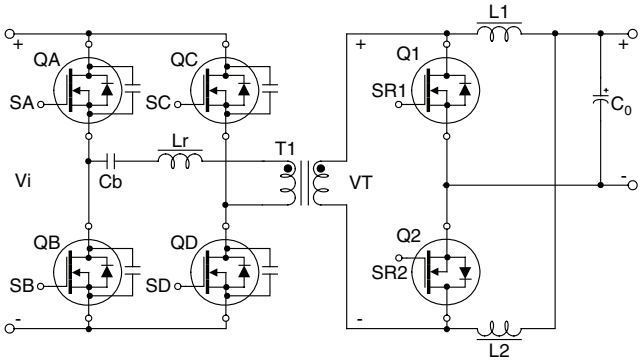

Figure 1 - Phase-Shifted Full-Bridge Converter

Introduction to the Phase-Shifted Full-Bridge Converter

The phase-shifted full-bridge converter has long been used to achieve high efficiency and high density in power supply designs with outputs from 500 W to 5000 W. The traditional full-bridge converter transfers power from primary bulk capacitors to secondary LC filters when its MOSFETs (QA and QD, or QB and QC) are turned on at the same time. This operation results in increased power dissipation (known as switching loss) when a primary MOSFET is turned on and off. The higher the switching frequency, the greater the switching losses.

The phase-shifted full-bridge converter introduces an almost 50 % fixed-duty cycle to QA, QB, QC, and QD. The pulse width modulation (PWM) duty is controlled by the overlapped duty of QA and QD, and QB and QC. There is a small amount of overlap between QA and QB, and QC and QD, which is called PWM delay (PWM delay AB, and PWM delay CD). PWM delay will prevent the same-side MOSFETs (QA and QB, or QC and QD) from turning on simultaneously, which would result in a short circuit that burns out the MOSFETs. In addition, the delay time helps the MOSFETs to achieve zero voltage switching (ZVS). When the PWM pulse is off, the snubber inductance Lr, by way of storage energy, will resonate with the output capacitances of the MOSFETs and oscillate the MOSFET voltage to zero before the MOSFETs turn on at the next period. At this stage, ZVS (which means no switching loss) occurs and a significant improvement in efficiency is gained.

Due to high density (per W/inch^3) and thermal considerations, most designers do not add an external snubber inductor in conjunction with the transformer (shown in Figure 1). The snubber inductance Lr results from the leakage inductance of transformer T1. Only if the primary current Ip is enough to let Lr be stored at a minimum energy, and an achieved ZVS transition, is the external inductor not necessary. Using the leakage inductance of the transformer, most power supplies can achieve ZVS with more than 50 % maximum load. It is necessary to add Cb to avoid an unbalance of the transformer flux and saturation of the transformer.

Switching Analysis of Synchronous Rectifier MOSFETs With Phase-Shifted Full-Bridge Converter and Current Doubler

Resonant Operation of ZVS

- The first criterion for achieving ZVS is

$$\frac{1}{2} \times Lr \times Ip^2 > \frac{1}{2} \times Cr \times Vi^2$$

where $Cr = \left[\left(\frac{8}{3} \times C_{OSS}\right) + Cxfm\right]$,

if Cxfrm is small and negligible with comparison to C_{OSS},

$$Cr = \left(\frac{8}{3} \times C_{OSS}\right).$$

$$\Rightarrow \frac{1}{2} \times Lr \times Ip^2 > \frac{4}{3} \times C_{OSS} \times Vi^2$$

Designers may measure the I_{DS} and V_{DS} of a MOSFET to find out at which output load ZVS of the MOSFET starts to happen (for example, 40 %). If Lr is the leakage inductance of the transformer, the LCR meter can measure Lr by shorting the secondary wire. Adequate Ip stores the energy and, by way of Lr, forces the V_{DS} of the MOSFET to zero before the MOSFET turns on.

In Figures 2 and 3, the primary current is Ip and a > b > c. The critical point is Ip = b. That is

$$\frac{1}{2} \times Lr \times b^2 = \frac{4}{3} \times C_{OSS} \times Vi,\ max^2 \Rightarrow b = \sqrt{\frac{8}{3} \times \frac{C_{OSS} \times Vi,\ max^2}{Lr}}$$

If Ip ≥ b, the MOSFET can achieve ZVS. If Ip < b, ZVS is not possible.

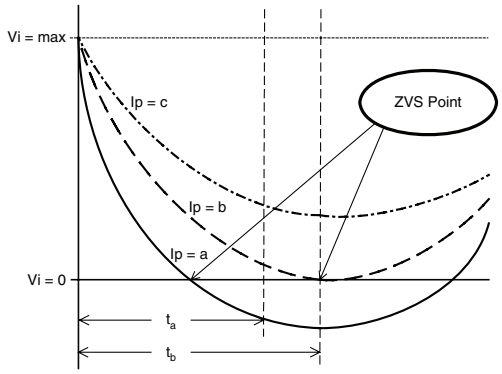

Figure 2 - C_{OSS} Discharging Waveform

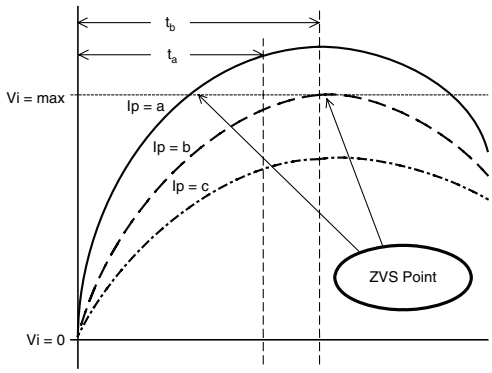

Figure 3 - C_{OSS} Charging Waveform

- The second criterion for achieving ZVS is that the delay time is long enough to allow resonant voltages to finish the energy transfer in C_{OSS} and Lr. Assuming the frequency of the resonant is Fr, one period time Tr is $\frac{1}{Fr}$.

Figures 2 and 3 show the voltage waveforms of the resonant transitions. Figure 2 occurs while the C_{OSS} of the MOSFET discharges from Vi = max to zero. Figure 3 occurs while the C_{OSS} of the MOSFET charges from Vi = zero to max. The boundary condition occurs when Ip = b. The delay time must be equal to or greater than tb, or the MOSFET cannot achieve ZVS. Designers may choose to let the delay time be equal to ta, and have no ZVS in light loads. The criteria of the duty cycle is $Duty_{maximum} + Duty_{delay} = 50\ \%$ switching period.

The larger delay time will cause the maximum duty cycle to be smaller, impacting the hold-up time performance.

The power transition from Lr to C_{OSS} needs to be completed to achieve ZVS. The minimum time is one-fourth of the resonant period.

$$\Rightarrow tb = \frac{1}{4} \times Tr$$

$$\Rightarrow Tr = \frac{1}{Fr},\ Fr = \frac{1}{2 \times \pi \times \sqrt{Lr \times Cr}}$$

$$\Rightarrow tb = \frac{\pi}{2} \times \sqrt{Lr \times Cr}$$

APPLICATION NOTE

Switching Analysis of Synchronous Rectifier MOSFETs With Phase-Shifted Full-Bridge Converter and Current Doubler

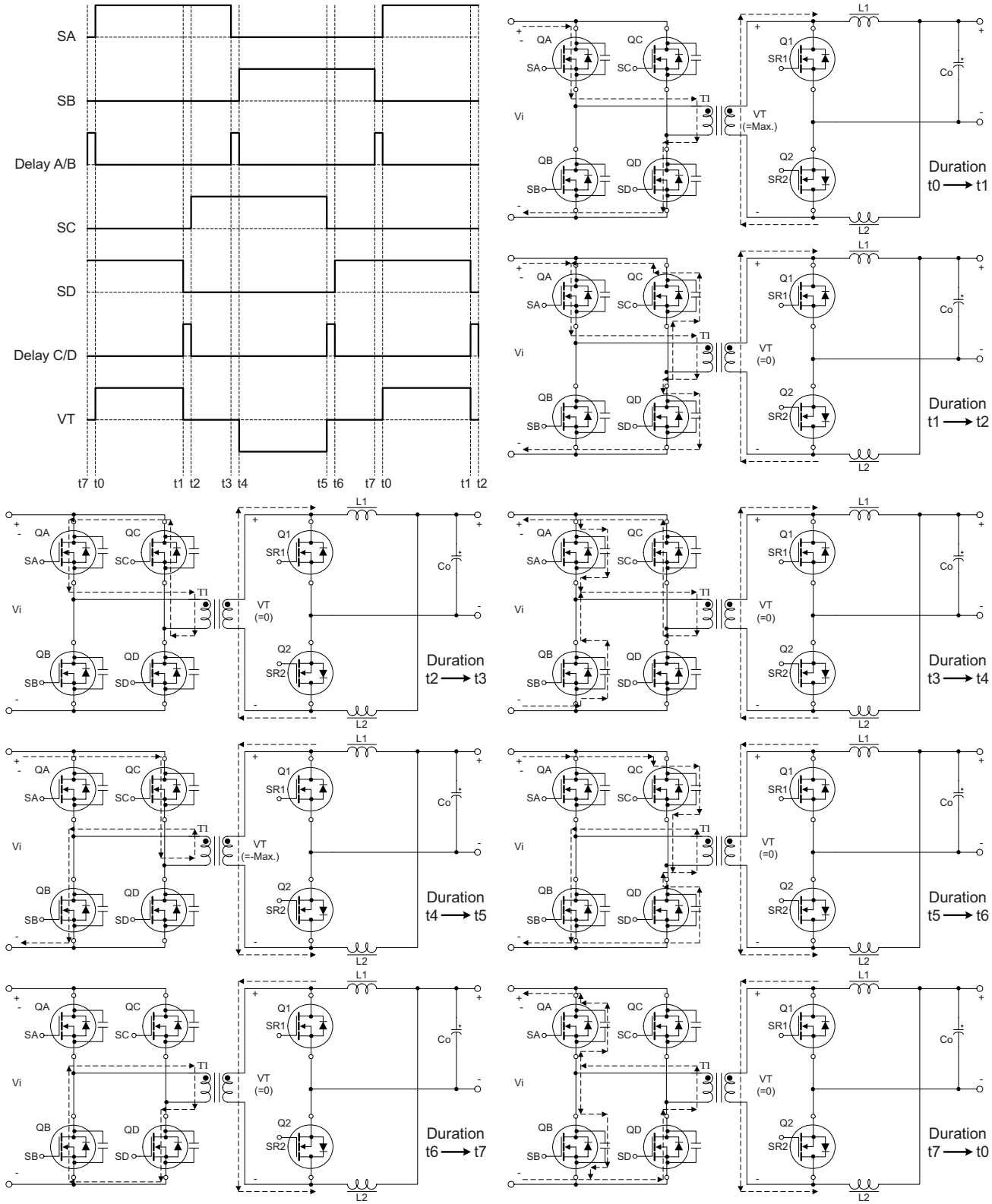

Figure 4 - Schematic Operation of Phase-Shifted Full-Bridge PWM Control

Switching Analysis of Synchronous Rectifier MOSFETs With Phase-Shifted Full-Bridge Converter and Current Doubler

Schematic Operation and Description

- **Timeframe t0 → t1:**

  At the beginning of this timeframe, QD has already turned on and the V_{DS} of QA is zero. QA starts to turn on when the V_{DS} equals zero. The primary current is flowing through QA, T1, and QD as shown in Figure 4. The power transfers from the Vi source tank to the VT of the secondary PWM pulse source by way of transformer T1.

- **Timeframe t1 → t2:**

  Inductance Lr exists inside of transformer T1. The characteristics of inductance will keep the current Ip in the same direction. If there is no passive component in the current loop of Ip, the value of Ip will remain the same with no energy loss. At t1, QD turns off. The stored energy of Lr forces Ip to keep flowing with its value at t1. This action will start to charge the C_{OSS} of QD and discharge the C_{OSS} of QC as shown in Figure 4. If the Ip is adequate as shown in Figure 4, the voltage of drain of QD, or source of QC, will resonate from Vi, max to zero. The ZVS transition will finish within one-fourth of the resonant cycle. After the voltage of drain of QD, or source of QC, reaches zero, the current Ip stops flowing through the C_{OSS}. It turns on the body diode of QC and Ip keeps flowing.

- **Timeframe t2 → t3:**

  At t2, QC starts to turn on. Ip transfers the current path from the body diode of QC to the MOSFET QC. As shown in Figure 4, the Ip current will keep flowing through QA, T1, and QC with almost the same value, which means the resistance loss is very low.

- **Timeframe t3 → t4:**

  At t3, QA turns off. The stored energy of Lr forces Ip to keep flowing with its value at t3. This action will start to charge the C_{OSS} of QA and discharge the C_{OSS} of QB as shown in Figure 4. If the Ip is adequate as shown in Figure 4, the voltage of source of QA, or drain of QB, will resonate from Vi, max to zero. The ZVS transition will finish within one-fourth of the resonant cycle. After the voltage of source of QA, or drain of QB, reaches Vi, max, the current Ip stops flowing through the C_{OSS}. It turns on the body diode of QB and keeps flowing.

- **Timeframe t4 → t5:**

  QC has already turned on and the V_{DS} of QB is zero. QB starts to turn on when its V_{DS} is zero. The primary current is flowing through QA, T1, and QD as shown in Figure 4. The power transfers from the Vi source tank to the VT of the secondary PWM pulse source by way of transformer T1.

- **Timeframe t5 → t6:**

  Inductance Lr exists inside of transformer T1. The characteristics of inductance will keep the current Ip in the same direction. If there is no passive component in the current loop of Ip, the value of Ip will remain the same. At t1, QC turns off. The stored energy of Lr forces Ip to keep flowing with its value at t5. This action will start to charge the C_{OSS} of QC and discharge the C_{OSS} of QD as shown in Figure 4. If the Ip is adequate as shown in Figure 4, the voltage of drain of QD, or the source of QC, will resonate from Vi, max to zero. The ZVS transition will finish within one-fourth of the resonant cycle. After the voltage of drain of QD, or the source of QC, reaches zero, the current Ip stops flowing through the C_{OSS}. It turns on the body diode of QD and Ip keeps flowing.

- **Timeframe t6 → t7:**

  At t6, QD starts to turn on. Ip transfers the current path from the body diode of QD to the MOSFET QD. As shown in Figure 4, the Ip current will keep flowing through QB, T1, and QD with almost the same value, which means the resistance loss is very low.

- **Timeframe t7 → t0:**

  At t7, QB turns off. The stored energy of Lr forces Ip to keep flowing with its value at t3. This action will start to charge the C_{OSS} of QB and discharge the C_{OSS} of QA as shown in Figure 4. If the Ip is adequate as shown in Figure 4, the voltage of drain of QB, or the source of QA, will resonate from zero to Vi, max. The ZVS transition will finish within one-fourth of the resonant cycle. After the voltage of drain of QB, or the source of QA, reaches Vi max, the current Ip stops flowing through the C_{OSS}. It turns on the body diode of QA and keeps flowing.

Primary Circuit Application and Consideration:

a. With adequate Ip, the primary MOSFETs of a phase-shifted full-bridge converter switch will show no dissipation at the turn-on stage, i.e. ZVS. However, the power dissipation at the turn-off stage cannot be avoided.

$\omega_r = 2 \times \pi \times Fr, ta, Ip = a$ which refers to Figure 3.

Vi, a is the maximum voltage when Ip = a.

$$\Rightarrow \frac{1}{2} \times Lr \times a^2 = \frac{4}{3} \times C_{OSS} \times Vi, a^2 \Rightarrow Vi, a = \sqrt{\frac{3}{8} \times \frac{Lr \times a^2}{C_{OSS}}}$$

Switching Analysis of Synchronous Rectifier MOSFETs With Phase-Shifted Full-Bridge Converter and Current Doubler

To calculate ta is to find the time Vi, a(t) = Vi, max

$$\Rightarrow Vi,a \times \sin(\omega_r \times ta) = Vi,max \Rightarrow ta = \frac{\sin^{-1}\left(\frac{Vi,max}{Vi,a}\right)}{\omega_r}$$

$$\Rightarrow Pat = \frac{1}{ta}\int_0^{ta}(Vi,a(t) \times Ip)dt = \frac{1}{t_a}\int_0^{ta}(Vi,a \times (\sin\omega \times t) \times Ip)dt = \frac{Vi,a \times a}{ta}\int_0^{ta}(\sin\omega_r \times t)dt$$

$$\Rightarrow Pat = \frac{Vi,a \times a}{ta \times \omega_r} \times (1 - \cos(\omega_r \times ta)) \rightarrow Pat = \text{power dissipation in the transition period.}$$

The power dissipation of a MOSFET at turn-off is Pa, off (T_{SW} is switching period).

$$\Rightarrow Pa,off = \frac{ta}{T_{SW}} \times \frac{Vi,a \times a}{ta \times \omega_r} \times (1 - \cos(\omega_r \times ta)) \Rightarrow Pa,off1 = \frac{Vi,a \times a}{T_{SW} \times \omega_r} \times (1 - \cos(\omega_r \times ta))$$

If Ip=b, then

$$\Rightarrow Vi,b = Vi,max;\ tb = \frac{1}{4 \times f_r} \Rightarrow tb = \frac{\pi}{2 \times \omega_r} \text{ where } \omega_r = 2 \times \pi \times f_r$$

$$Pat = \frac{2}{\pi} \times Vi,max \times b \text{ and } Pa = \frac{Vi,max \times b}{T_{SW} \times \omega_r}$$

b. When the MOSFETs and the transformer start the resonant transition, energy is sometimes lost. The $r_{DS(on)}$, the forward drop voltage of the body diode, the parasitical resistance in the PCB, and the wire resistance of the transformer gradually dissipate the energy stored as inductance. Some stored energy is dissipated in the time interval of the C/D resonant transition delay and the PWM-off transition. The stored energy of the A/B resonant transition delay will be smaller than that of the C/D resonant transition delay. Thus, it is easier to achieve ZVS in the C/D resonant transition delay than the A/B resonant transition delay. That is why the case thermal data of MOSFETs QA and QB are always higher than QC and QD.

c. Thermal considerations in light loads are a problem. Phase-shifted control enlarges the overlap waveforms of the MOSFET voltage and current in light loads. That means power losses will increase tremendously in this situation, because there is no ZVS and Ip keeps the voltage of the MOSFET at a high value before switching. Even worse, most current power supplies specify smaller airflow under light output load conditions as a way of reducing acoustic noise. The case temperature of the MOSFET will be very high. Designers should do thermal testing around 10 % to 40 % of the load and check the data carefully. Be sure to meet the de-rating guidelines of the customer's specifications. Designers may set a variable step value for delay A/B and delay C/D. Sensing the primary current, the controller changes to a longer delay time in light loads. The longer transition time can reduce the power losses in the MOSFET.

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Control Drivers of Synchronous Rectifier With Current Doubler

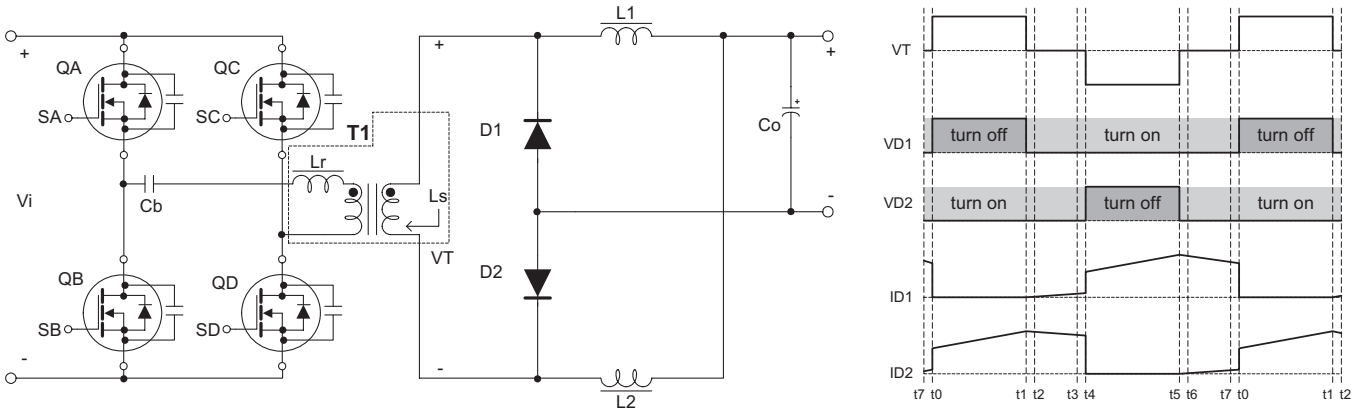

Figure 5 - Schematic Operation of Diode Rectifier

- The secondary side acts as a buck converter. The diodes act as switchers by following the power transferring from the primary side. When VT is positive, D1 will automatically turn off. When VT is negative, D2 will automatically turn off.
- Synchronous rectifiers can replace diode rectifiers. That is, control drivers of synchronous rectifiers behave as diode rectifiers. Because the product of the average current Id and $r_{DS(on)}$ is much lower than the V_F of the diode, higher efficiency can be achieved by using the SR topology. The SR MOSFET, however, must be controlled to turn on and perform in the zone of the diode turn-on as shown in Figure 5. If SR1 turns on before t1 and turns off after t0, the sudden short circuit of Q1 and Q2 will result in their burning out and damaging other components.
- Two types of control drivers have been introduced in today's application.

Type 1 SR Driver

- Designers may put the phase-shifted full-bridge controller in the secondary side of the main transformer. In this scenario, the control driver of the synchronous rectifier is built up without an insulation transformer. See Figure 6. SR1 is controlled "off" in t1 and t2, and t7 and t0, providing a delay that avoids the short circuit of Q1 and Q2 and results in optimal efficiency.

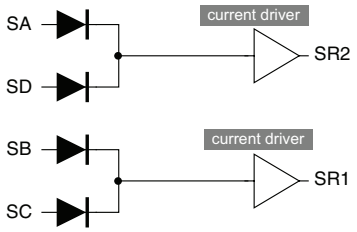

Figure 6 - Schematic Diagram of Type 1 Synchronous Rectifier

TRUTH TABLE OF TYPE 1 SYNCHONOUS RECTIFIER

STATE	PRIMARY GATE SIGNAL				SR INPUT SIGNAL	
	SA	SB	SC	SD	SR1	SR2
t0 → t1	H	L	L	H	L	H
t1 → t2	H	L	L	L	L	H
t2 → t3	H	L	H	L	H	H
t3 → t4	L	L	H	L	H	L
t4 → t5	L	H	H	L	H	L
t5 → t6	L	H	L	L	H	L
t6 → t7	L	H	L	H	H	H
t7 → t0	L	L	L	H	L	H

Switching Analysis of Synchronous Rectifier MOSFETs With Phase-Shifted Full-Bridge Converter and Current Doubler

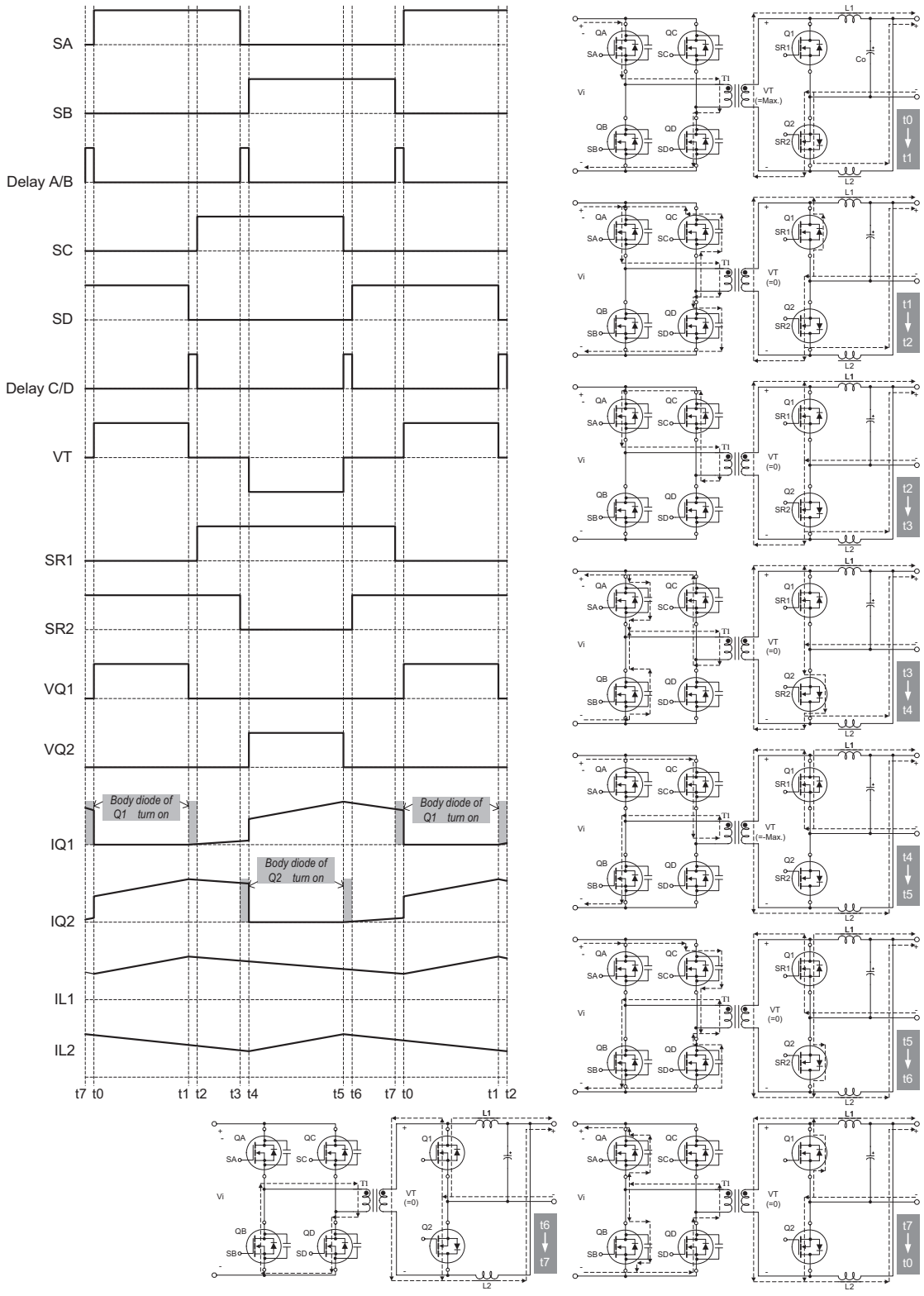

Figure 7 - Schematic Operation of Phase-Shifted Full-Bridge PWM Control With Type 1 SR Driver

Switching Analysis of Synchronous Rectifier MOSFETs With Phase-Shifted Full-Bridge Converter and Current Doubler

Schematic Operation and Description With Type 1 SR Driver

- **Timeframe t0 → t1:**

  QA and QD are turned on and power is transferred from the primary side to the secondary side. SR2 is already turned on. No current flows through Q1. Q2 will take all the transferring current flow through itself. However, before t0, the body diode of Q1 is turned on. At t0, forcing the body diode of Q1 to turn off will cause a diode reverse-recovery condition. The high spike voltage of Q1 V_{DS} and the turn-off switching loss occur.

  Assuming output inductors (L1 and L2) both work in continuous mode, the currents of L1 and L2 will keep flowing in the same direction. Two paths of current flow are separated through L1 and L2. The current of L1 is increasing by the forced voltage VT, and that of L2 is decreasing with the freewheeling stored energy in L2.

- **Timeframe t1 → t2:**

  At t1, the forced voltage is off and transfers from the maximum value to zero voltage. In this short time, Q1 V_{DS} will reach zero voltage and the Q1 body diode will turn on. Since the primary Ip keeps almost the same value, the current of the secondary side transformer is almost the same value as at t1. Therefore, the current of body diode Q1 will start at zero current and increase slowly. Besides the two current paths in the timeframe t0 → t1, the current through the Q1 diode and L1 is the third path.

- **Timeframe t2 → t3:**

  At t2, SR1 starts to turn the Q1 MOSFET on. Because the body diode of Q1 is already turned on, the V_{DS} of Q1 is zero. ZVS occurs in the turn-on switching of Q1. The three current paths are the same as those of timeframe t1 → t2. The third one, however, is not flowing through the Q1 diode, but the Q1 MOSFET.

- **Timeframe t3 → t4:**

  At t3, the voltage of QA source or QB source is resonated from the maximum value to zero voltage. In this short time, the V_{DS} of QB will reach zero voltage and the body diode will turn on. Since the primary IP keeps almost the same value, the current of the secondary side transformer is almost the same value as at t1. Therefore, the current of the body diode Q2 will take all the current of the Q2 MOSFET at t3. The three current paths are the same as those of timeframe t2 → t3. However, the path through MOSFET Q2 is changed through the body diode of Q2.

- **Timeframe t4 → t5:**

  QB and QC are turned on. SR2 is already turned on. There is no current flow through Q2. Q1 will take all the transferring current flow through itself. However, before t4, the body diode of Q2 is turned on. The high spike voltage of Q1 V_{DS} and the turn-off switching loss occur.

  Two paths of current flow are separated through L1 and L2. The current of L2 is increasing by forced voltage VT, and that of L1 is decreasing with the freewheeling stored energy in L2.

- **Timeframe t5 → t6:**

  At t5, the forced voltage VT is off and transfers from the maximum value to zero voltage. In this short time, Q2 V_{DS} will reach zero voltage and the Q2 body diode will turn on. Since the primary IP keeps almost the same value, the current of the secondary side transformer is almost the same value as at t1. Therefore, the current of body diode Q2 will start at zero current and increase slowly. Besides the two current paths in timeframe t4 → t5, the current through the Q2 diode and L2 is the third path.

- **Timeframe t6 → t7:**

  At t6, SR2 starts to turn the Q2 MOSFET on. Because the body diode of Q2 is already turned on, the V_{DS} of Q2 is zero. ZVS occurs in the turn-on switching of Q2. The three current paths are the same as those of timeframe t5 → t6. The third one, however, is not flowing through the Q2 diode, but the Q2 MOSFET.

- **Timeframe t7 → t0:**

  At t7, the voltage of QA source or QB source is resonated from the maximum value to zero voltage. In this short time, the V_{DS} of QB will reach zero voltage and the body diode will turn on. Since the primary IP keeps almost the same value, the current of the secondary side transformer is almost the same value as at t1. Therefore, the current of body diode Q1 will take all the current of the Q1 MOSFET at t7. The three current paths are the same as those of timeframe t6 → t7. The path through the MOSFET Q1, however, is changed through the body diode of Q1.

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Type 2 SR Driver

- The control driver of synchronous rectifier can use the PWM control signals SA and SB for the inputs. This is an easy way for a design to build up in circuitry (Figure 8). Obviously, the power loss of Q1 derives from the product of V_F in the body diode and the average in t2 to t4. It is greater than that of the type 1 SR driver.

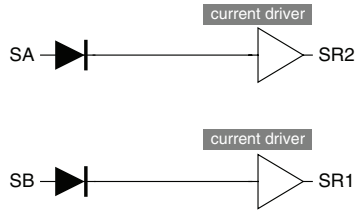

Figure 8 - Schematic Diagram of Type 2 Synchronous Rectifier

TRUTH TABLE OF TYPE 2 SYNCHONOUS RECTIFIER

STATE	PRIMARY GATE SIGNAL				SR INPUT SIGNAL	
	SA	SB	SC	SD	SR1	SR2
t0 → t1	H	L	L	H	L	H
t1 → t2	H	L	L	L	L	H
t2 → t3	H	L	H	L	L	H
t3 → t4	L	L	H	L	L	L
t4 → t5	L	H	H	L	H	L
t5 → t6	L	H	L	L	H	L
t6 → t7	L	H	L	H	H	L
t7 → t0	L	L	L	H	L	L

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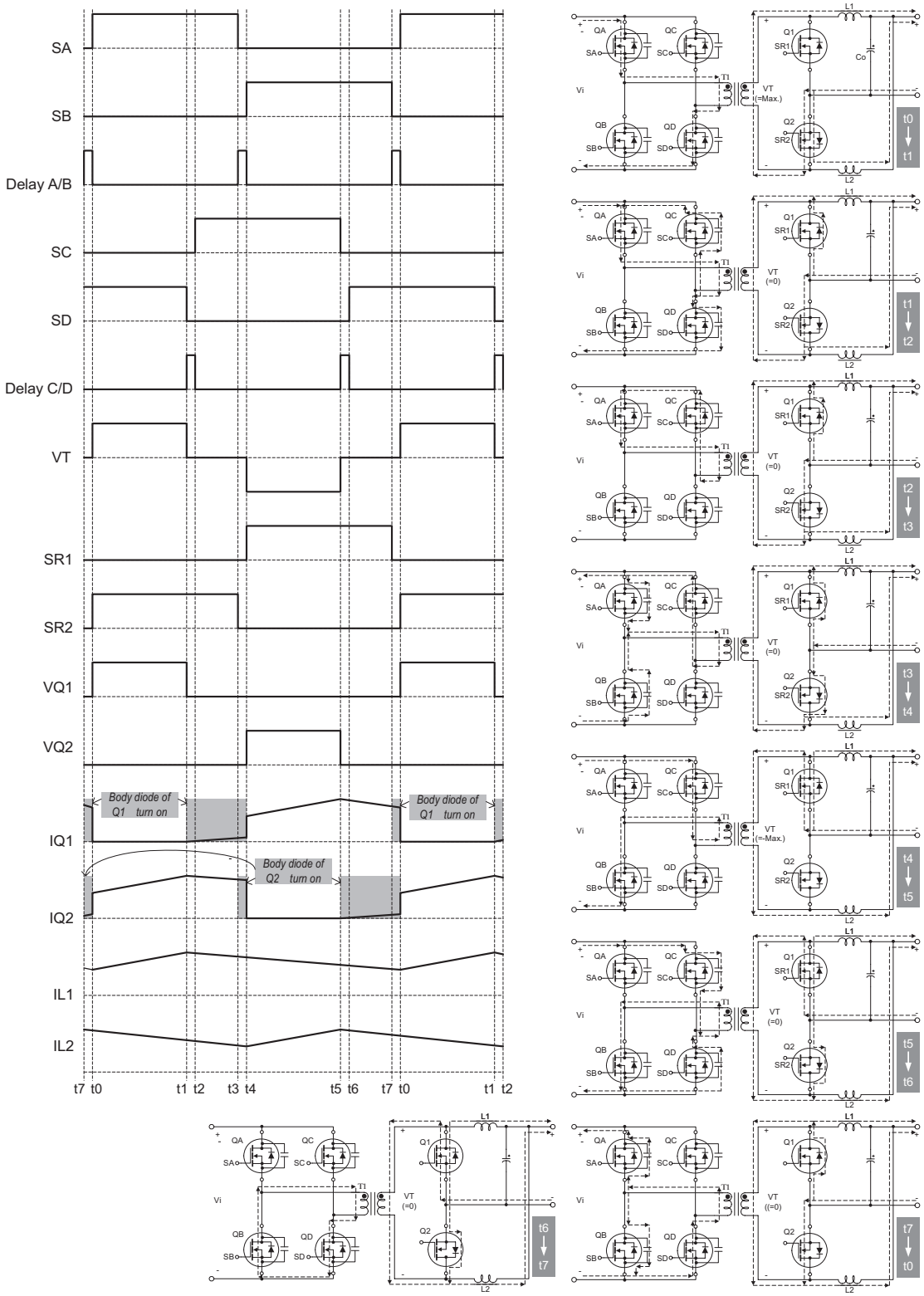

Figure 9 - Schematic Operation of Phase-Shifted Full-Bridge PWM Control With Type 2 SR Driver

Switching Analysis of Synchronous Rectifier MOSFETs With Phase-Shifted Full-Bridge Converter and Current Doubler

Schematic Operation and Description

- **Timeframe t0 → t1 and t1 → t2**

  At t0, SR2 starts to turn the Q2 MOSFET on. Because the body diode of Q2 is already turned on, the V_{DS} of Q2 is zero. ZVS occurs in the turn-on switching of Q2. The high spike voltage of Q1 V_{DS} and the turn-off switching loss also occur. Other operations are the same as type 1.

- **Timeframe t2 → t3**

  At t2, SR1 is still off. The current continues to flow through the body diode of Q1. Other operations are the same as type 1.

- **Timeframe t3 → t4**

  All operations are the same as type 1. However, SR1 and SR2 are low. The current will not flow through the MOSFET, but the body diode.

- **Timeframe t4 → t5 and t5 → t6**

  At t4, SR1 starts to turn the Q1 MOSFET on. Because the body diode of Q1 is already turned on, the V_{DS} of Q1 is zero. ZVS occurs in the turn-on switching of Q1. The high spike voltage of Q2 V_{DS} and the turn-off switching loss also occur. Other operations are the same as type 1.

- **Timeframe t6 → t7**

  At t6, SR2 is still off. The current continues to flow through the body diode of Q2. Other operations are the same as type 1.

- **Timeframe t7 → t0**

  All operations are the same as type 1. However, SR1 and SR2 are low. The current will not flow through the MOSFET, but the body diode.

Design Consideration of Synchronous Rectifier MOSFET

Voltage Spike of V_{DS} in Turn-Off of Body Diode

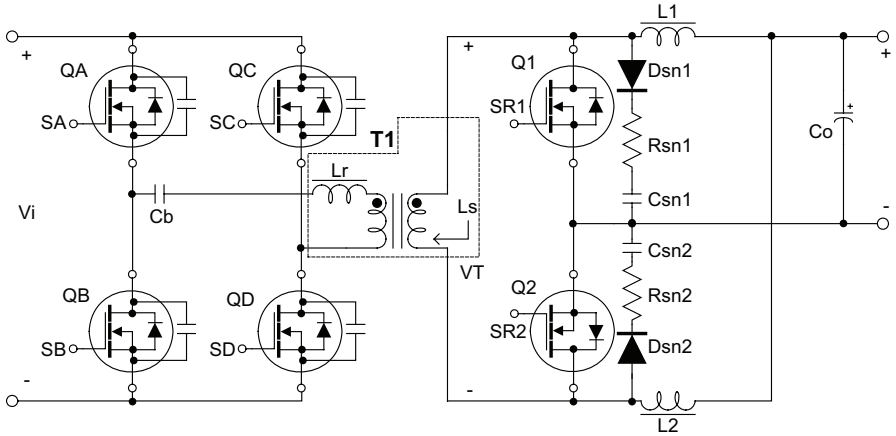

Figure 10 - Leakage Inductance of Transformer and Snubber of SR

Since Q2 is on at t0, Q1 will be off at the same time. The leakage inductance Ls $\left(=\frac{Ns^2}{Np^2}\times Lr\right)$ is transferred from the primary side to the secondary side and is combined with the parasitical capacitance (PCB and MOSFET). Inductance L and capacitance C resonate a high-voltage spike. This spike may cause an over-rating of V_{DSS} in the SR MOSFET. The spike only happens at the turn-off moment. The snubbers may be added as shown in Figure 10. Below, we report on experiments aimed at discovering the main parameter that causes the voltage spike. The results are obtained by testing a power supply.

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Delay Circuit of Control Driver

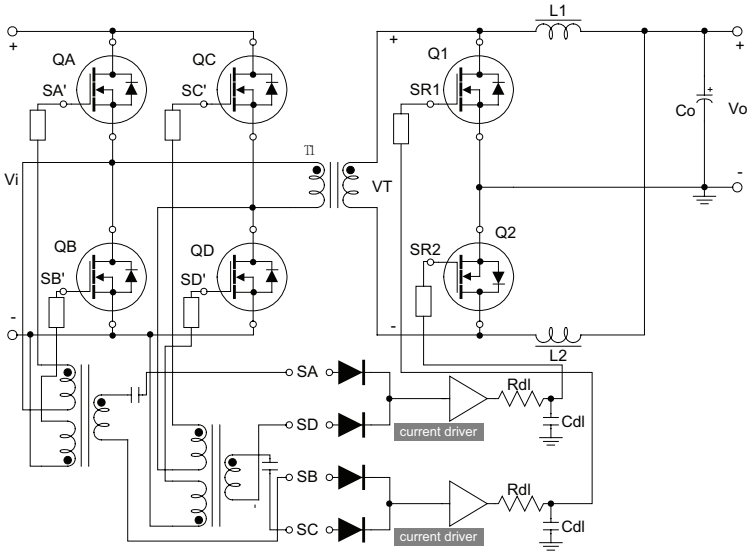


Figure 11 - Driver Circuit With RC Delay of Secondary SR

Putting the feedback control and PWM controller on the secondary side allows better regulation of the output and simplifies design of the control compensator. Most power supplies use a pulse transformer (or driver transformer) to drive the primary MOSFET. But this approach does not represent an "ideal" transformer, and its use introduces switching delays for SA, SB, SC, and SD. Figure 11 shows a design that measures the delay time between SA and SA', and sets the RC delay for the SR driver, so that the SR MOSFET will not turn on before the primary MOSFET, avoiding the short circuit of Q1 and Q2.

Calculation of SR Power Dissipation

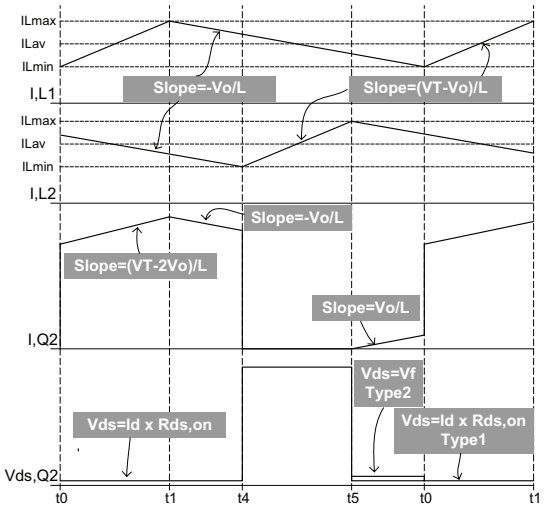


Figure 12 - Illustration of Power Dissipation of Synchronous Rectifier

To simplify the calculation, the duration of the A/B and C/D delays can be considered negligible. Figure 12 shows the current waveforms of the output inductors Id and V_{DS} of the SR Q2 MOSFET.

Switching Analysis of Synchronous Rectifier MOSFETs With Phase-Shifted Full-Bridge Converter and Current Doubler

Power dissipation calculations of the four periods according to the type 1 SR driver are stated as follows:

1. Timeframe t0 → t1

$$\text{average Id} = IL_{av} + IL_{av} = 2 \times IL_{av} = Io\left(IL_{av} = \frac{Io}{2}\right)$$

$$V_{DS} = r_{DS(on)} \times \text{average Id} = r_{DS(on)} \times Io$$

$$\text{Power dissipation Pd1} = \left(\frac{D \times T_S}{T_S}\right) \times Id \times V_{DS} = D \times r_{DS(on)} \times Io^2$$

2. Timeframe t1 → t4

$$\text{average Id} = Io + T_{SX}\left(\frac{Vo}{4 \times L} - \frac{D \times Vo}{2 \times L}\right) \qquad V_{DS} = r_{DS(on)} \times \text{average Id} = r_{DS(on)} \times \left[Io + T_{SX}\left(\frac{Vo}{4 \times L} - \frac{D \times Vo}{2 \times L}\right)\right]$$

$$\text{Power dissipation Pd2} = \left[\frac{(0.5 - D) \times T_S}{T_S}\right] \times Id \times V_{DS} = (0.5 - D) \times r_{DS(on)} \times \left[Io + T_{SX}\left(\frac{Vo}{4 \times L} - \frac{D \times Vo}{2 \times L}\right)\right]^2$$

3. Timeframe t4 → t5

Power dissipation = Turn-off power loss according to waveforms

$$Pd3 = \frac{t_{rr}}{2 \times T_S} \times V_{DS,\,off} \times Irm$$

4. Timeframe t5 → t0

$$\text{average Id} = T_{SX}\left(\frac{Vo}{4 \times L} - \frac{D \times Vo}{2 \times L}\right)$$

$$V_{DS} = r_{DS(on)} \times \text{average Id} = r_{DS(on)} \times T_{SX}\left(\frac{Vo}{4 \times L} - \frac{D \times Vo}{2 \times L}\right)$$

$$\text{Power dissipation Pd2} = \left[\frac{(0.5 - D) \times T_S}{T_S}\right] \times Id \times V_{DS} = (0.5 - D) \times r_{DS(on)} \times \left[T_{SX}\left(\frac{Vo}{4 \times L} - \frac{D \times Vo}{2 \times L}\right)\right]^2$$

5. Total Power Dissipation = Pd1 + Pd2 + Pd3 + Pd4

Example:

Assume T_S = 10 µs, D = 0.3, Io = 30 A, Vo = 12 V, L = 10 µH, $r_{DS(on)}$ = 4.7 mΩ, t_{rr} = 40 ns, Irm = 6 A, $V_{DS,\,off}$ = 40 V

$$Pd1 = 0.3 \times 0.0047 \times 30^2 = 1.269\ \text{W}$$

$$Pd2 = 0.2 \times 0.0047 \times \left[30 + 10 \times 10^{-6} \times \left(\frac{12}{4 \times 10 \times 10^{-6}} - \frac{0.3 \times 12}{2 \times 10 \times 10^{-6}}\right)\right]^2 = 0.2 \times 0.0047 \times 31.2^2 = 0.915\ \text{W}$$

$$Pd3 = \frac{40 \times 10^{-9}}{2 \times 10 \times 10^{-6}} \times 40 \times 6 = 0.48\ \text{W}$$

$$Pd4 = 0.2 \times 0.0047 \times \left[10 \times 10^{-6} \times \left(\frac{12}{4 \times 10 \times 10^{-6}} - \frac{0.3 \times 12}{2 \times 10 \times 10^{-6}}\right)\right]^2 = 0.2 \times 0.0047 \times 1.2^2 = 0.002\ \text{W}$$

• Total power dissipation of type 1 MOSFET = 2.666 W

If the driver is type 2, Pd4 is different (V_F = 1.3 V)

$$Pd4 = \left[\frac{(0.5 - D) \times T_S}{T_S}\right] \times V_F \times \left[T_{SX}\left(\frac{Vo}{4 \times L} - \frac{D \times Vo}{2 \times L}\right)\right] = 0.2 \times 1.3 \times 1.2 = 0.312\ \text{W}$$

Pd1, Pd2, Pd3 are same as those of type 2

• Total power dissipation of type 2 MOSFET = 2.976 W

If there is no SR, just Schottky diode rectifiers operate in the secondary side (V_F = 0.8 V)

$$Pd1 = \left(\frac{D \times T_S}{T_S}\right) \times V_F \times Io = 0.3 \times 0.7 \times 30 = 7.2\ \text{W}$$

$$Pd2 = (0.5 - D) \times V_F \times \left[Io + T_{SX}\left(\frac{Vo}{4 \times L} - \frac{D \times Vo}{2 \times L}\right)\right] = 0.2 \times 0.8 \times 31.2 = 4.992\ \text{W}$$

$$Pd3 = \frac{40 \times 10^{-9}}{2 \times 10 \times 10^{-6}} \times 40 \times 6 = 0.48\ \text{W}$$

$$Pd4 = \left[\frac{(0.5 - D) \times T_S}{T_S}\right] \times V_F \times \left[T_{SX}\left(\frac{Vo}{4 \times L} - \frac{D \times Vo}{2 \times L}\right)\right] = 0.2 \times 0.8 \times 1.2 = 0.192\ \text{W}$$

• Total power dissipation of Schottky diode = 12.864 W

Switching Analysis of Synchronous Rectifier MOSFETs With Phase-Shifted Full-Bridge Converter and Current Doubler

Test Results and Analysis of Synchronous Rectifier MOSFET

Do the Voltage Spikes of SR Relate to t_{rr} and Q_{rr}?

Assume the spike is related to t_{rr} and Q_{rr} of the body diode, because the spike is found while the MOSFET is turned off. If t_{rr} and Q_{rr} are bigger, that may induce the larger V_{DS} spike in the recovery period.

The following test waveforms show:

(1) Channel 3: V_{DS}; 50 V/div

(2) Channel 4: Id; 5 A/div

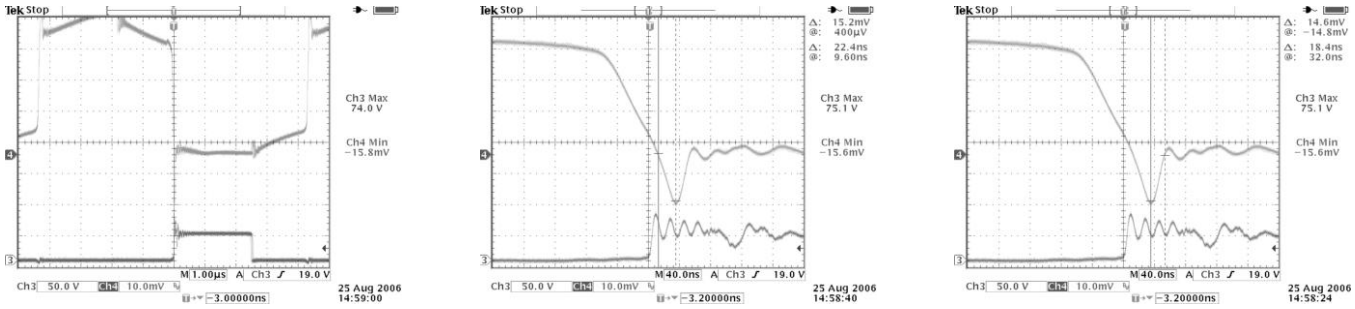


Figure 13 - 30-A Load of SUP90N08-4m8p

1. Test waveforms in Figure 13 show that the spike occurs when SR has been turned off and the reverse voltage of V_{DSS} starts to rise.
2. After SR is turned off, the current of the SR body diode goes negative and processes the reverse recovery operation.
3. Placing capacitors in between the drain and source of SR is one method of finding out if the voltage spike is related to t_{rr}.

Does the Voltage Spike of SR Relate to Cds and Cdg?

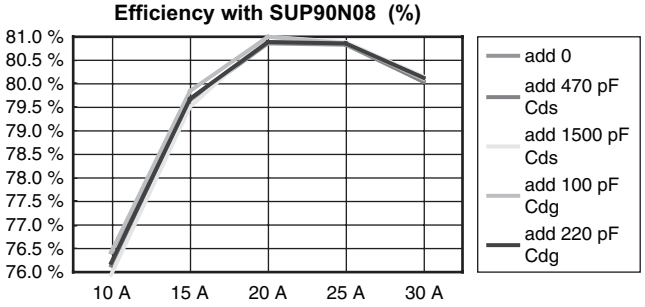
Assume the spike is related to Cds, Cdg, and Cgs of the body diode. Changing Cds or Cdg may change C_{iss}, C_{rss}, and C_{OSS} of the SR MOSFET. The change probably interferes with the efficiency, Ids, and V_{DS} waveforms.

The following data shows the test results. Some test waveforms are shown in the last section for your reference. The comparison of efficiency and the V_{DSS} spike are listed in the table and statistic chart.

1. Efficient Result

- No significant difference of efficiency for SR by adding Cds and Cdg with SUP90N08.

	OUTPUT LOAD	ADD 0 (%)	ADD 470 pF Cds (%)	ASS 1500 pF Cds (%)	ADD 100 pF Cdg (%)	ADD 220 pF Cdg (%)
Power Supply Efficiency with SUP90N08	10 A	76.4	76.2	75.9	76.4	76.2
	15 A	79.6	79.7	79.5	79.8	79.7
	20 A	80.9	80.9	81.0	81.0	80.9
	25 A	80.8	80.8	80.9	80.8	80.9
	30 A	80.0	80.0	80.1	80.1	80.1

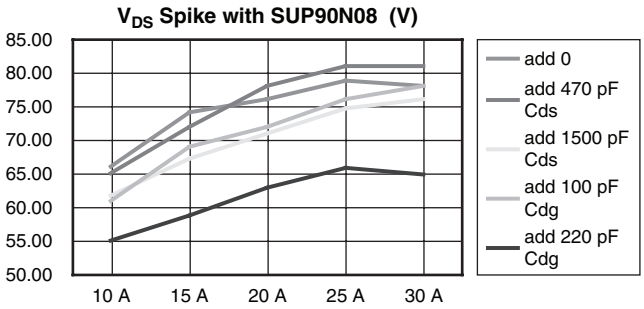


Switching Analysis of Synchronous Rectifier MOSFETs With Phase-Shifted Full-Bridge Converter and Current Doubler

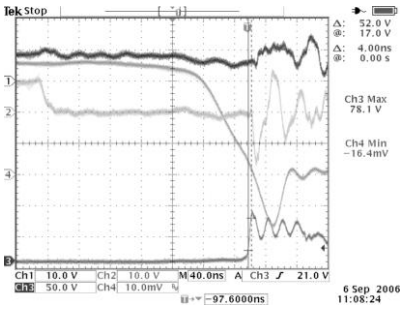
2. V_{DS} Spike Result

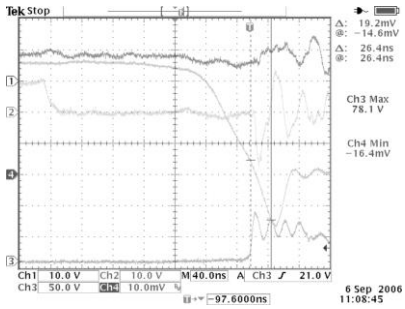
- Adding extra Cds in SUP90N08 does not significantly improve the V_{DS} spike. However, adding extra Cdg in SUP90N08 leads to improvement (Cdg = 220 pF, around 13 V below the original data).

	OUTPUT LOAD	ADD 0	ADD 470 pF Cds	ASS 1500 pF Cds	ADD 100 pF Cdg	ADD 220 pF Cdg
V_{DS} Spike with SUP90N08	10 A	66.0	65.1	61.7	61.1	55.1
	15 A	74.1	72.0	67.4	69.1	58.9
	20 A	76.0	78.1	71.1	71.9	63.0
	25 A	79.0	81.0	74.9	76.1	65.9
	30 A	78.1	81.0	76.0	78.0	65.0

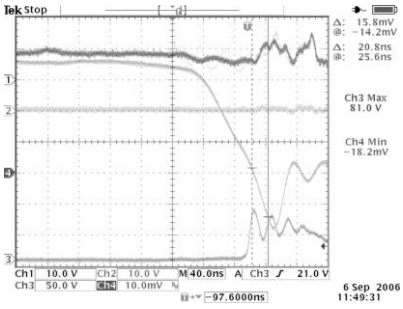


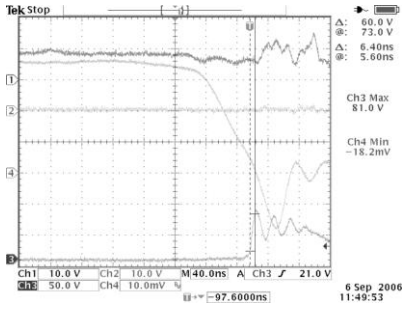
The following test waveforms show "Channel 1: Vg, Q1; 10 V/div", "Channel 2: Vg, Q2; 10 V/div", "Channel 3: V_{DS}, Q2; 50 V/div", and "Channel 4: Id, Q2; 5 A/div":



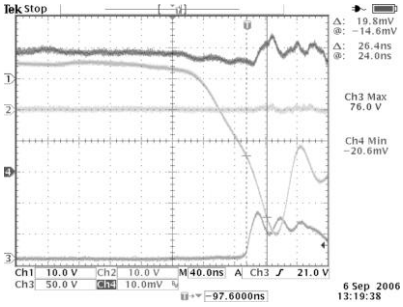


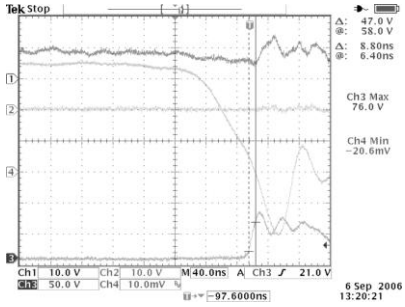
30-A Load of SUP90N08-V1





30-A Load of SUP90N08-V1, add Cds 470 pF





30-A Load of SUP90N08-V1, add Cds 1500 pF

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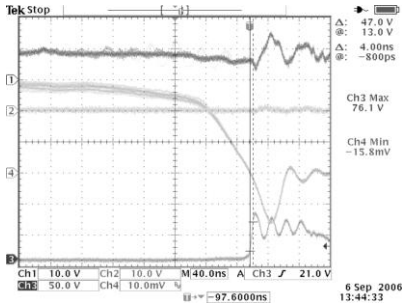
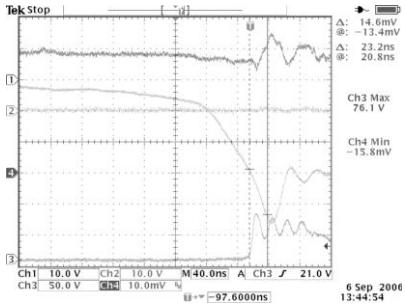
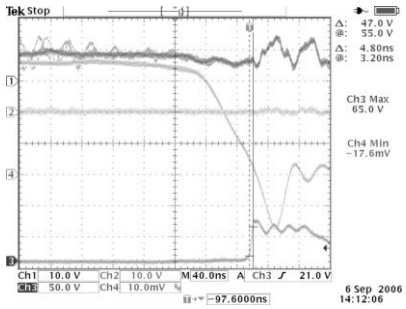
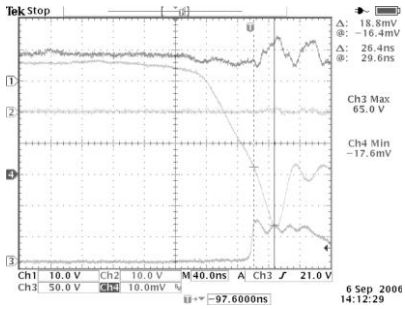




25-A Load of SUP90N08-V1, add Cdg 100 pF





30-A Load of SUP90N08-V1, add Cdg 220 pF

References

[1] Richard G. Hoft, “Semiconductor Power Electronics”, published by Van Nostrand Reinhold Company Inc. in 1986.

[2] Bill Andreycak, “Phase Shift, Zero Voltage Transition Design Consideration and the UC3875 PWM Controller”, Texas Instruments Literature No. SLUA107.

[3] Steve Mappus, “Control Driven Synchronous Rectifier in Phase shifted Full Bridge Converters”, Texas Instruments Literature No. SLUA287.