VC0882
Data Book

Revision 0.92

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CONTENTS

Chapter 01

Overview

1 Overview

The Vimicro VC0882, is a high performance, low power, multimedia application and high integrated system-on-chip (SOC) targeted at Application Processor (AP) of Tablet PC and Smart Phone. It is implemented on TSMC 65nm low power process technology.

The embedded microprocessor in VC0882 is based on 1.3Ghz ARM Cortex-A8 with NEON coprocessor. Also it is integrated with the high performance video decoder up to 1080P with 30fps for H.264, H.263, RMVB, MPEG4, MPEG2,VC1 etc. And it can support H.264, MPEG4, H.263 video encoder up to 30fps for 720p.

VC0882 is embedded for 2D and 3D graphic acceleration processor (GPU) to support display and gaming. This GPU delivers the scalable ultra-threaded unified shader architecture up to 15MTriangle rate per second. Also it supports the industry standard API such as Open GL ES1.1 and 2.0, Open VG1.0

Camera interface supports multiple formats from parallel sensors, ccir656 interface and raw image data. Display engine can deal with overlay of 4 display layers plus background and HW cursors. The video subsystem also supports SDTV and HDTV with 10-bit 3-channel 250Mhz analog Video DAC output. 24 bits LCD interface is applied with most of post processing and 1920x1080 maximum display sizes for all of panels and HDMI Bridge. It also supports the face detection function through the cooperation of hardware and software.

VC0882 can support most of high-level operation systems such as Android OS and Linux. And it integrates the state-of-the-art power management technologies for dynamic voltage control with multi power domains.

Integrated DDR controller can be compatible to external LPDDR, DDR2 and DDR3 with the data rates up to 667Mb/s. It supports 6 high performance and low power PLLs for flexible clock switch. VC0882 includes 3 SDIO/MMC card interfaces and 8bits/16bits NAND Flash with ECC, 2 PWMs, 3 UART interfaces, 2 SPI controller interfaces. One USB OTG 2.0 and one USB Host 2.0 can implement the data transfer between SOC and PC. Also, VC0882 contains the embedded 10-bit SAR ADC with 4-wire touch panel interface and carries one high quality 24-bit stereo ADC and DAC for audio processing. It can support the EFUSE function to program electrical fuse IP.

Chapter 02

Feature Description

2 Feature Description

2.1 System Block Diagram

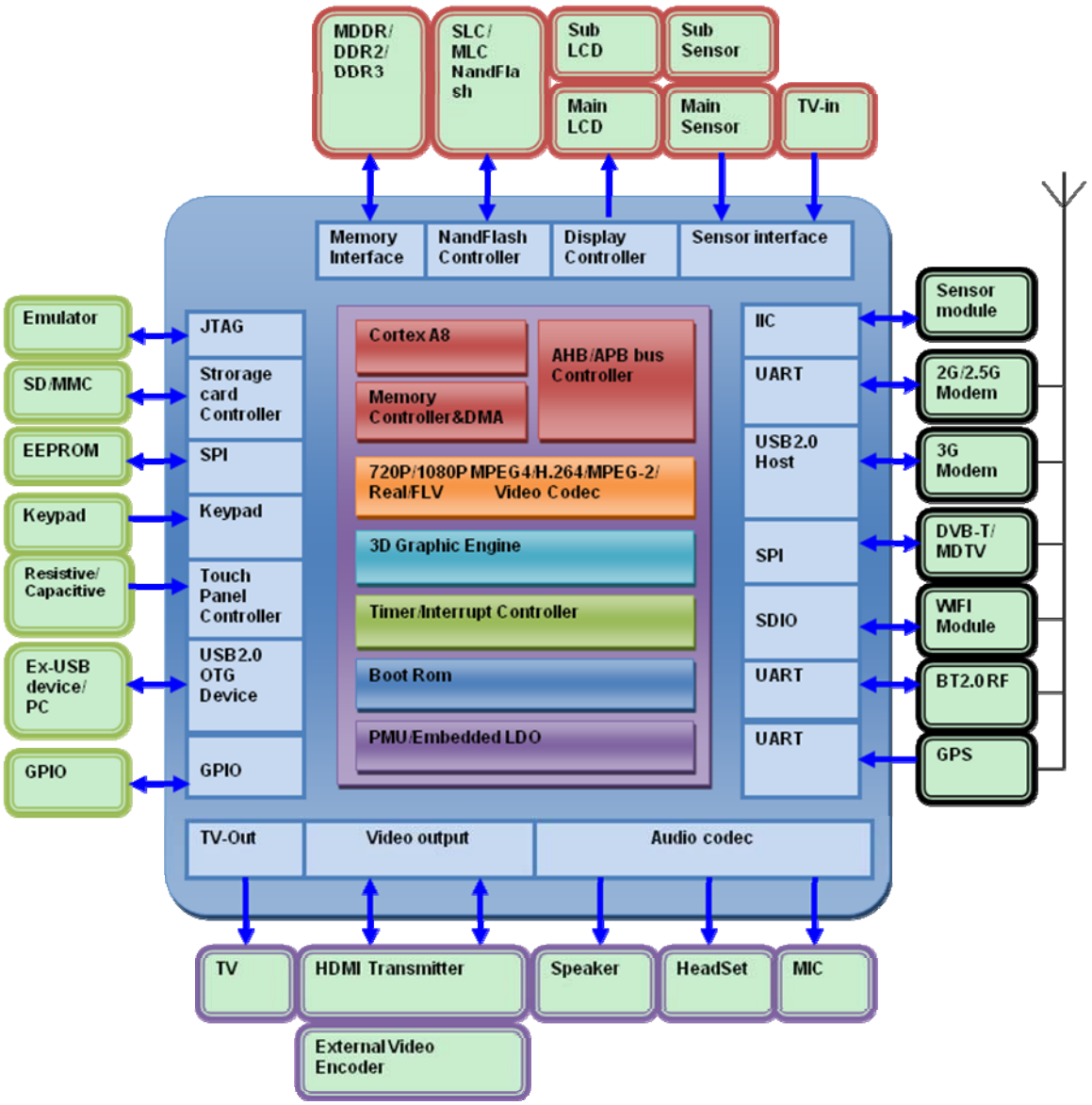

Figure 2-1 System Diagram of 445BGA

2.2 Highlight Feature

- Embedded up to 1.3Ghz ARM CORTEX-A8 CPU with v7-A instruction set
- Embedded up to 720p H.264, MPEG-4, H-263 video encoder with 30fps
- Embedded up to 1080p H.264, SVC, MPEG-4, MPEG-2, MPEG-1, H.263, VC-1, JPEG, RV, VP6 and DivX video decoder with 30fps
- Embedded with graphic 3D engine for compliant with the OpenGL ES 2.0; OpenGL ES1.1; OpenVG 1.1
- Embedded with Data rates of up to 667 Mb/s (333 MHz) for LPDDR, DDR2 and DDR3
- Embedded 6 PLLs for flexible clock switch
- Support parallel cameral sensor interface with max 4Kx4K resolution
- Support LCD interface for DBI, DPI and HDMI bridge
- Support NTSC and PAL SDTV and YPbPr analog signals output on 480i /480p /576i /576p /720p /1080i /1080p systems
- Embedded 8 bit/16 bit NAND Flash controller with up to 48 bits ECC
- Supports 4 SDIO devices
- One USB host and one USB OTG compliant with USB2.0 specification
- Contains a high-quality 24-bit audio stereo ADC and a high-quality 24-bit stereo DAC
- Support Touch Panel Interface with10-bit SAR ADC: DNL - ±1 LSB, INL - ±2 LSB
- Embedded with multi-power domains and smart DVFS scheme
- Power consumption value: 108mW for audio playing, 183mW for screen display, 630mW for 1080P player and 800uW for sleep mode

2.3 CPU Subsystem

■ Embedded ARM CORTEX-A8

- Full implementation of the ARM architecture v7-A instruction set
- 64-bit high-speed Advanced Microprocessor Bus
- Programmable CPU frequency up to 1.3Ghz for typical case
- memory interface supporting multiple outstanding transactions
- A pipeline for executing ARM integer instructions
- A NEON pipeline for executing Advanced SIMD and VFP instruction sets
- Dynamic branch prediction with branch target address cache, global history buffer, and 8-entry return stack
- Memory Management Unit (MMU) and separate instruction and data Translation

- Look-aside Buffers (TLBs) of 32 entries each
- Level 1 32KB instruction cache and 32KB data caches
- Level 2 128KB cache
- Level 2 cache with parity and Error Correction Code (ECC) configuration option
- Embedded Trace Macrocell (ETM) support for non-invasive debug
- Static and dynamic power management including Intelligent Energy Management (IEM)
- ARMv7 debug with watch point and breakpoint registers and a 32-bit Advanced
- Peripheral Bus (APB) slave interface to a CoreSight debug system.

■ Interrupt Controller

- Hierarchical interrupt scheme which process 1st level interrupts in Interrupt Controller while handling 2nd level interrupt in the associated sub-modules
- Support both FIQ and IRQ
- Support up to 32 interrupts
- Using interrupt source based MASK scheme and source pending registers to avoid losing interrupts
- Programmable interrupt prioritization

■ Timers

- 3 general purpose timers, 4 dual timers and 1 watchdog timer
- Programmable timer period and timer operation mode
- Individual interrupt for each timer
- Unique 24MHz clock for all timer

■ CLOCK & RST

- Supports 1 oscillator (or crystal): 26 MHz XCLK
- Embeds 6 high performance, low power PLLs
- Includes configurable clock dividers to produce desired clock frequencies
- Implements clock gating technology to save power
- Inserts clock multiplexers to enhance flexibility
- Seamlessly dynamic clock switching between XCLK and all 6 PLLs
- Integrates pmu hardware reset, watchdog reset, global software reset and each module's individual software reset
- Inserts clock multiplexers to enhance flexibility

■ EFUSE

- Support to manage the electrical fuse IP by APB bus in normal mode or by

PAD on ATE test mode
- Embedded power switch
- Support to program to 1 bit at a time according to the configured address
- Software can read 1-8 bytes at a time according to configured address and configured read byte length
- Provide power down and standby mode
- Asynchronous signal interface

2.4 Memory Subsystem

■ DDR controller

- Compatible with JEDEC standard LPDDR, DDR2, DDR3
- Data rates of up to 667 Mb/s (333 MHz)
- Compatible with the AMBA 3 AXI protocol
- Compatible with the AMBA 3 APB protocol
- Supported AXI burst type: incremental and wrap
- Register programmable timing parameters support DDR2/DDR3/LPDDR1 components from DRAM various vendors
- Support LPDDR1/DDR2 read/write command interrupt access
- Advanced features such ODT, ZQ Calibration and *additive latency*
- Support for two CSs (chip select) with shared clock pins, command pins, address pins and data pins
- Support for DDR device density ranging from 64Mbit to 2Gbit
- Support 16bit/32bit LPDDR1/DDR2/DDR3 device
- Supports autonomous DDR power down entry and exit based on programmable idle periods
- Support for self refresh entry on software command and automatic exit on DRAM access command arrival
- Automated Read DQS recognition and Automated Dynamic DQS Drift Compensation
- Built-in DQS Gate Training
- Support DDR3 DLL-off Mode
- Support LPDDR1 Deep Power Down Mode

■ DMA Controller

- Compliance to the AMBA 3.0 Specification---AXI protocol for integration into SoC implementation.
- One DMA channel which can support unidirectional transfer for software request
- Support memory-to-memory transfers

- Support Software link list descriptor-based DMA transfers
- Support programming max burst length

■ SRAM Controller

- Embedded 32Kbyte SRAM in chip
- Supports 14 bit address and 16 bit data

■ Acts as single-port SRAM for test program and as dual-port SRAM

■ ROM Controller

- Embedded with 64Kbyte ROM
- Supports with 14 bit address and 64 bit data
- For system boot only

2.5 Video Subsystem

■ Camera Interface

- Support master type sensor module and 8-bit parallel data output from sensor
- Support two camera sensors (only one works at the same time)
- Support max sensor resolution: 4096x4096 and 100Mhz max pixel clock
- Support max output image size (to memory): 4096x4096
- Support parallel interface for SYNC mode or ITU-R BT656 mode
- Support YCbCr422-format data/RAW image data/JPEG compressed data/RGB data (Bypass post-processing for RAW data/JPEG data/RGB data)
- Support two post-processing paths for capture and display
- Support up-scaling and down-scaling for capture path/preview path
- Capture path support slice mode and frame mode
- Support auto-focus
- Special Effect
    - o Mono color
    - o Sepia
    - o Special color
    - o Negative
    - o Four blocks
    - o Grid color

■ Display Engine

- Support 4 display layers plus background and HW cursor
- Support HW cursor with max resolution 64x64
- Using Pipeline architecture to implement overlay & alpha-blending operation
- Support up-scaling for overlay pixel data up to 1920x1080
- Support brightness/contrast/hue/saturation adjustment
- Support programmable gamma correction
- Support dithering for less than 24-bit color display
- Provide capture path to implement the function as “capture with frame”
- Max panel resolution: 1600x1200 for TV/1920x1080 for LCD panel and Max pixel rate up to 162MHz
- Support BT601 and BT609 color domain
- Programmable bits-per-pixel when output to LCDIF module: 16/18/24-bpp such as YUV422, RGB565, RGB666, RGB888, and etc.
- Support programmable multi-cycle output mode: 1/2/3/4 cycles per pixel

■ Face Detection

- Includes the calculation of integral and LAB (Locally Assembled Binary) in hardware and some functions implemented by software
- Support maximum sizer image width is 320 pixels, height is 240 pixels, minimum sizer image width is 24 pixels, height is 24 pixels and no limitation for original image size
- About process 5~10 QVGA frames in a second
- Support detection of smile faces, but not wink faces and report the eyes position.
- Support the face in profile angle is -20 ~ 20 degrees, pitching angle is -30 ~ 30 degrees.
- Support detection of black skin faces, color eyes and white hair

■ Video Encoder

- Supports H.264 baseline Levels 1-3.1, I-Slice and P-Slice CAVLC encoding, contained intra prediction, image size up to 1280x1024
- Supports MPEG-4 Levels 1-5, I-VOP and P-VOP, Max MV range +-16 pixels, image size up to 1280x1024
- Supports H.263 Profile 0 Level 10-70
- Supports JPEG baseline image size up to 4672x3504
- Supports cropping and rotation (90 or 270 degrees) functions

■ Video Decoder

- Supports to decode H.264, SVC, MPEG-4, MPEG-2, MPEG-1, H.263, VC-1, JPEG, RV, VP6 and DivX profile and level for up to 1920x1080
- Supports most of post-processing, up-scaling, down-scaling, dithering, alpha-blending, color conversion, de-interlacing.
- Also supports contrast, brightness, saturation, cropping, digital zoom, picture in picture, image rotation etc.

■ 3D Graphic Engine

- OpenGL ES 2.0 compliant, including extensions; OpenGL ES1.1; OpenVG 1.1
- IEEE 32-bit floating-point pipeline supports long shader instructions (maximum 256 instruction)
- Up to 256 threads per shader
- Up to 16 programmable Scalable Ultra-threaded, unified vertex and pixel shaders
- FSAA mechanisms: MSAA 4x, high quality FSAA 16x
- Vertex processing supported format: BYTE, UBYTE, SHORT, USHORT, INT, UINT, DEC, UDEC, FLOAT,FLOAT16,D3DCOLOR, FIXED16DOT16
- Up to 8 programmable elements per vertex
- Dependent texture operation with high-performance
- Alpha blending
- Support for 4 vertex shader and 8 pixel shader simultaneous textures

■ 2D Graphic Engine

- Bit blit, stretch blit, pattern blit and fast clear
- Line drawing and Rectangle fill and clear
- Mono expansion for text rendering
- Anti-aliased font support
- ROP2, ROP3, ROP4
- Alpha blending
- 90/180/270 degree rotation and Vertical and Horizontal mirror
- Transparency by monochrome mask, chroma key or pattern mask
- High quality 9-tap filter for scaling
- 32K x 32K coordinate system
- Color space conversion between YUV and RGB for both BT709 and BT601
- Clipping window
- Color Index Input conversion Support
- Filter Blit
- Input Formats: (Only Filter Blit support YUV input)
    - A1R5G5B5
    - A4R4G4B4
    - A8R8G8B8

  - X1R5G5B5
  - X4R4G4B4
  - X8R8G8B8
  - RGB565
  - NV12 (semi-planer YUV420)
  - NV16 (semi-planer YUV422)
  - YUY2(package YUV422)
  - UYVY(package YUV422)
  - YV12(planer YUV420)
  - 8-bit color index
  - 1-bit monochrome
- The output data Formats:
  - A1R5G5B5
  - A4R4G4B4
  - A8R8G8B8
  - X1R5G5B5
  - X4R4G4B4
  - X8R8G8B8
  - RGB565

■ LCD Interface

- Supports Display Bus Interface (DBI) output mode, compliant to the MIPI Alliance Display Bus Interface protocol v2.0
- Supports accessing (including writing and reading) in through mode
- Supports dual LCD panels work at different time(DBI & DBI, DBI&DPI)
- Supports up to 24 bits per pixel (BPP)
- Display size programmable up to 1080p(1920*1080) with configured interlaced or progressed mode
- Supports Display Pixel Interface (DPI) output mode, compliant to the MIPI Alliance Display Pixel Interface protocol V2.0
- Display size programmable up to 1080p(1920 x1080) with configured interlaced or progressed mode;
- Support for 12 & 16&18BPP&24BPP modes for RGB parallel output format (RGB444 , RGB565, RGB666,RGB888);
- Support programmable pixel clock and asynchronous reset signal ;
- Support flexible 3-wire and 4-wire serial interface(including write operation and read operation of panel registers)
- Support parallel dpi interface with up to 24 bits interface;
- Support CCIR656 interface (PAL mode and NTSC mode, 8 bit interface only);
- Support CCIR601 interface.
- Support UPS051&UPS052 interface (8 bit interface only).
- Support 24BPP modes for UPS051&UPS052 interface.

- Support 16BPP modes for CCIR656 and 24BPP modes for CCIR601.
- Programmable 24-bit/18-bit/16-bit/12-bit/8-bit digital output interface
- Supports various RGB format (RGB888, RGB565, RGB666, RGB555), YUV format (YUV444, YUV422) with 1X, 2X, 3X, 4X multiplexed output.
- Support Max pixel rate up to 150MHz in DPI mode

■ TV Encoder

- Support NTSC-M/J/4.43 and PAL- /B/D/G/H/M/N/I/Nc SDTV Composite signal (480i/576i) output.
- Support YPbPr analog signals output on 480i /480p /576i /576p /720p /1080i /1080p systems
- Embedded with 10 bits Video DAC for analog signal output

2.6 Storage Subsystem

■ NAND Flash Controller

- Compliant to open NAND Flash Interface (ONFI) 1.0 Specification
- Hardware BCH (Bose, Chaudhuri & Hocquenghem Type of code) encoder and decoder are included
- Error detection/correction capability of 4/8/16 bits per 512 bytes
- Error detection/correction capability of 24/32/40/48 bits per 1024 bytes
- 8-bit parallel architecture and calculation based on 1-bit length
- Support SLC, MLC and TLC NAND flash
- Support interlaced storage of ECC and user data
- Support Asynchronous Interface Bus Operation, Clock Frequency 50M for 8-bit interface and Clock Frequency 100M for 16-bit interface
- Support booting from NAND flash with built-in bootloader

■ SDIO Host

- Supports 3 SD IO devices
- Compatible with SD Memory Card Spec 2.0 and supports SDHC up to 32GB card
- Compatible with SDIO Card Spec 2.0
- Compatible with JESD84-A43 standard (MMC 4.3), up to 8-bit data bus
- Support for SD Memory, SDIO, SD Combo, miniSD, MMC, MMC plus, MMC RS and Trans-Flash cards
- Support dual voltage cards typically operating at 1.8V and 3.3V
- Support programmable protocol bus clock for different cards, up to 52MHz

■ USB Host

- High-speed single-port USB host controller. Support one USB downstream port.
- Fully compliant with the USB 2.0 specification, Enhanced Host Controller Interface (EHCI) Specification, Revision 1.0, and the Open Host Controller Interface (OHCI) Specification Release 1.0a.
- Supports high-speed, 480-Mbps transfers using an EHCI Host Controller, as well as full and low speeds through one integrated OHCI Host Controllers.
- The supported peripherals are determined by OS software.
- Also supported: USB-HDD, USB-DVDRW, USB Mouse, USB Keyboard, USB Modem.

■ USB OTG

- USB 2.0 high-speed dual-role controller:
- Operates either as the host/peripheral in point-to-point communications with another USB function or as a function controller for a USB peripheral
- Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
- Supports point-to-point communications with one high-, full- or low-speed device

2.7 Peripheral Subsystem

■ PWM

- Supports up to 2 channels
- The pulse ratio of the output waveform ranges from 0/256 to 255/256
  The frequency of the output waveform ranges from 6KHz to 12MHz

■ UART

- Support 3 UART controllers.
- Functional compatible with the 16550A
- Full-duplex operation.
- Fully programmable serial interface, Data bit: 7-bit or 8-bit, Parity bit: None, Even, Odd, or Stick check, Stop bit: 1-bit or 2-bit.
- Break condition detection and generation.
- Programmable integer and fractional divisor for baud rate generation.
- Programmable Baud rate computation method support up to 12Mbps baud rate.
- Loop-back mode for self test.
- Slow infrared asynchronous interface that conforms to the Infrared Data Association (IrDA) specification.
- Modem control functions with DSR, DCD, RI and DTR signals.

■ SPI

- Support 2 SPI controllers;
- Provide master/slave modes selectable by control registers;
- Full duplex synchronous serial data transfer;
- The max transfer speed in master mode is 54MHz
- The max transfer speed in slave mode is 27MHz

■ I2C

- Master mode only
- Compliant to Philips I2C-Bus Specification v2.1
- Supports for standard mode (up to 100Kbps) and fast mode (up top 400Kbps)
- Support 7-bit and 10-bit device addressing modes
- Max transfer length of each transaction is 65535 for read or write operation
- Arbitration lost detection and bus busy detection

■ Touch Panel Interface

- Master mode only
- Embedded 10-bit SAR ADC: DNL - ±1 LSB, INL - ±2 LSB
- Support control function of resistive 4-wire touch panel
- Support pen down detect
- Support 4-channel analog input measurement
- multi-touch supported in Software including zoom in & out and rotation

■ Audio Codec

- Master mode only
- Contains a high-quality 24-bit stereo ADC and a high-quality 24-bit stereo DAC
- Provides 6 mono differential line inputs with boost gain stage (0/4/8/12/16/20 dB), they can be used either for line in or microphone in application
- Provides 1 stereo single-end 16/32 Ohm headphone output
- Provides 2 mono differential line output that but can't be driven simultaneously
- Provides 1 mono differential BTL 16/32 Ohm receiver output
- Provides a stereo differential speaker output and one of them can also be configured to the mono differential BTL 8 ohm output
- Provides 2 microphone bias output
- Supports audio sampling rates (Fs) from 8KHz to 96KHz (88.2KHz not supported)
- Supports the Automatic Gain Control (AGC) function to better sound recording performances
- Provides 2 I2S/PCM Interfaces of master mode through VC0882 PADs, so as

to connect external devices of slave mode
- Includes two 32-bit stereo digital mixer (produce Y = A + B result)
- Supports 6 memory formats of audio raw data: Stereo-32bit, Stereo-16bit, Stereo-8bit, Mono-32bit, Mono-16bit, and Mono-8bit

2.8 Power Management

- Robust power on/off control and sequence
- AP Software is allowed to control variable voltage output of abundant power supply devices in PMIC via I2C interface.
- AP is partitioned into multi power domains to allow power off of inactive domains and down-scaling of supply voltage when the domain can work with low frequency.
- AP is divided into two Power domains: PMU (always-on domain) & PSO (shut-off domain). PMU power domain includes PMU logic and all digital IO domains. These digital IO should be powered on/off with PMU logic power at the same time, including DDR memory IO. PSO power domain is divided into four voltage domains to support individual power on/off control, down/up scaling of voltage level for each voltage domain depending on applications. These four voltage domains are ARM, GPU, Video Codec, Other Core. Each voltage domain has its own supply from PMIC with variable voltage output.
- AP has the following power modes to support low power design.

Power modes	POWER OFF	NORMAL	IDLE	HALT	SLEEP
PMU domain	Off	On	On	On	On
PSO domain	Off	On	On with ARM clock gating	On With all module clock gating	Off

- Static and dynamic clock gating to decrease dynamic power consumption in AP chip.
- Seamless clock switch to support low power mode in AP chip.
- DVFS(Dynamic Voltage & Frequency Scaling) Technology allows adaptive down/up scaling of clock frequency and voltage level inside one scenario or between scenarios to reduce further dynamic power and also leakage power consumption. Temperature & Process change can also be compensated for by

hardware.

2.9 PAD and PAD Control

- Support 1.7v ~ 3.6v normal digital I/O
- Support 2.4v ~ 3.6v normal analog I/O and 5v special analog I/O
- Support 1.4v ~ 1.9v high-speed MDDR/DDR2/DDR3 I/O
- 4mA/8mA/12mA/16mA drive strength of I/O
- Schmitt trigger input for special signals such as clock, reset
- 16bit strap pins for Software
- Up to 59 GPIO interrupt controllers and 8 Hardware interrupt controllers
- Multi IO power domain to support connecting to external devices with different voltage supply

Chapter 03

Pin Description And Package information

3 Pin Description and Package info

3.1 Ball Map

	1	2	3	4	5	6	7	8	9	10	11
A	DDR_DQS_INV0	DDR_DQM1	DDR_DQ10	DDR_DQ8	DDR_DQ2	DDR_DQ0	SPI0_MISO	SPI0_SCLK	KEYPAD1	KEYPAD0	KEYPAD2
B	DDR_DQM0	DDR_DQS0	DDR_DQ13	DDR_DQ15	DDR_DQ5	DDR_DQ7	SPI0_MOSI	SPI0_SS0N	UART1_SDO	KEYPAD3	KEYPAD6
C	DDR_DQS_INV1	DDR_DQS1	AUD1_SDO_DAC	UART0_SDO	UART1_DCDN	UART1_DSRN	UART1_CTSN	UART1_SDI	KEYPAD4	KEYPAD7	KEYPAD11
D	DDR_DQ12	DDR_DQ11	AUD1_SDI_ADC	AUD1_WS	UART0_SDI	UART1_RIN	UART1_DTRN	UART1_RTSN	KEYPAD5	KEYPAD9	KEYPAD12
E	DDR_DQ14	DDR_DQ9	VDD_IO_DDR	VDD_IO_DDR	AUD1_SCK	PWM0	PWM1	VSS	VSS	VSSA_PLL12_1	VSSA_PLL12_3
F	DDR_DQ4	DDR_DQ6	VDD_IO_DDR	VDD_IO_DDR	VDD_CORE_PMU			AUD0_SDI_ADC	AUD0_WS	AUD0_SDO_DAC	AUD0_SCK
G	DDR_DQ1	DDR_DQ3	VSS	VSS	DDR_VREF						
H	DDR_A3	DDR_A5	VSS	VSS	VSS	DDR_ZQ					
J	DDR_RSTN	DDR_A7	VSS	VSS	VSS	DDR_ODT0			VSS	VSS	VSS
K	DDR_A13	DDR_A9	VSS	VSS	VSS	DDR_BA0			VSS	VSS	VSS
L	DDR_A0	DDR_A2	VSS	VSS	VSS	DDR_CS0N			VSS	VSS	VSS
M	DDR_CLK	DDR_CLK_INV	VSS	VSS	VSS	DDR_CKE0			VSS	VSS	VSS

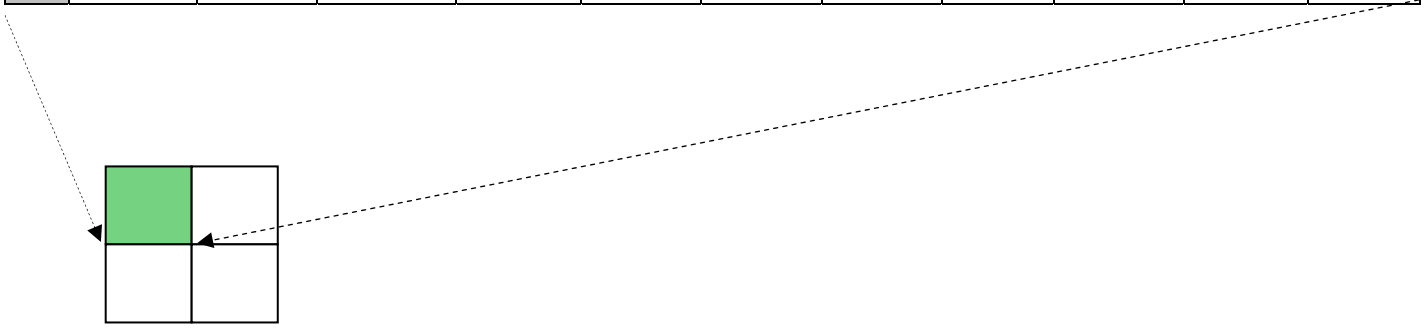

Figure 3-1 Pin Allocation of 445BGA (left-top)

N	DDR_A1	DDR_A12	VSS	VSS	VSS	DDR_RASN			VSS	VSS	VSS
P	DDR_A11	DDR_A10	VSS	VSS	VSS	DDR_CASN			VSS	VSS	VSS
R	DDR_A4	DDR_BA1	VSS	VSS	VSS	DDR_WEN			VSSA_AUD_PA	VSSA_AUD_PA	VSSA_AUD
T	DDR_A8	DDR_A6	VDD_IO_DDR	VDD_IO_DDR	VSS	DDR_BA2					
U	DDR_DQ23	DDR_DQ21	VDD_IO_DDR	VDD_IO_DDR	DDR_ODT1						
V	DDR_DQ16	DDR_DQ18	VDD_CORE_GPU	VDD_CORE_GPU	DDR_CKE1			AUDC_SPKOUTL_P	AUDC_SPKOUTL_N	AUDC_MICBIAS1	USBOTG_RREFEXT
W	DDR_DQ27	DDR_DQ29	DDR_CS1N	DDR_A14	DDR_A15	VSSA_AUD	VSSA_AUD_PA	AUDC_SPKOUTL_P	AUDC_SPKOUTL_N	VSSA_AUD	VSSA_AUD
Y	DDR_DQ25	DDR_DQ31	VDD_CORE_PMU	VDDA_AUD_RCV	VDDA_AUD_OPA	AUDC_LINER2_P	AUDC_LINER1_N	AUDC_SPKOUTR_N	AUDC_HSOUTR	AUDC_VCAP	USBOTG_VBUS
AA	DDR_DQS2	DDR_DQM3	VDD_CORE_PMU	VDDA_AUD_VIN	VDDA_AUD_OPA	VDDA_AUD_VOUT	AUDC_LINER1_P	AUDC_SPKOUTR_P	AUDC_HSOUTL	VDDA_AUD_HP	VDDA_USBHOST33
AB	DDR_DQS_INV2	DDR_DQM2	DDR_DQ28	DDR_DQ30	DDR_DQ19	DDR_DQ22	AUDC_RCVOUT_P	AUDC_LINEL1_P	AUDC_LINEOUT1_N	USBOTG_DPLUS	USBHOST_DPLUS
AC	DDR_DQS3	DDR_DQS_INV3	DDR_DQ24	DDR_DQ26	DDR_DQ20	DDR_DQ17	AUDC_RCVOUT_N	AUDC_LINEL1_N	AUDC_LINEOUT1_P	USBOTG_DMINUS	USBHOST_DMINUS
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**

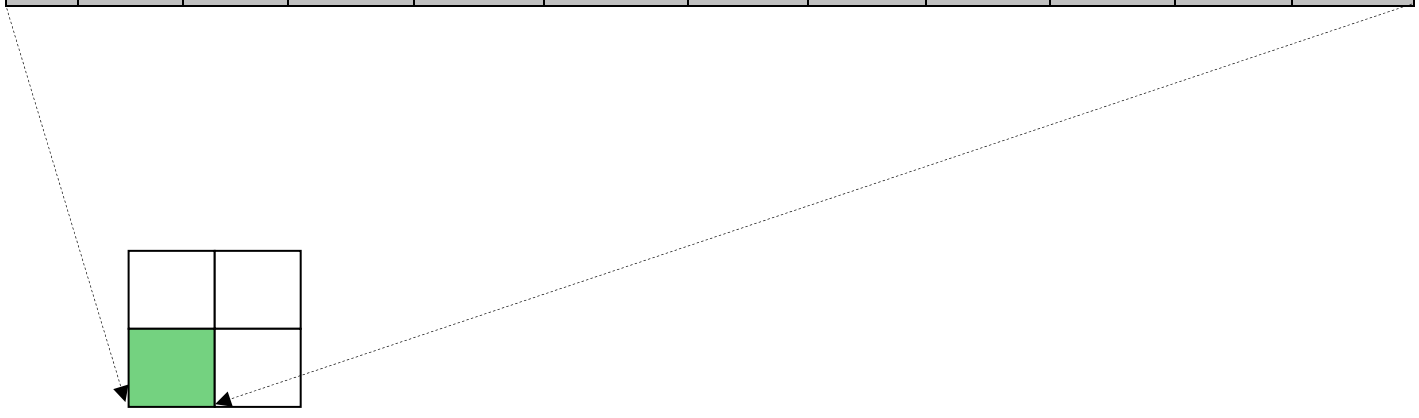

Figure 3-2 Pin Allocation of 445BGA (left-bottom)

12	13	14	15	16	17	18	19	20	21	22	23	
KEYPAD8	I2C_SCK0	X32K_OUT0	X32K_IN	XCLKOUT	XCLKIN	NF_CLE	NF_DATA2	NF_DATA8	NF_CEN2	NF_DATA11	NF_WEN	**A**
KEYPAD10	KEYPAD13	I2C_SCK1	X32K_OUT1	XCLK_OUT0	XCLK_OUT1	NF_CEN1	NF_DATA10	NF_DATA1	NF_DATA3	NF_REN	NF_WPN	**B**
KEYPAD14	I2C_SDA0	PMIC_IRQ	JTG_TDO	JTG_TRSTN	JTG_TCK	NF_CEN0	NF_CEN3	VDD_IO_NF	NF_DATA12	NF_DATA13	NF_RB0	**C**
KEYPAD15	I2C_SDA1	TEST	EN_VDD_CORE	JTG_TMS	JTG_TDI	NF_DATA0	NF_DATA4	NF_DATA9	NF_ALE	NF_DATA14	NF_DATA6	**D**
VSSA_PLL12_4	VSSA_PLL12_2	VSSA_PLL12_5	VSSA_PLL12_6	VDD_IO_SYS	RSTN	VDDA_PLL12_1	VDDA_PLL12_3	VDDA_PLL12_4	NF_DATA5	NF_DATA7	NF_DATA15	**E**
VDD_CORE_ARM	VDD_CORE_ARM	VDD_CORE_ARM	VDD_CORE_ARM	VDD_CORE_ARM			VDDA_PLL12_5	VDDA_PLL12_6	VDDA_PLL12_2	GPIO_J27	GPIO_J28	**F**
							GPIO_A4	GPIO_A2	GPIO_A12	GPIO_J29	GPIO_J30	**G**
						VDD_CORE_PMU	GPIO_A5	GPIO_A3	GPIO_A1	GPIO_A0	SD2_CLK	**H**
VDD_CORE_ARM	VDD_CORE_ARM	VDD_CORE_ARM	VDD_CORE_ARM			VSS	VSS	SD2_DATA0	SD2_CMD	SD2_DATA2	SD2_DATA1	**J**
VSS	VSS	VSS	VSS			VSS	VSS	SD2_DATA3	SD2_DATA4	SD2_DATA5	SD2_RSTN	**K**
VSS	VSS	VSS	VSS			VSS	VSS	SD2_DETECTN	VDD_IO_SD23	SD2_DATA6	SD2_DATA7	**L**
VSS	VSS	VSS	VSS			VDD_CORE_VIDEO	VSS	VDD_IO_LCD	VDD_IO_LCD	LCD_SDA	LCD_RDN	**M**

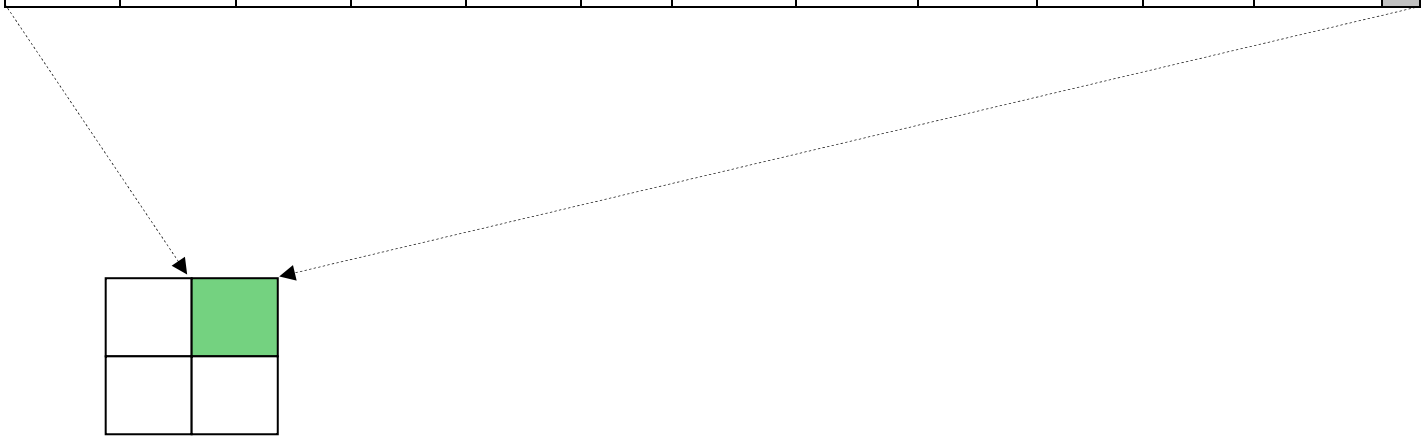

Figure 3-3 Pin Allocation of 445BGA (right-top)

VSS	VSS	VSS	VSS			VDD_CORE_VIDEO	VSS	LCD_DATA18	LCD_DATA23	LCD_DATA13	LCD_DATA21	**N**
VSS	VSS	VSS	VSS			CS_VSYNC	VSS	LCD_DATA12	LCD_DATA14	LCD_DATA16	LCD_SCK	**P**
VSSA_USB	VSSA_USB	VSSA_VDAC	VSSA_VDAC			CS_DATA5	VSS	LCD_DATA5	LCD_DATA10	LCD_WRN	LCD_PCLK	**R**
						CS_DATA6	CS_SDA	LCD_DATA4	LCD_RS	LCD_DATA8	LCD_DATA9	**T**
							TP_VREF	LCD_DATA2	LCD_DATA22	LCD_DATA20	LCD_DATA19	**U**
USBOTG_ID	VDDA_USBOTG33	VDD_CORE_CORE	VDD_CORE_CORE	VDD_CORE_CORE			VSS_TP33	LCD_DATA0	LCD_DATA17	LCD_DATA15	LCD_DATA11	**V**
VSSA_USB	VSSA_USB	VSSA_VDAC	VSSA_VDAC	VDD_EFUSE	VDD_IO_SD01	TP_KEYSCAN	VSSA_TP33	LCD_CS0N	LCD_DATA6	LCD_DATA7	LCD_DATA3	**W**
USBHOST_RREFEXT	VDAC_OUTG	VDAC_OUTB	SD0_DATA1	SD1_DATA1	SD1_CMD	TP_BAT_TEMP	VDDA_TP33	CS_RSTN0	CS_PWD0	LCD_DATA1	LCD_RST0N	**Y**
VDAC_VREFIN	VDAC_OUTR	VDAC_RSET	SD1_DATA0	SD1_DATA2	SD1_DATA3	TP_BAT_ID	VDD_TP33	VDD_IO_CS	CS_HSYNC	CS_DATA7	CS_SCK	**AA**
VDAC_COMP	VDD_VDAC	SD0_CMD	SD0_DATA0	SD0_DATA2	SD1_DETECTN	TP_XINP	TP_YINP	CS_DATA1	CS_DATA0	CS_DATA3	CS_CLK	**AB**
VDAC_VREFOUT	VDDA_VDAC	SD0_CLK	SD0_DETECTN	SD0_DATA3	SD1_CLK	TP_XINN	TP_YINN	TP_BAT_VOLT	CS_DATA4	CS_DATA2	CS_PCLK	**AC**
12	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	

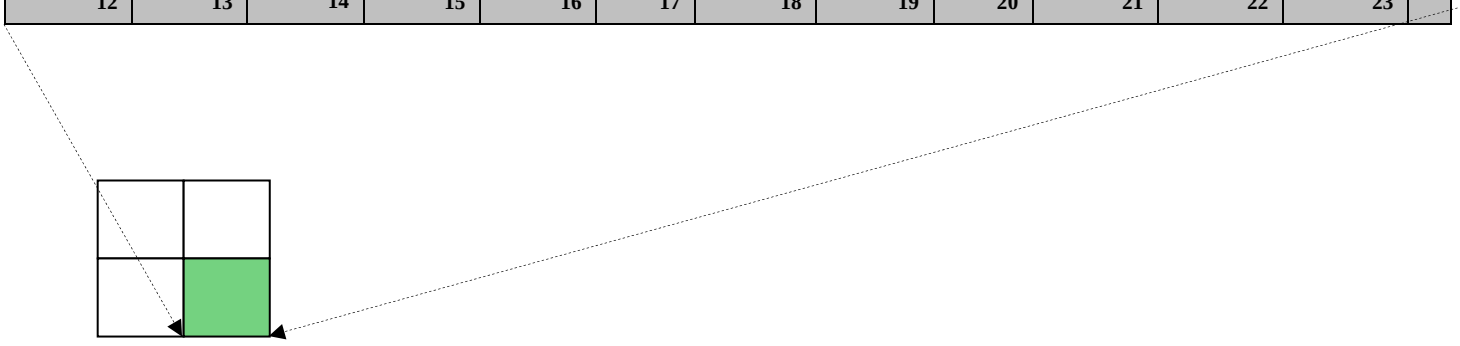

Figure 3-4 Pin Allocation of 445BGA (right-bottom)

3.2 Pin description

Table 3-1 Signal Description of 445BGA

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
RSTN	E17	I,Sh	4	VDD_IO_SYS	I,RSTN	Reset Signal Input
XCLKIN	A17	I,Sh		VDD_IO_SYS	I,XCLKIN	External Crystal Input for System Clock
XCLKOUT	A16	O		VDD_IO_SYS	O,XCLKOUT	External Crystal Ouput for System Clock
X32K_IN	A15	B，Sh, PD	4	VDD_IO_SYS	I,XCLK_32K_IN	External 32.768K Clock Input,**Share** with GPIO_A26
X32K_OUT0	A14	B,PD	8	VDD_IO_SYS	I,GPIO_A22,PD	32.768K Clock Output 0,**Share** with GPIO_A22
X32K_OUT1	B15	B,PD	8	VDD_IO_SYS	I,GPIO_A23,PD	32.768K Clock Output 1,**Share** with GPIO_A23
XCLK_OUT0	B16	B,PD	8	VDD_IO_SYS	I,GPIO_A27,PD	System Clock Output 0,**Share** with GPIO_A27
XCLK_OUT1	B17	B,PD	8	VDD_IO_SYS	I,GPIO_A24,PD	System Clock Output 1,GPIO_A24
TEST	D14	I,PD	4	VDD_IO_SYS	I,TEST	Test Mode Enable
PMIC_IRQ	C14	B,PD	4	VDD_IO_SYS	I,GPIO_A28,PD	Interrupt Source and Wakeup Source from PMIC,**Share** with GPIO_A28
EN_VDD_CORE	D15	B,PD	4	VDD_IO_SYS	O,EN_VDD_CORE	Enable Power Supply To Digital Core, except Video Codec Core and 3D Core,**Share** with GPIO_A29
GPIO_A0	H22	B,PD	8	VDD_IO_SYS	I,GPIO_A0,PD	GPIO_A0,**Share** with NF_CEN8(NAND Chip Enable 8),**Share** with UMOUT0(ASIC debug)
GPIO_A1	H21	B,PD	8	VDD_IO_SYS	I,GPIO_A1,PD	GPIO_A1,**Share** with NF_CEN9(NAND Chip Enable 9),**Share** with UMOUT1(ASIC debug)
GPIO_A2	G20	B,PD	8	VDD_IO_SYS	I,GPIO_A2,PD	GPIO_A2,**Share** with NF_CEN10(NAND Chip Enable 10),**Share** with UMOUT2(ASIC debug)
GPIO_A3	H20	B,PD	8	VDD_IO_SYS	I,GPIO_A3,PD	GPIO_A3,**Share** with NF_CEN11(NAND Chip Enable 11),**Share** with UMOUT3(ASIC debug)
GPIO_A4	G19	B,PU	8	VDD_IO_SYS	I,GPIO_A4,PU	GPIO_A4,**Share** with NF_CEN12(NAND Chip Enable 12),**Share** with UMOUT4(ASIC debug)
GPIO_A5	H19	B,PU	8	VDD_IO_SYS	I,GPIO_A5,PU	GPIO_A5,**Share** with NF_CEN13(NAND Chip Enable 13),**Share** with UMOUT5(ASIC debug)
GPIO_A12	G21	B,PU	8	VDD_IO_SYS	I,GPIO_A12,PU	GPIO_A12,**Share** with SPI0_SS1N(SPI0 Slave Select 1, only in SPI0 Master Mode),UMOUT12(ASIC debug)

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
JTG_TCK	C17	B, PU, Sh	4	VDD_IO_SYS	I,JTG_TCK,PU	JTAG Test Clock,**Share** with GPIO_A17
JTG_TMS	D16	B, PU	4	VDD_IO_SYS	I,JTG_TMS,PU	JTAG Test Mode Select,**Share** with GPIO_A18
JTG_TRSTN	C16	B, PD, Sh	4	VDD_IO_SYS	I,JTG_TRSTN,PD	JTAG Test Reset,**Share** with GPIO_A19
JTG_TDI	D17	B, PU	4	VDD_IO_SYS	I,JTG_TDI,PU	JTAG Test Data Input,**Share** with GPIO_A20
JTG_TDO	C15	B, PU	4	VDD_IO_SYS	B,JTG_TDO	JTAG Test Data Output,**Share** with GPIO_A21
PWM0	E6	B,PD	4	VDD_IO_SYS	I,GPIO_C0,PD	PWM0 output,**Share** with GPIO_C0
PWM1	E7	B,PD	4	VDD_IO_SYS	I,GPIO_C1,PD	PWM1 output,**Share** with GPIO_C1
I2C_SCK0	A13	B, PU	8	VDD_IO_SYS	I,GPIO_C16,PU	I2C0 Serial Clock,**Share** with GPIO_C16
I2C_SDA0	C13	B, PU	8	VDD_IO_SYS	I,GPIO_C17,PU	I2C0 Serial Data,**Share** with GPIO_C17
I2C_SCK1	B14	B, PU	8	VDD_IO_SYS	I,GPIO_C18,PU	I2C1 Serial Clock,**Share** with GPIO_C18
I2C_SDA1	D13	B, PU	8	VDD_IO_SYS	I,GPIO_C19,PU	I2C1 Serial Data,**Share** with GPIO_C19
UART0_SDO	C4	B, PU	4	VDD_IO_SYS	I,GPIO_C2,PU	UART0 Serial Data Output,**Share** with GPIO_C2
UART0_SDI	D5	B, PU	4	VDD_IO_SYS	I,GPIO_C3,PU	UART0 Serial Data Input,**Share** with GPIO_C3
UART1_DSRN	C6	B, PU	4	VDD_IO_SYS	I,GPIO_C4,PU	UART1 Data Set Ready,**Share** with UART3_SDO(UART3 Serial Data Output),**Share** with GPIO_C4
UART1_DCDN	C5	B, PU	4	VDD_IO_SYS	I,GPIO_C5,PU	UART1 Data Carrier Detect,**Share** with UART3_SDI(UART3 Serial Data Input),**Share** with GPIO_C5
UART1_RIN	D6	B, PU	4	VDD_IO_SYS	I,GPIO_C6,PU	UART1 Ring Indicator,**Share** with UART3_CTSN(UART3 Clear to Send),**Share** with GPIO_C6

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
UART1_DTRN	D7	B, PD	4	VDD_IO_SYS	I,GPIO_C7,PD	UART1 Data Terminal Ready,**Share** with UART3_RTSN(UART3 Request to Send),**Share** with GPIO_C7
UART1_CTSN	C7	B, PU	4	VDD_IO_SYS	I,GPIO_C8,PU	UART1 Clear to Send,**Share** with GPIO_C8
UART1_RTSN	D8	B, PD	4	VDD_IO_SYS	I,GPIO_C9,PD	UART1 Request to Send,**Share** with GPIO_C9
UART1_SDO	B9	B, PU	4	VDD_IO_SYS	I,GPIO_C10,PU	UART1 Serial Data Output,**Share** with GPIO_C10
UART1_SDI	C8	B, PU	4	VDD_IO_SYS	I,GPIO_C11,PU	UART1 Serial Data Input,**Share** with GPIO_C11
SPI0_SCLK	A8	B, PU	12	VDD_IO_SYS	I,GPIO_C20,PU	SPI0 Serial Clock,**Share** with GPIO_C20
SPI0_SS0N	B8	B, PU	8	VDD_IO_SYS	I,GPIO_C21,PU	SPI0 Slave Select 0,**Share** with GPIO_C21
SPI0_MOSI	B7	B, PU	8	VDD_IO_SYS	I,GPIO_C22,PU	SPI0 Master Out Slave In,**Share** with GPIO_C22
SPI0_MISO	A7	B, PU	8	VDD_IO_SYS	I,GPIO_C23,PU	SPI0 Master In Slave Out,**Share** with GPIO_C23
KEYPAD0	A10	B,PU	4	VDD_IO_SYS	I,GPIO_D0,PU	Keypad 0,**Share** with TRACE_DATA0(Trace data0 for ARM debug),**Share** with UMOUT16(ASIC debug),**Share** with GPIO_D0
KEYPAD1	A9	B,PU	4	VDD_IO_SYS	I,GPIO_D1,PU	Keypad 1,**Share** with TRACE_DATA1(Trace data1 for ARM debug),**Share** with UMOUT17(ASIC debug),**Share** with GPIO_D1
KEYPAD2	A11	B,PU	4	VDD_IO_SYS	I,GPIO_D2,PU	Keypad 2,**Share** with TRACE_DATA2(Trace data2 for ARM debug),**Share** with UMOUT18(ASIC debug),**Share** with GPIO_D2
KEYPAD3	B10	B,PU	4	VDD_IO_SYS	I,GPIO_D3,PU	Keypad 3,**Share** with TRACE_DATA3(Trace data3 for ARM debug),**Share** with UMOUT19(ASIC debug),**Share** with GPIO_D3
KEYPAD4	C9	B,PU	4	VDD_IO_SYS	I,GPIO_D4,PU	Keypad 4,**Share** with TRACE_DATA4(Trace data4 for ARM debug),**Share** with UMOUT20(ASIC debug),**Share** with GPIO_D4

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
KEYPAD5	D9	B,PU	4	VDD_IO_SYS	I,GPIO_D5,PU	Keypad 5,**Share** with TRACE_DATA5(Trace data5 for ARM debug),**Share** with UMOUT21(ASIC debug),**Share** with GPIO_D5
KEYPAD6	B11	B,PU	4	VDD_IO_SYS	I,GPIO_D6,PU	Keypad 6,**Share** with TRACE_DATA6(Trace data6 for ARM debug),**Share** with UMOUT22(ASIC debug),**Share** with GPIO_D6
KEYPAD7	C10	B,PU	4	VDD_IO_SYS	I,GPIO_D7,PU	Keypad 7,**Share** with TRACE_DATA7(Trace data7 for ARM debug),**Share** with UMOUT23(ASIC debug),**Share** with GPIO_D7
KEYPAD8	A12	B,PU	4	VDD_IO_SYS	I,GPIO_D8,PU	Keypad 8,**Share** with TRACE_DATA8(Trace data8 for ARM debug),**Share** with UMOUT24ASIC debug),**Share** with GPIO_D8
KEYPAD9	D10	B,PU	4	VDD_IO_SYS	I,GPIO_D9,PU	Keypad 9,**Share** with TRACE_DATA9(Trace data9 for ARM debug),**Share** with UMOUT25(ASIC debug),**Share** with GPIO_D9
KEYPAD10	B12	B,PU	4	VDD_IO_SYS	I,GPIO_D10,PU	Keypad 10,**Share** with TRACE_DATA10(Trace data10 for ARM debug),**Share** with UMOUT26(ASIC debug),**Share** with GPIO_D10
KEYPAD11	C11	B,PU	4	VDD_IO_SYS	I,GPIO_D11,PU	Keypad 11,**Share** with TRACE_DATA11(Trace data11 for ARM debug),**Share** with UMOUT27(ASIC debug),**Share** with GPIO_D11
KEYPAD12	D11	B,PU	4	VDD_IO_SYS	I,GPIO_D12,PU	Keypad 12,**Share** with TRACE_DATA12(Trace data12 for ARM debug),**Share** with UMOUT28(ASIC debug),**Share** with GPIO_D12
KEYPAD13	B13	B,PU	4	VDD_IO_SYS	I,GPIO_D13,PU	Keypad 13,**Share** with TRACE_DATA13(Trace data13 for ARM debug),**Share** with UMOUT29(ASIC debug),**Share** with GPIO_D13
KEYPAD14	C12	B,PU	4	VDD_IO_SYS	I,GPIO_D14,PU	Keypad 14,**Share** with TRACE_DATA14(Trace data14 for ARM debug),**Share** with UMOUT30(ASIC debug),**Share** with GPIO_D14
KEYPAD15	D12	B,PU	4	VDD_IO_SYS	I,GPIO_D15,PU	Keypad 15,**Share** with TRACE_DATA15(Trace data15 for ARM debug),**Share** with UMOUT31(ASIC debug),**Share** with GPIO_D15
AUD0_SCK	F11	B,PD	8	VDD_IO_SYS	I,GPIO_D17,PD	Audio0 Bit Clock,**Share** with GPIO_D17

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
AUD0_WS	F9	B, PD	4	VDD_IO_SYS	I,GPIO_D18,PD	Audio0 Word Select For Both ADC & DAC,**Share** with GPIO_D18
AUD0_SDI_ADC	F8	B, PD	4	VDD_IO_SYS	I,GPIO_D19,PD	Audio0 Serial Data Input From ADC,**Share** with GPIO_D19
AUD0_SDO_DAC	F10	B, PD	4	VDD_IO_SYS	I,GPIO_D20,PD	Audio0 Serial Data Output to DAC,**Share** with GPIO_D20
AUD1_SCK	E5	B, PD	8	VDD_IO_SYS	I,GPIO_D22,PD	Audio1 Bit Clock,**Share** with GPIO_D22
AUD1_WS	D4	B, PD	4	VDD_IO_SYS	I,GPIO_D23,PD	Audio1 Word Select For Both ADC & DAC,**Share** with GPIO_D23
AUD1_SDI_ADC	D3	B, PD	4	VDD_IO_SYS	I,GPIO_D24,PD	Audio1 Serial Data Input From ADC,**Share** with GPIO_D24
AUD1_SDO_DAC	C3	B, PD	4	VDD_IO_SYS	I,GPIO_D25,PD	Audio1 Serial Data Output to DAC,**Share** with GPIO_D25
CS_DATA0	AB21	B, PD	4	VDD_IO_CS	I,GPIO_H0,PD	Sensor Data 0,**Share** with GPIO_H0
CS_DATA1	AB20	B, PD	4	VDD_IO_CS	I,GPIO_H1,PD	Sensor Data 1,**Share** with GPIO_H1
CS_DATA2	AC22	B, PD	4	VDD_IO_CS	I,GPIO_H2,PD	Sensor Data 2,**Share** with GPIO_H2
CS_DATA3	AB22	B, PD	4	VDD_IO_CS	I,GPIO_H3,PD	Sensor Data 3,**Share** with GPIO_H3
CS_DATA4	AC21	B, PD	4	VDD_IO_CS	I,GPIO_H4,PD	Sensor Data 4,**Share** with GPIO_H4
CS_DATA5	R18	B, PD	4	VDD_IO_CS	I,GPIO_H5,PD	Sensor Data 5,**Share** with GPIO_H5
CS_DATA6	T18	B, PD	4	VDD_IO_CS	I,GPIO_H6,PD	Sensor Data 6,**Share** with GPIO_H6
CS_DATA7	AA22	B, PD	4	VDD_IO_CS	I,GPIO_H7,PD	Sensor Data 7,**Share** with GPIO_H7
CS_HSYNC	AA21	B, PD	4	VDD_IO_CS	I,GPIO_H8,PD	Sensor HSYNC Input,**Share** with GPIO_H8
CS_VSYNC	P18	B, PD	4	VDD_IO_CS	I,GPIO_H9,PD	Sensor VSYNC Input,**Share** with GPIO_H9

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
CS_PCLK	AC23	B, PD, Sh	4	VDD_IO_CS	I,GPIO_H10,PD	Sensor Pixel Clock,**Share** with GPIO_H10
CS_CLK	AB23	B, PD	16	VDD_IO_CS	I,GPIO_H11,PD	Sensor Master Clock,**Share** with GPIO_H11
CS_RSTN0	Y20	B, PU	4	VDD_IO_CS	I,GPIO_H12,PU	Sensor0 Reset,**Share** with GPIO_H12
CS_PWD0	Y21	B, PD	4	VDD_IO_CS	I,GPIO_H13,PD	Sensor0 Power Down,**Share** with GPIO_H13
CS_SCK	AA23	B, PU	4	VDD_IO_CS	I,GPIO_H18,PU	Sensor Interface I2C Serial Clock,**Share** with GPIO_H18
CS_SDA	T19	B, PU	4	VDD_IO_CS	I,GPIO_H19,PU	Sensor Interface I2C Serial Data,**Share** with GPIO_H19
LCD_DATA0	V20	B, PD	8	VDD_IO_LCD	I,GPIO_I0,PD	LCD Data 0,**Share** with GPIO_I0
LCD_DATA1	Y22	B, PD	8	VDD_IO_LCD	I,GPIO_I1,PD	LCD Data 1,**Share** with GPIO_I1
LCD_DATA2	U20	B, PD	8	VDD_IO_LCD	I,GPIO_I2,PD	LCD Data 2,**Share** with GPIO_I2
LCD_DATA3	W23	B, PD	8	VDD_IO_LCD	I,GPIO_I3,PD	LCD Data 3,**Share** with GPIO_I3
LCD_DATA4	T20	B, PD	8	VDD_IO_LCD	I,GPIO_I4,PD	LCD Data 4,**Share** with GPIO_I4
LCD_DATA5	R20	B, PD	8	VDD_IO_LCD	I,GPIO_I5,PD	LCD Data 5,**Share** with GPIO_I5
LCD_DATA6	W21	B, PD	8	VDD_IO_LCD	I,GPIO_I6,PD	LCD Data 6,**Share** with GPIO_I6
LCD_DATA7	W22	B, PD	8	VDD_IO_LCD	I,GPIO_I7,PD	LCD Data 7,**Share** with GPIO_I7
LCD_DATA8	T22	B, PD	8	VDD_IO_LCD	I,GPIO_I8,PD	LCD Data 8,**Share** with GPIO_I8
LCD_DATA9	T23	B, PD	8	VDD_IO_LCD	I,GPIO_I9,PD	LCD Data 9,**Share** with GPIO_I9
LCD_DATA10	R21	B, PD	8	VDD_IO_LCD	I,GPIO_I10,PD	LCD Data 10,**Share** with GPIO_I10
LCD_DATA11	V23	B, PD	8	VDD_IO_LCD	I,GPIO_I11,PD	LCD Data 11,**Share** with GPIO_I11

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
LCD_DATA12	P20	B, PD	8	VDD_IO_LCD	I,GPIO_I12,PD	LCD Data 12,**Share** with GPIO_I12
LCD_DATA13	N22	B, PD	8	VDD_IO_LCD	I,GPIO_I13,PD	LCD Data 13,**Share** with GPIO_I13
LCD_DATA14	P21	B, PD	8	VDD_IO_LCD	I,GPIO_I14,PD	LCD Data 14,**Share** with GPIO_I14
LCD_DATA15	V22	B, PD	8	VDD_IO_LCD	I,GPIO_I15,PD	LCD Data 15,**Share** with GPIO_I15
LCD_DATA16	P22	B, PD	8	VDD_IO_LCD	I,GPIO_I16,PD	LCD Data 16,**Share** with GPIO_I16
LCD_DATA17	V21	B, PD	8	VDD_IO_LCD	I,GPIO_I17,PD	LCD Data 17,**Share** with GPIO_I17
LCD_DATA18	N20	B, PD	8	VDD_IO_LCD	I,GPIO_I18,PD	LCD Data 18,**Share** with GPIO_I18
LCD_DATA19	U23	B, PD	8	VDD_IO_LCD	I,GPIO_I19,PD	LCD Data 19,**Share** with GPIO_I19
LCD_DATA20	U22	B, PD	8	VDD_IO_LCD	I,GPIO_I20,PD	LCD Data 20,**Share** with GPIO_I20
LCD_DATA21	N23	B, PD	8	VDD_IO_LCD	I,GPIO_I21,PD	LCD Data 21,**Share** with GPIO_I21
LCD_DATA22	U21	B, PD	8	VDD_IO_LCD	I,GPIO_I22,PD	LCD Data 22,**Share** with GPIO_I22
LCD_DATA23	N21	B, PD	8	VDD_IO_LCD	I,GPIO_I23,PD	LCD Data 23,**Share** with GPIO_I23
LCD_CS0N	W20	B, PU	8	VDD_IO_LCD	I,GPIO_I24,PU	LCD Select 0 for Main Panel (DBI),**Share** with LCD_CSX(LCD Serial Bus Chip Select(DPI)),**Share** with GPIO_I24
LCD_RS	T21	B, PD	8	VDD_IO_LCD	I,GPIO_I26,PD	LCD Register/Data Select (DBI),**Share** with LCD_DE(LCD Data Enable (DPI)),**Share** with GPIO_I26
LCD_WRN	R22	B, PU	8	VDD_IO_LCD	I,GPIO_I27,PU	LCD Write Strobe (DBI),**Share** with LCD_VSYNC(LCD Vertical Sync (DPI)),**Share** with VGA_VSYNC(VGA Vertical Sync),**Share** with GPIO_I27
LCD_RDN	M23	B, PU	8	VDD_IO_LCD	I,GPIO_I28,PU	LCD Read Strobe (DBI),**Share** with LCD_HSYNC(LCD Horizontal Sync (DPI)),**Share** with VGA_HSYNC(VGA Horizontal Sync),**Share** with GPIO_I28
LCD_RST0N	Y23	B, PD	4	VDD_IO_LCD	I,GPIO_I29,PD	LCD Panel Reset 0,**Share** with GPIO_I29

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
LCD_PCLK	R23	B, PD	16	VDD_IO_LCD	I,GPIO_I30,PD	LCD Pixel Clock (DPI),**Share** with GPIO_I30
LCD_SDA	M22	B, PU	4	VDD_IO_LCD	I,GPIO_I31,PU	LCD SPI Serial Bus Data Out (DPI),**Share** with GPIO_I31
LCD_SCK	P23	B, PU	4	VDD_IO_LCD	I,GPIO_H20,PU	LCD SPI Serial Bus Clock (DPI),**Share** with GPIO_H20
SD0_DATA0	AB15	B,PU	8	VDD_IO_SD01	I,GPIO_K0,PU	SDIO0 Card Data 0,**Share** with GPIO_K0
SD0_DATA1	Y15	B,PU	8	VDD_IO_SD01	I,GPIO_K1,PU	SDIO0 Card Data 1,**Share** with GPIO_K1
SD0_DATA2	AB16	B,PU	8	VDD_IO_SD01	I,GPIO_K2,PU	SDIO0 Card Data 2,**Share** with GPIO_K2
SD0_DATA3	AC16	B,PU	8	VDD_IO_SD01	I,GPIO_K3,PU	SDIO0 Card Data 3,**Share** with GPIO_K3
SD0_CLK	AC14	B, PD	16	VDD_IO_SD01	I,GPIO_K4,PD	SDIO0 Card Clock,**Share** with GPIO_K4
SD0_CMD	AB14	B, PU	8	VDD_IO_SD01	I,GPIO_K5,PU	SDIO0 Card Command/Response ,**Share** with GPIO_K5
SD0_DETECTN	AC15	B, PU	4	VDD_IO_SD01	I,GPIO_K6,PU	SDIO0 Card Detect, Low Active,**Share** with GPIO_K6
SD1_DATA0	AA15	B,PU	8	VDD_IO_SD01	I,GPIO_K8,PU	SDIO1 Card Data,**Share** with SPI2_SCLK(SPI2 Serial Clock),**Share** with GPIO_K8
SD1_DATA1	Y16	B,PU	8	VDD_IO_SD01	I,GPIO_K9,PU	SDIO1 Card Data,**Share** with SPI2_SS0N(SP2 Slave Select 0),**Share** with GPIO_K9
SD1_DATA2	AA16	B,PU	8	VDD_IO_SD01	I,GPIO_K10,PU	SDIO1 Card Data,**Share** with SPI2_MOSI(SPI2 Master Out Slave In),**Share** with GPIO_K10
SD1_DATA3	AA17	B,PU	8	VDD_IO_SD01	I,GPIO_K11,PU	SDIO1 Card Data,**Share** with SPI2_MISO(SPI2 Master In Slave Out),**Share** with GPIO_K11
SD1_CLK	AC17	B, PD	16	VDD_IO_SD01	I,GPIO_K12,PD	SDIO1 Card Clock ,**Share** with GPIO_K12
SD1_CMD	Y17	B, PU	8	VDD_IO_SD01	I,GPIO_K13,PU	SDIO1 Card Command / Response ,**Share** with GPIO_K13
SD1_DETECTN	AB17	B, PU	4	VDD_IO_SD01	I,GPIO_K14,PU	SDIO1 Card Detect, Low Active,**Share** with GPIO_K14
SD2_DATA0	J20	B,PU	8	VDD_IO_SD23	I,GPIO_K20,PU	SDIO2 Card Data 0,**Share** with GPIO_K20

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
SD2_DATA1	J23	B,PU	8	VDD_IO_SD23	I,GPIO_K21,PU	SDIO2 Card Data 1,**Share** with GPIO_K21
SD2_DATA2	J22	B,PU	8	VDD_IO_SD23	I,GPIO_K22,PU	SDIO2 Card Data 2,**Share** with GPIO_K22
SD2_DATA3	K20	B,PU	8	VDD_IO_SD23	I,GPIO_K23,PU	SDIO2 Card Data 3,**Share** with GPIO_K23
SD2_DATA4	K21	B,PU	8	VDD_IO_SD23	I,GPIO_K24,PU	SDIO2 Card Data 4,**Share** with GPIO_K24
SD2_DATA5	K22	B,PU	8	VDD_IO_SD23	I,GPIO_K25,PU	SDIO2 Card Data 5,**Share** with GPIO_K25
SD2_DATA6	L22	B,PU	8	VDD_IO_SD23	I,GPIO_K26,PU	SDIO2 Card Data 6,**Share** with GPIO_K26
SD2_DATA7	L23	B,PU	8	VDD_IO_SD23	I,GPIO_K27,PU	SDIO2 Card Data 7,**Share** with GPIO_K27
SD2_CLK	H23	B, PD	16	VDD_IO_SD23	I,GPIO_K16,PD	SDIO2 Card Clock ,**Share** with GPIO_K16
SD2_CMD	J21	B, PU	8	VDD_IO_SD23	I,GPIO_K17,PU	SDIO2 Card Command/Response ,**Share** with GPIO_K17
SD2_RSTN	K23	B,PU	4	VDD_IO_SD23	I,GPIO_K18,PU	SDIO2 Card Reset Signal,**Share** with GPIO_K18
SD2_DETECTN	L20	B, PU	4	VDD_IO_SD23	I,GPIO_K19,PU	SDIO2 Card Detect, **Share** with GPIO_K19
NF_CEN0	C18	B, PU	8	VDD_IO_NF	I,GPIO_J20,PU	NAND Chip Enable 0,**Share** with GPIO_J20
NF_CEN1	B18	B, PU	8	VDD_IO_NF	I,GPIO_J21,PU	NAND Chip Enable 1,**Share** with GPIO_J21
NF_CEN2	A21	B, PU	8	VDD_IO_NF	I,GPIO_J22,PU	NAND Chip Enable 2,**Share** with GPIO_J22
NF_CEN3	C19	B, PU	8	VDD_IO_NF	I,GPIO_J23,PU	NAND Chip Enable 3,**Share** with GPIO_J23
NF_CLE	A18	B, PD	8	VDD_IO_NF	I,GPIO_J16,PD	NAND Command Latch Enable,**Share** with GPIO_J16
NF_ALE	D21	B, PD	8	VDD_IO_NF	I,GPIO_J17,PD	NAND Address Latch Enable,**Share** with GPIO_J17
NF_WEN	A23	B, PU	12	VDD_IO_NF	I,GPIO_J18,PU	NAND Write Enable,**Share** with GPIO_J18

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
NF_REN	B22	B, PU	12	VDD_IO_NF	I,GPIO_J19,PU	NAND Read Enable,**Share** with GPIO_J19
NF_DATA0	D18	B, PU	8	VDD_IO_NF	I,GPIO_J0,PU	NAND Data 0,**Share** with GPIO_J0
NF_DATA1	B20	B, PU	8	VDD_IO_NF	I,GPIO_J1,PU	NAND Data 1,**Share** with GPIO_J1
NF_DATA2	A19	B, PU	8	VDD_IO_NF	I,GPIO_J2,PU	NAND Data 2,**Share** with GPIO_J2
NF_DATA3	B21	B, PU	8	VDD_IO_NF	I,GPIO_J3,PU	NAND Data 3,**Share** with GPIO_J3
NF_DATA4	D19	B, PU	8	VDD_IO_NF	I,GPIO_J4,PU	NAND Data 4,**Share** with GPIO_J4
NF_DATA5	E21	B, PU	8	VDD_IO_NF	I,GPIO_J5,PU	NAND Data 5,**Share** with GPIO_J5
NF_DATA6	D23	B, PU	8	VDD_IO_NF	I,GPIO_J6,PU	NAND Data 6,**Share** with GPIO_J6
NF_DATA7	E22	B, PU	8	VDD_IO_NF	I,GPIO_J7,PU	NAND Data 7,**Share** with GPIO_J7
NF_DATA8	A20	B, PU	8	VDD_IO_NF	I,GPIO_J8,PU	NAND Data 8,**Share** with GPIO_J8
NF_DATA9	D20	B, PU	8	VDD_IO_NF	I,GPIO_J9,PU	NAND Data 9,**Share** with GPIO_J9
NF_DATA10	B19	B, PU	8	VDD_IO_NF	I,GPIO_J10,PU	NAND Data 10,**Share** with GPIO_J10
NF_DATA11	A22	B, PU	8	VDD_IO_NF	I,GPIO_J11,PU	NAND Data 11,**Share** with GPIO_J11
NF_DATA12	C21	B, PU	8	VDD_IO_NF	I,GPIO_J12,PU	NAND Data 12,**Share** with GPIO_J12
NF_DATA13	C22	B, PU	8	VDD_IO_NF	I,GPIO_J13,PU	NAND Data 13,**Share** with GPIO_J13
NF_DATA14	D22	B, PU	8	VDD_IO_NF	I,GPIO_J14,PU	NAND Data 14,**Share** with GPIO_J14
NF_DATA15	E23	B, PU	8	VDD_IO_NF	I,GPIO_J15,PU	NAND Data 15,**Share** with GPIO_J15
NF_WPN	B23	B, PD	8	VDD_IO_NF	I,GPIO_J24,PD	NAND Write Protect,**Share** with GPIO_J24

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
NF_RB0	C23	B, PU	4	VDD_IO_NF	I,GPIO_J25,PU	NAND Ready/Busy 0,**Share** with GPIO_J25
GPIO_J27	F22	B,PU	8	VDD_IO_NF	I,GPIO_J27,PU	GPIO_J27,**Share** with NF_CEN4(NAND Chip Enable 4)
GPIO_J28	F23	B,PU	8	VDD_IO_NF	I,GPIO_J28,PU	GPIO_J28,**Share** with NF_CEN5(NAND Chip Enable 5)
GPIO_J29	G22	B,PU	8	VDD_IO_NF	I,GPIO_J29,PU	GPIO_J29,**Share** with NF_CEN6(NAND Chip Enable 6)
GPIO_J30	G23	B,PU	8	VDD_IO_NF	I,GPIO_J30,PU	GPIO_J30,**Share** with NF_CEN7(NAND Chip Enable 7)
DDR_CS0N	L6	O		VDD_IO_DDR	O,DDR_CS0N	DDR SDRAM Chip Select 0
DDR_CS1N	W3	O		VDD_IO_DDR	O,DDR_CS1N	DDR SDRAM Chip Select 1
DDR_A0	L1	O		VDD_IO_DDR	O,DDR_A0	DDR SDRAM Memory Address 0
DDR_A1	N1	O		VDD_IO_DDR	O,DDR_A1	DDR SDRAM Memory Address 1
DDR_A2	L2	O		VDD_IO_DDR	O,DDR_A2	DDR SDRAM Memory Address 2
DDR_A3	H1	O		VDD_IO_DDR	O,DDR_A3	DDR SDRAM Memory Address 3
DDR_A4	R1	O		VDD_IO_DDR	O,DDR_A4	DDR SDRAM Memory Address 4
DDR_A5	H2	O		VDD_IO_DDR	O,DDR_A5	DDR SDRAM Memory Address 5
DDR_A6	T2	O		VDD_IO_DDR	O,DDR_A6	DDR SDRAM Memory Address 6
DDR_A7	J2	O		VDD_IO_DDR	O,DDR_A7	DDR SDRAM Memory Address 7
DDR_A8	T1	O		VDD_IO_DDR	O,DDR_A8	DDR SDRAM Memory Address 8
DDR_A9	K2	O		VDD_IO_DDR	O,DDR_A9	DDR SDRAM Memory Address 9
DDR_A10	P2	O		VDD_IO_DDR	O,DDR_A10	DDR SDRAM Memory Address 10
DDR_A11	P1	O		VDD_IO_DDR	O,DDR_A11	DDR SDRAM Memory Address 11
DDR_A12	N2	O		VDD_IO_DDR	O,DDR_A12	DDR SDRAM Memory Address 12
DDR_A13	K1	O		VDD_IO_DDR	O,DDR_A13	DDR SDRAM Memory Address 13
DDR_A14	W4	O		VDD_IO_DDR	O,DDR_A14	DDR SDRAM Memory Address 14
DDR_A15	W5	O		VDD_IO_DDR	O,DDR_A15	DDR SDRAM Memory Address 15
DDR_CLK_INV	M2	O		VDD_IO_DDR	O,DDR_CLK_INV	DDR SDRAM Clock Inverse
DDR_CLK	M1	O		VDD_IO_DDR	O,DDR_CLK	DDR SDRAM Clock
DDR_CKE0	M6	O		VDD_IO_DDR	O,DDR_CKE0	DDR SDRAM Clock Enable 0
DDR_CKE1	V5	O		VDD_IO_DDR	O,DDR_CKE1	DDR SDRAM Clock Enable 1
DDR_CASN	P6	O		VDD_IO_DDR	O,DDR_CASN	DDR SDRAM Column Address Select
DDR_RASN	N6	O		VDD_IO_DDR	O,DDR_RASN	DDR SDRAM Row Address Select

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
DDR_WEN	R6	O		VDD_IO_DDR	O,DDR_WEN	DDR SDRAM Write Enable
DDR_DQM0	B1	O		VDD_IO_DDR	O,DDR_DQM0	DDR SDRAM Data Read/Write Mask, Byte 0
DDR_DQM1	A2	O		VDD_IO_DDR	O,DDR_DQM1	DDR SDRAM Data Read/Write Mask, Byte 1
DDR_DQM2	AB2	O		VDD_IO_DDR	O,DDR_DQM2	DDR SDRAM Data Read/Write Mask, Byte 2
DDR_DQM3	AA2	O		VDD_IO_DDR	O,DDR_DQM3	DDR SDRAM Data Read/Write Mask, Byte 3
DDR_BA0	K6	O		VDD_IO_DDR	O,DDR_BA0	DDR SDRAM Bank 0 Access
DDR_BA1	R2	O		VDD_IO_DDR	O,DDR_BA1	DDR SDRAM Bank 1 Access
DDR_BA2	T6	O		VDD_IO_DDR	O,DDR_BA2	DDR SDRAM Bank 2 Access
DDR_DQ0	A6	B		VDD_IO_DDR	B,DDR_DQ0	DDR SDRAM Data 0
DDR_DQ1	G1	B		VDD_IO_DDR	B,DDR_DQ1	DDR SDRAM Data 1
DDR_DQ2	A5	B		VDD_IO_DDR	B,DDR_DQ2	DDR SDRAM Data 2
DDR_DQ3	G2	B		VDD_IO_DDR	B,DDR_DQ3	DDR SDRAM Data 3
DDR_DQ4	F1	B		VDD_IO_DDR	B,DDR_DQ4	DDR SDRAM Data 4
DDR_DQ5	B5	B		VDD_IO_DDR	B,DDR_DQ5	DDR SDRAM Data 5
DDR_DQ6	F2	B		VDD_IO_DDR	B,DDR_DQ6	DDR SDRAM Data 6
DDR_DQ7	B6	B		VDD_IO_DDR	B,DDR_DQ7	DDR SDRAM Data 7
DDR_DQ8	A4	B		VDD_IO_DDR	B,DDR_DQ8	DDR SDRAM Data 8
DDR_DQ9	E2	B		VDD_IO_DDR	B,DDR_DQ9	DDR SDRAM Data 9
DDR_DQ10	A3	B		VDD_IO_DDR	B,DDR_DQ10	DDR SDRAM Data 10
DDR_DQ11	D2	B		VDD_IO_DDR	B,DDR_DQ11	DDR SDRAM Data 11
DDR_DQ12	D1	B		VDD_IO_DDR	B,DDR_DQ12	DDR SDRAM Data 12
DDR_DQ13	B3	B		VDD_IO_DDR	B,DDR_DQ13	DDR SDRAM Data 13
DDR_DQ14	E1	B		VDD_IO_DDR	B,DDR_DQ14	DDR SDRAM Data 14
DDR_DQ15	B4	B		VDD_IO_DDR	B,DDR_DQ15	DDR SDRAM Data 15
DDR_DQ16	V1	B		VDD_IO_DDR	B,DDR_DQ16	DDR SDRAM Data 16
DDR_DQ17	AC6	B		VDD_IO_DDR	B,DDR_DQ17	DDR SDRAM Data 17
DDR_DQ18	V2	B		VDD_IO_DDR	B,DDR_DQ18	DDR SDRAM Data 18
DDR_DQ19	AB5	B		VDD_IO_DDR	B,DDR_DQ19	DDR SDRAM Data 19
DDR_DQ20	AC5	B		VDD_IO_DDR	B,DDR_DQ20	DDR SDRAM Data 20
DDR_DQ21	U2	B		VDD_IO_DDR	B,DDR_DQ21	DDR SDRAM Data 21
DDR_DQ22	AB6	B		VDD_IO_DDR	B,DDR_DQ22	DDR SDRAM Data 22
DDR_DQ23	U1	B		VDD_IO_DDR	B,DDR_DQ23	DDR SDRAM Data 23
DDR_DQ24	AC3	B		VDD_IO_DDR	B,DDR_DQ24	DDR SDRAM Data 24
DDR_DQ25	Y1	B		VDD_IO_DDR	B,DDR_DQ25	DDR SDRAM Data 25
DDR_DQ26	AC4	B		VDD_IO_DDR	B,DDR_DQ26	DDR SDRAM Data 26
DDR_DQ27	W1	B		VDD_IO_DDR	B,DDR_DQ27	DDR SDRAM Data 27

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
DDR_DQ28	AB3	B		VDD_IO_DDR	B,DDR_DQ28	DDR SDRAM Data 28
DDR_DQ29	W2	B		VDD_IO_DDR	B,DDR_DQ29	DDR SDRAM Data 29
DDR_DQ30	AB4	B		VDD_IO_DDR	B,DDR_DQ30	DDR SDRAM Data 30
DDR_DQ31	Y2	B		VDD_IO_DDR	B,DDR_DQ31	DDR SDRAM Data 31
DDR_DQS0	B2	B		VDD_IO_DDR	B,DDR_DQS0	DDR SDRAM Data Strobe,Byte 0
DDR_DQS1	C2	B		VDD_IO_DDR	B,DDR_DQS1	DDR SDRAM Data Strobe,Byte 1
DDR_DQS2	AA1	B		VDD_IO_DDR	B,DDR_DQS2	DDR SDRAM Data Strobe,Byte 2
DDR_DQS3	AC1	B		VDD_IO_DDR	B,DDR_DQS3	DDR SDRAM Data Strobe,Byte 3
DDR_DQS_INV0	A1	B		VDD_IO_DDR	B,DDR_DQS_INV0	DDR SDRAM Data Strobe Inverse,Byte 0
DDR_DQS_INV1	C1	B		VDD_IO_DDR	B,DDR_DQS_INV1	DDR SDRAM Data Strobe Inverse,Byte 1
DDR_DQS_INV2	AB1	B		VDD_IO_DDR	B,DDR_DQS_INV2	DDR SDRAM Data Strobe Inverse,Byte 2
DDR_DQS_INV3	AC2	B		VDD_IO_DDR	B,DDR_DQS_INV3	DDR SDRAM Data Strobe Inverse,Byte 3
DDR_RSTN	J1	O		VDD_IO_DDR	O,DDR_RSTN	DDR SDRAM Reset Signal, only for DDR3
DDR_ODT0	J6	O		VDD_IO_DDR	O,DDR_ODT0	DDR SDRAM On Die Termination 0
DDR_ODT1	U5	O		VDD_IO_DDR	O,DDR_ODT1	DDR SDRAM On Die Termination 1
DDR_ZQ	H6	I		VDD_IO_DDR	I, DDR_ZQ	DDR SDRAM ZQ
VDAC_RSET	AA14	AIO				VDAC External Resistor Connected to Analog Ground of VDAC Bias Circuit
VDAC_OUTR	AA13	AO				VDAC Channal R Output
VDAC_OUTG	Y13	AO				VDAC Channal G Output
VDAC_OUTB	Y14	AO				VDAC Channal B Output
VDAC_VREFIN	AA12	AI				VDAC Reference Voltage Input
VDAC_VREFOUT	AC12	AO				VDAC Reference Voltage Output
VDAC_COMP	AB12	AIO				VDAC Compensation Pin, Connecting External 0.1uF Capacitor to VDAC Analog Power
USBOTG_RREFEXT	V11	AIO				USB OTG External Resistor For Current Reference
USBOTG_DPLUS	AB10	AIO				USB OTG D+ Port
USBOTG_DMINUS	AC10	AIO				USB OTG D- Port

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
USBOTG_ID	V12	AIO				USB OTG ID
USBOTG_VBUS	Y11	AIO				USB OTG VBUS
USBHOST_REREXT	Y12	AIO				USB HOST External Resistor For Current Reference
USBHOST_DPLUS	AB11	AIO				USB HOST D+ Port
USBHOST_DMINUS	AC11	AIO				USB HOST D- Port
AUDC_VCAP	Y10	AO				Internally Generated Common-Mode Voltage Output
AUDC_LINEL1_P	AB8	AI				Left Differential Line 1 Positive Input
AUDC_LINEL1_N	AC8	AI				Left Differential Line 1 Negative Input
AUDC_LINER1_P	AA7	AI				Right Differential Line 1 Positive Input
AUDC_LINER1_N	Y7	AI				Right Differential Line 1 Negative Input
AUDC_LINER2_P	Y6	AI				Right Differential Line 2 Positive Input
AUDC_HSOUTL	AA9	AO				Left Stereo Single-End Headphone Output
AUDC_HSOUTR	Y9	AO				Right Stereo Single-End Headphone Output
AUDC_RCVOUT_P	AB7	AO				Mono Differential Receiver Positive Output
AUDC_RCVOUT_N	AC7	AO				Mono Differential Receiver Negative Output
AUDC_SPKOUTL_P	V8	AO				Left Stereo Differential Speaker Positive Output
AUDC_SPKOUTL_P	W8	AO				Left Stereo Differential Speaker Positive Output
AUDC_SPKOUTL_N	V9	AO				Left Stereo Differential Speaker Negative Output
AUDC_SPKOUTL_N	W9	AO				Left Stereo Differential Speaker Negative Output

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
AUDC_SPKOUTR_P	AA8	AO				Right Stereo Differential Speaker Positive Output
AUDC_SPKOUTR_N	Y8	AO				Right Stereo Differential Speaker Negative Output
AUDC_LINEOUT1_P	AC9	AO				Mono Differential Line 1 Positive Output
AUDC_LINEOUT1_N	AB9	AO				Mono Differential Line 1 Negative Output
AUDC_MICBIAS1	V10	AO				Microphone Bias Voltage Output 1
TP_XINP	AB18	AIO				Touch Panel X Value of Positive End
TP_XINN	AC18	AIO				Touch Panel X Value of Negative End
TP_YINP	AB19	AIO				Touch Panel Y Value of Positive End
TP_YINN	AC19	AIO				Touch Panel Y Value of Negative End
TP_BAT_VOLT	AC20	AI		0 ~ 2.4v		Touch Panel Battery Voltage
TP_BAT_TEMP	Y18	AI		0 ~ 2.4v		Touch Panel Battery Temperature
TP_BAT_ID	AA18	AI		0 ~ 2.4v		Touch Panel Battery ID
TP_KEYSCAN	W18	AI		0 ~ 2.4v		Touch Panel Analog Key Scan In
TP_VREF	U19	AO				Touch Panel Reference Voltage Positive Output
VDDA_VDAC	AC13	PWR		2.25~2.75v or 3.0 ~ 3.6v		VDAC Analog Power for Channel R/G/B
VDD_VDAC	AB13	PWR		2.25~2.75v or 3.0 ~ 3.6v		VDAC Digital Power
VSSA_VDAC	R14	GND		0V		VDAC Analog Ground for Channel R/G/B/Bias Circuit
VSSA_VDAC	R15	GND		0V		VDAC Analog Ground for Channel R/G/B/Bias Circuit
VSSA_VDAC	W14	GND		0V		VDAC Analog Ground for Channel R/G/B/Bias Circuit
VSSA_VDAC	W15	GND		0V		VDAC Analog Ground for Channel R/G/B/Bias Circuit
VDDA_PLL12_1	E18	PWR		1.0v ~1.5v		PLL Analog Power 1

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
VSSA_PLL12_1	E10	GND		0V		PLL Analog Ground 1
VDDA_PLL12_2	F21	PWR		1.0v ~1.5v		PLL Analog Power 2
VSSA_PLL12_2	E13	GND		0V		PLL Analog Ground 2
VDDA_PLL12_3	E19	PWR		1.0v ~1.5v		PLL Analog Power 3
VSSA_PLL12_3	E11	GND		0V		PLL Analog Ground 3
VDDA_PLL12_4	E20	PWR		1.0v ~1.5v		PLL Analog Power 4
VSSA_PLL12_4	E12	GND		0V		PLL Analog Ground 4
VDDA_PLL12_5	F19	PWR		1.0v ~1.5v		PLL Analog Power 5
VSSA_PLL12_5	E14	GND		0V		PLL Analog Ground 5
VDDA_PLL12_6	F20	PWR		1.0v ~1.5v		PLL Analog Power 6
VSSA_PLL12_6	E15	GND		0V		PLL Analog Ground 6
VDDA_USBOTG33	V13	PWR		3.0v ~ 3.6v		USB OTG PHY Analog Power 3.3v
VDDA_USBHOST33	AA11	PWR		3.0v ~ 3.6v		USB PHY Analog Power 3.3v
VSSA_USB	R12	GND		0V		USB PHY Analog Ground
VSSA_USB	R13	GND		0V		USB PHY Analog Ground
VSSA_USB	W12	GND		0V		USB PHY Analog Ground
VSSA_USB	W13	GND		0V		USB PHY Analog Ground
VDDA_TP33	Y19	PWR		3.0v ~ 3.6v		Touch Panel SAR ADC Analog Power

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
VSSA_TP33	W19	GND		0V		Touch Panel SAR ADC Analog Ground
VSSA_AUD	R11	PWR		0v		AUD Ground for Receiver PA, Internal LDO , Headphone & Linein IO
VSSA_AUD	W6	GND		0v		AUD Ground for Receiver PA, Internal LDO , Headphone & Linein IO
VDDA_AUD_HP	AA10	PWR		2.25v ~ 2.75v		AUD 2.5 V Power Supply For Headphone
VSSA_AUD	W10	GND		0v		AUD Ground for Receiver PA ,Internal LDO , Headphone & Linein IO
VSSA_AUD_PA	R9	GND		0v		AUD 3.3 V Ground For Speaker PA & Speaker PA IO
VDDA_AUD_OPA	Y5	PWR		2.7v ~ 3.6v		AUD 3.3 V Power Supply For Speaker PA Macro & Speaker PA IO
VDDA_AUD_OPA	AA5	PWR		2.7v ~ 3.6v		AUD 3.3 V Power Supply For Speaker PA Macro & Speaker PA IO
VSSA_AUD_PA	R10	GND		0v		AUD 3.3 V Ground For Speaker PA & Speaker PA IO
VSSA_AUD_PA	W7	GND		0v		AUD 3.3 V Ground For Speaker PA & Speaker PA IO
VDDA_AUD_RCV	Y4	PWR		2.7v ~ 3.6v		AUD 3.3 V Power Supply For Receiver PA
VSSA_AUD	W11	GND		0v		AUD Ground for Receiver PA ,Internal LDO , Headphone & Linein IO
VDDA_AUD_VIN	AA4	PWR		2.7v ~ 3.6v		AUD 3.3 V Power Supply Input
VDDA_AUD_VOUT	AA6	AO		2.25v ~ 2.75v		AUD 2.5V internal LDO Output
VDD_CORE_ARM	F12	PWR		1.0v ~1.5v		ARM Core Digital Power
VDD_CORE_ARM	F13	PWR		1.0v ~1.5v		ARM Core Digital Power
VDD_CORE_ARM	F14	PWR		1.0v ~1.5v		ARM Core Digital Power
VDD_CORE_ARM	F15	PWR		1.0v ~1.5v		ARM Core Digital Power

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
VDD_CORE_ARM	F16	PWR		1.0v ~1.5v		ARM Core Digital Power
VDD_CORE_ARM	J12	PWR		1.0v ~1.5v		ARM Core Digital Power
VDD_CORE_ARM	J13	PWR		1.0v ~1.5v		ARM Core Digital Power
VDD_CORE_ARM	J14	PWR		1.0v ~1.5v		ARM Core Digital Power
VDD_CORE_ARM	J15	PWR		1.0v ~1.5v		ARM Core Digital Power
VDD_CORE_VIDEO	M18	PWR		1.0v ~1.5v		Video Core Power
VDD_CORE_VIDEO	N18	PWR		1.0v ~1.5v		Video Core Power
VDD_CORE_GPU	V3	PWR		1.0v ~1.5v		GPU Core Power
VDD_CORE_GPU	V4	PWR		1.0v ~1.5v		GPU Core Power
VDD_CORE_CORE	V14	PWR		1.0v ~1.5v		Shutdown Domain Core Digital Power except ARM, Video Codec & GPU
VDD_CORE_CORE	V15	PWR		1.0v ~1.5v		Shutdown Domain Core Digital Power except ARM, Video Codec & GPU
VDD_CORE_CORE	V16	PWR		1.0v ~1.5v		Shutdown Domain Core Digital Power except ARM, Video Codec & GPU
VDD_CORE_PMU	F5	PWR		1.0v ~1.5v		PMU Domain Core Logic Digital Power and ALL DIGITAL I/O Core Power
VDD_CORE_PMU	H18	PWR		1.0v ~1.5v		PMU Domain Core Logic Digital Power and ALL DIGITAL I/O Core Power
VDD_CORE_PMU	Y3	PWR		1.0v ~1.5v		PMU Domain Core Logic Digital Power and ALL DIGITAL I/O Core Power
VDD_CORE_PMU	AA3	PWR		1.0v ~1.5v		PMU Domain Core Logic Digital Power and ALL DIGITAL I/O Core Power
VDD_IO_SYS	E16	PWR		2.6v ~ 3.0v		SYS I/O Digital Power
VDD_IO_LCD	M20	PWR		1.7v ~ 3.6v		LCD I/O Digital Power

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
VDD_IO_LCD	M21	PWR		1.7v ~ 3.6v		LCD I/O Digital Power
VDD_IO_NF	C20	PWR		1.7v ~ 3.6v		NAND Flash I/O Digital Power
VDD_IO_SD01	W17	PWR		1.7v ~ 3.6v		SDIO 0/1 I/O Digital Power
VDD_IO_SD23	L21	PWR		1.7v ~ 3.6v		SDIO 2/3 I/O Digital Power
VDD_IO_CS	AA20	PWR		1.7v ~ 3.6v		Camera Sensor I/O Digital Power
VDD_IO_DDR	E3	PWR		1.7v ~ 1.95v 1.425 ~ 1.575v		DDR PHY I/O Power
VDD_IO_DDR	E4	PWR		1.7v ~ 1.95v 1.425 ~ 1.575v		DDR PHY I/O Power
VDD_IO_DDR	F3	PWR		1.7v ~ 1.95v 1.425 ~ 1.575v		DDR PHY I/O Power
VDD_IO_DDR	F4	PWR		1.7v ~ 1.95v 1.425 ~ 1.575v		DDR PHY I/O Power
VDD_IO_DDR	T3	PWR		1.7v ~ 1.95v 1.425 ~ 1.575v		DDR PHY I/O Power
VDD_IO_DDR	T4	PWR		1.7v ~ 1.95v 1.425 ~ 1.575v		DDR PHY I/O Power
VDD_IO_DDR	U3	PWR		1.7v ~ 1.95v 1.425 ~ 1.575v		DDR PHY I/O Power
VDD_IO_DDR	U4	PWR		1.7v ~ 1.95v 1.425 ~ 1.575v		DDR PHY I/O Power
DDR_VREF	G5	PWR		0.5 * VDD_IO_DDR		DDR PHY SSTL Reference Power

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
VDD_EFUSE	W16	PWR		2.25 ~ 2.75v		On-chip Efuse Cell Power
VDD_TP33	AA19	PWR		3.0v ~ 3.6v		Touch Panel SAR ADC 3.3v Digital Power
VSS_TP33	V19	GND		0v		Touch Panel SAR ADC 3.3v Digital Ground
VSS	E8	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	E9	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	G3	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	G4	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	H3	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	H4	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	H5	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	J3	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	J4	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	J5	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	J9	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	J10	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	J11	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	J18	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	J19	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
VSS	K3	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	K4	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	K5	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	K9	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	K10	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	K11	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	K12	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	K13	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	K14	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	K15	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	K18	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	K19	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	L3	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	L4	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	L5	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	L9	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	L10	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	L11	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
VSS	L12	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	L13	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	L14	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	L15	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	L18	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	L19	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	M3	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	M4	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	M5	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	M9	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	M10	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	M11	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	M12	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	M13	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	M14	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	M15	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	M19	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	N3	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
VSS	N4	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	N5	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	N9	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	N10	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	N11	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	N12	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	N13	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	N14	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	N15	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	N19	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	P3	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	P4	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	P5	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	P9	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	P10	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	P11	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	P12	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	P13	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
VSS	P14	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	P15	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	P19	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	R3	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	R4	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	R5	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	R19	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground
VSS	T5	GND		0v		Digital IO & Pre-driver Ground and Digital Core Logic Ground

3.3 Package Information

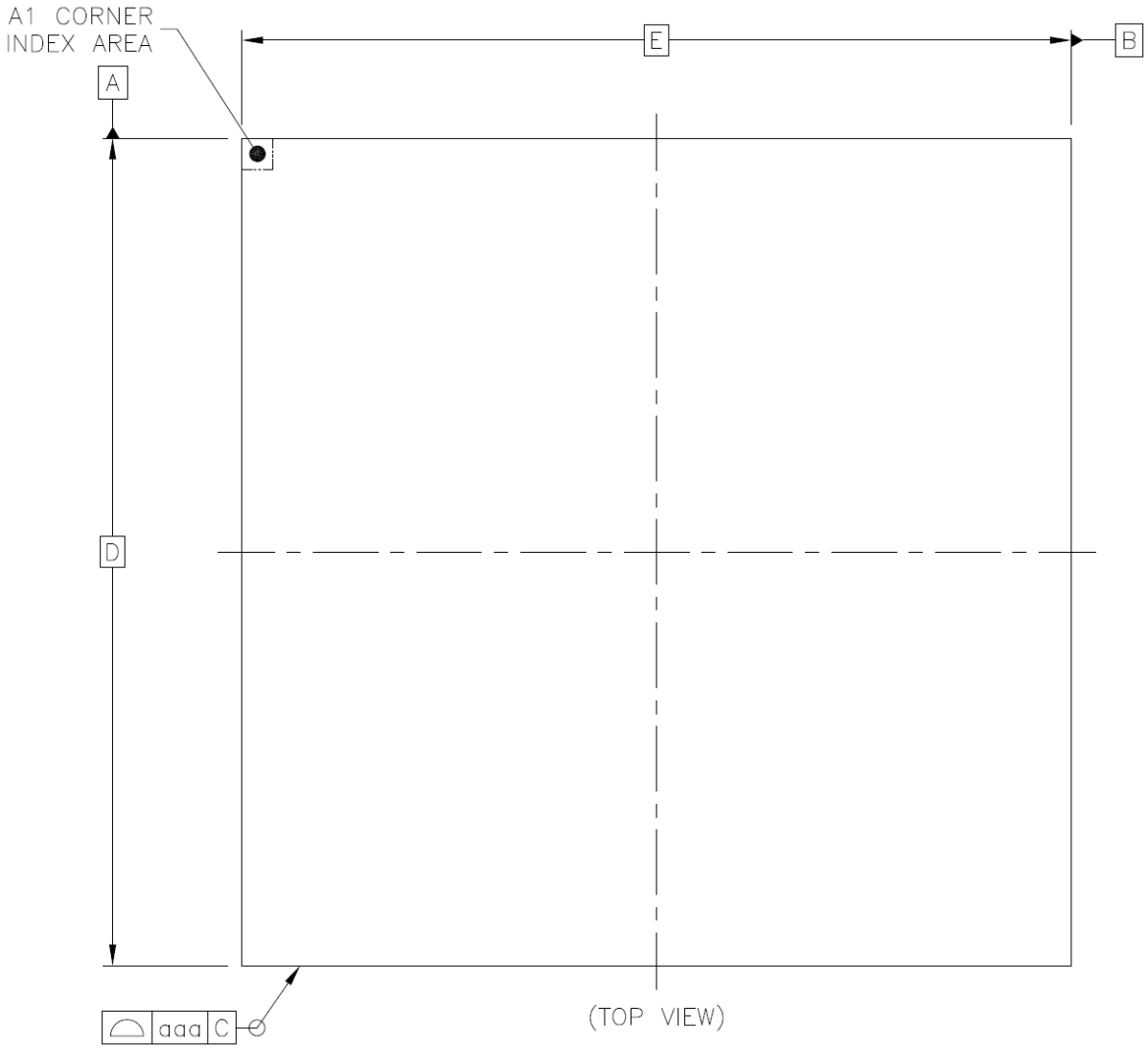

Figure3-5 Top View of 445BGA Package

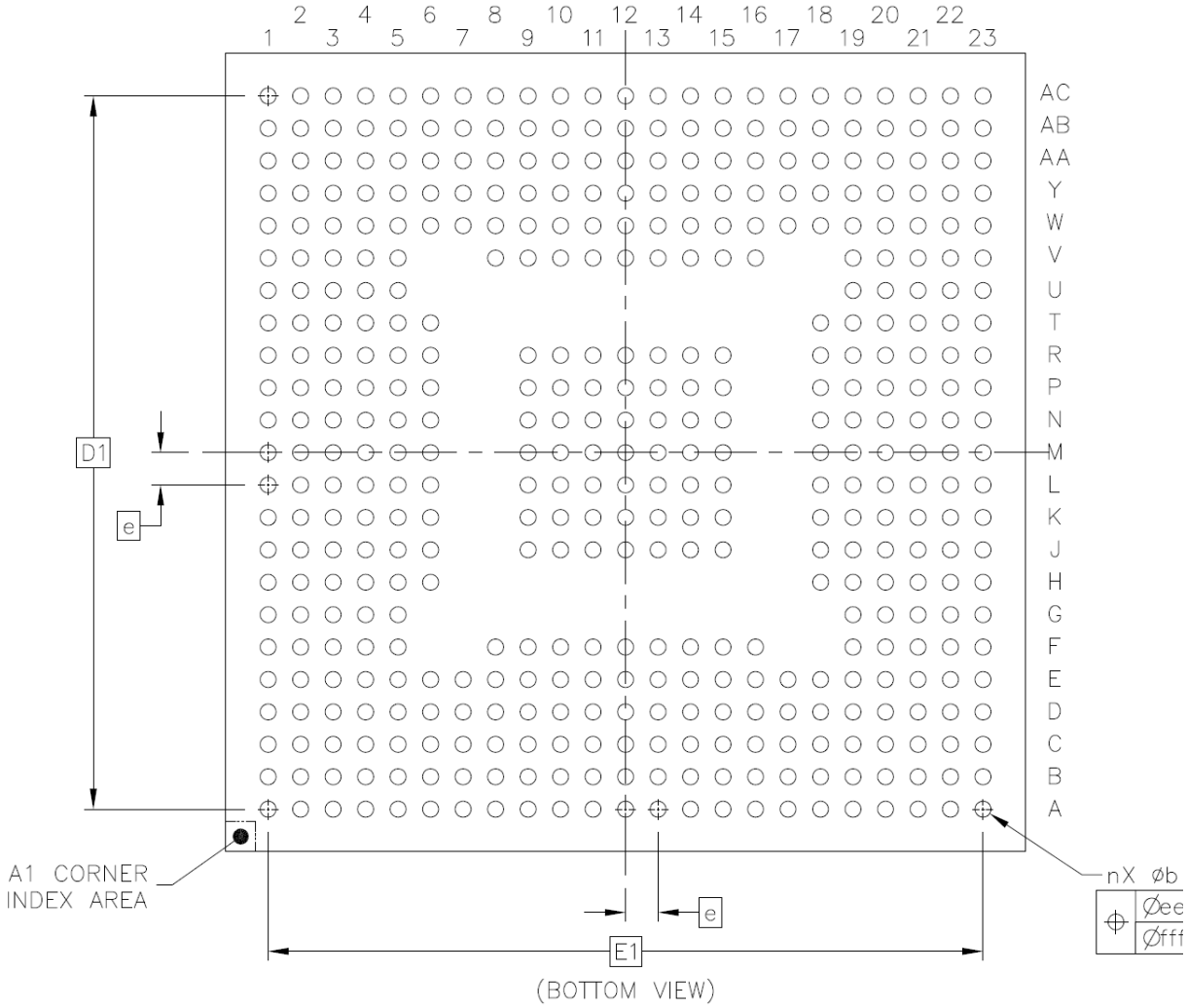

Figure 3-6 Bottom View of 445BGA Package

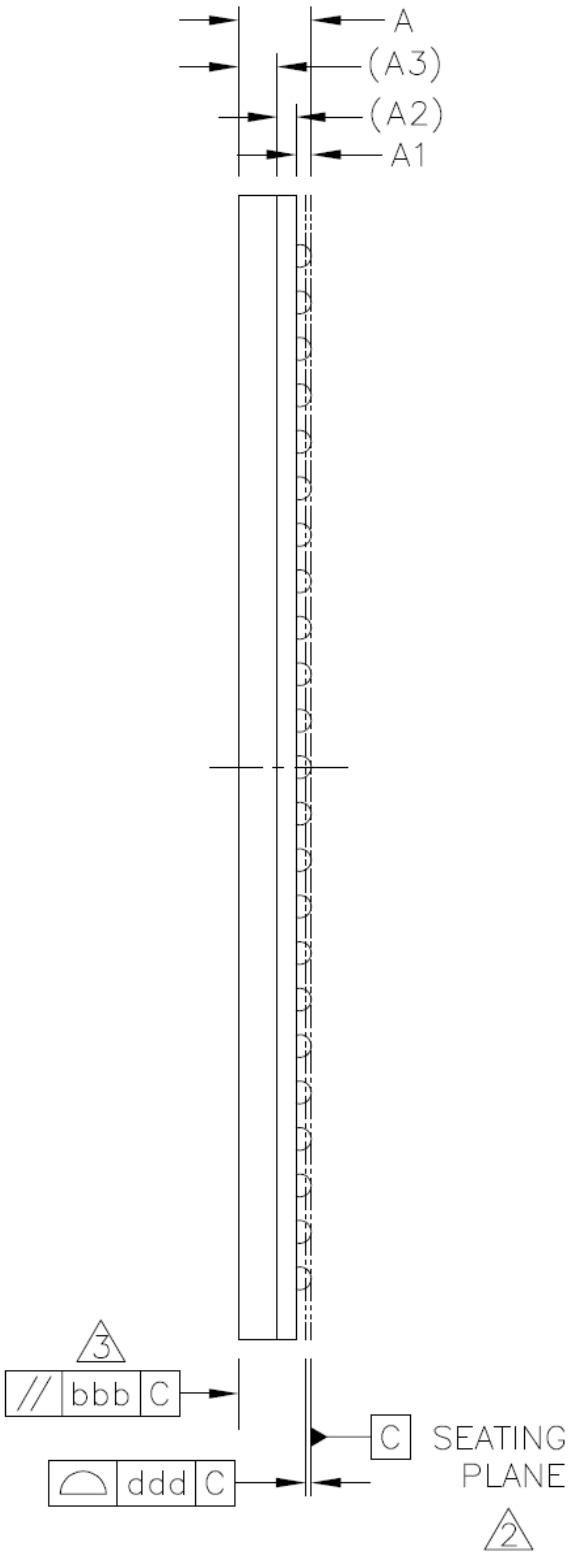

Figure 3-7 Side View of 445BGA Package

Table 3-2 Parameters of 445BGA Package

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.1
STAND OFF	A1	0.16	---	0.26
SUBSTRATE THICKNESS	A2		0.26	REF
MOLD THICKNESS	A3		0.54	REF
BODY SIZE	D		16	BSC
	E		16	BSC
BALL DIAMETER			0.3	
BALL OPENING			0.275	
BALL WIDTH	b	0.27	---	0.37
BALL PITCH	e		0.65	BSC
BALL COUNT	n		445	
EDGE BALL CENTER TO CENTER	D1		14.3	BSC
	E1		14.3	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Chapter 04

CPU SubSystem

4 CPU SubSystem

4.1 CORTEX-A8 Features

The Cortex-A8 processor is a high-performance, low-power, cached application processor that provides full virtual memory capabilities. The features of the processor include:

- Full implementation of the ARM architecture v7-A instruction set
- 64-bit high-speed Advanced Microprocessor Bus
- Architecture (AMBA) with Advanced Extensible Interface (AXI) for main
- memory interface supporting multiple outstanding transactions
- A pipeline for executing ARM integer instructions
- A NEON pipeline for executing Advanced SIMD and VFP instruction sets
- Dynamic branch prediction with branch target address cache, global history buffer, and 8-entry return stack
- Memory Management Unit (MMU) and separate instruction and data Translation
- Look-aside Buffers (TLBs) of 32 entries each
- Level 1 instruction and data caches of 32KB
- Level 2 cache of 128KB
- Level 2 cache with parity and Error Correction Code (ECC) configuration option
- Embedded Trace Macrocell (ETM) support for non-invasive debug
- Static and dynamic power management including Intelligent Energy Management (IEM)
- ARMv7 debug with watchpoint and breakpoint registers and a 32-bit Advanced Peripheral Bus (APB) slave interface to a CoreSight debug system.

CoreSight Sub-system Features

CoreSight systems provide all the infrastructure you require to debug, monitor, and optimize the performance of a complete System on Chip (SoC) design.
There are historically three main ways of debugging an ARM processor based SoC:

- Conventional JTAG debug. This is invasive debug with the core halted using:
  - ✧ breakpoints and watchpoints to halt the core on specific activity
  - ✧ a debug connection to examine and modify registers and memory and provide single-step execution.
- Conventional monitor debug
  This is invasive debug with the core running using a debug monitor that resides in memory.
- Trace

This is non-invasive debug with the core running at full speed using:

- ✧ collection of information on instruction execution and data transfers
- ✧ delivery off-chip in real-time
- ✧ tools to merge data with source code on a development workstation for later analysis.

The CoreSight addresses the requirement for a multi-core debug and trace solution with high bandwidth for whole systems beyond the core, including trace and monitor of the system bus.

The CoreSight provides:

- debug and trace visibility of whole systems
- cross triggering support between SoC subsystems
- higher data compression than previous solutions
- multi-source trace in a single stream
- standard Programmer's Models for standard tool support
- open interfaces for third party cores
- low pin count
- low silicon overhead.

This section describes some of the fundamental features of CoreSight Technology that enable you to address the issues and challenges of debugging complex SoCs. It contains the following sections:

- Debug access

You gain debug access in CoreSight systems through the Debug Access Port (DAP) that provides:

- ✧ real-time access to physical memory without halting the core and without any target resident code
- ✧ debug control and access to all status registers
- ✧ The same mechanism provides fast access for downloading code at the start of the debug session. This is faster than the traditional JTAG mechanism that uses the ARM core to write data to memory.

- Cross Triggering

The Embedded Cross Trigger (ECT), comprising of the Cross Trigger Interface (CTI) and Cross Trigger Matrix (CTM), provides a standard interconnect mechanism to pass debug or profiling events around the SoC.

The ECT provides you with a standard mechanism to connect different signal types. A set of standard triggers for cores and Embedded Trace Macrocells (ETMs) are predefined and you

can add triggers for third party cores。

- Trace

The CoreSight provides components that support a standard infrastructure for the capture and transmission of trace data, combination of multiple data streams by
funneling together, and then output of data to a trace port or storing in an on-chip buffer.
The CoreSight enables:

- ✧ simultaneous trace of asynchronous cores, busses
- ✧ debug and trace of an AMBA 2 AHB bus
- ✧ output of trace data to:
  - ◆ a trace port that can run at an independent frequency
  - ◆ an embedded trace buffer for on-chip storage of trace RAM

support for third party cores to enable debug control and standardized Programmer's Model and infrastructure..

System APB is connected to debug APB bus via APB MUX to enable software running on CORTEX-A8 accessing ETM, CTI and DBG inside CORTEX-A8 and CoreSight Components in CSSYS. Note that Coprocessor read and write instruction can only access part of ETM, CTI and DBG registers in CORTEX-A8.

4.2 Clock and Reset

VC0882 CLKRST Module provides the following features:

- Supports 1 oscillator (or crystal): 12/13/24/26 MHz XCLK
- Embeds 6 high performance, low power TCI PLLs
  - ✧ Divided reference frequency range 146KHz - 1.3GHz
  - ✧ /1 output frequency range 240MHz - 1.3GHz
  - ✧ Reference divider values 1-64
  - ✧ Feedback divider values 1-4096
  - ✧ Output divider values 1, 2-8 (even only)
  - ✧ /1 output multiples of div. reference 1-4096
  - ✧ Output duty cycle (nom, tol) 50%,+/-5% (/1 output), +/-2% (others)
  - ✧ Period jitter (P-P) (max) +/-2.5% output cycle
  - ✧ Input-to-output jitter (P-P) (max) n/a
    (jitter numbers are worst-case estimates with supply and substrate noise levels below -- actual results will be better)
  - ✧ Power dissipation (nom) 3mA @ 600MHz (/1 output)
  - ✧ Reset pulse width (min) 5μs
  - ✧ Reset /1 output frequency range 20MHz - 200MHz
  - ✧ Lock time (min allowed) 500 div. reference cycles
    (actual lock time will be much smaller)

- ✧ Freq. overshoot (full-~/half-~) (max) 40%/50%
- ✧ Area (including isolation) (max) ~0.11mm2

- ✧ Number of PLL supply pkg. pins 1 VDDA, 1 VSSA (preferred)
- ✧ Low freq. supply noise est. (P-P) (max) 10% VDDA
- ✧ Low freq. sub. noise est. (P-P) (max) 10% VDDA
- ✧ Reference input jitter (long-term, P-P) (max) 2% div. reference cycle
- ✧ Reference H/L pulse width (min) 420ps
- ✧ Process technology TSMC CLN65LP 0.065µm
- ✧ Supply voltage (VDD, VDDA) (nom, tol) 1.2V, +/-10%
- ✧ Junction temperature (nom, min, max) 70C, -40C, 125C

- Includes configurable clock dividers to produce desired clock frequencies
- Implements clock gating technology to save power
- Inserts clock multiplexers to enhance flexibility
- Supports system clock switching between XCLK and all 6 PLLs
- Integrates pmu hardware reset, watchdog reset, global software reset and each module's individual software reset

4.3 Interrupt controller

VC0882 adopts two-level interrupt architecture. The second-level interrupt controllers (SLIC Sub-module) are embedded in each module. It collects the module's local interrupts, filters with its mask settings, and then if no mask settings generates a high-level interrupt report to the first-level interrupt controller (FLIC Module).
SLIC Sub-module provides the following features:

- Embedded in each module
- Collects this module's local interrupts, which are sent to SLIC Module in high level pulses of one module clock cycle.
- Holds 1'b1 at some bits in XXX_SRCPND Register, which indicates these kinds of local interrupts have happened, until software writes 1'b1 to clear these bits
- Filters XXX_SRCPND Register with XXX_INTMASK Register, which allows software to mask unconcerned local interrupts
- Provides XXX_SETMASK and XXX_UNMASK Registers, so as to support atom manipulation for XXX_INTMASK Register
- If any 1'b1 in XXX_SRCPND Register has not been masked, generates and holds a high-level interrupt report to FLIC Module

FLIC Module provides the following features:

- Supports up to 64 interrupt sources
- Supports both IRQ and FIQ to ARM

- Specifies the mode of each interrupt source by INTC_INTMODE Register, where none or only one interrupt source may be specified to FIQ Mode
- Separates the interrupt source of FIQ Mode from the others of IRQ Mode, which doesn't affect INTC_INTPND and INTC_INTOFFSET Registers
- Interrupt sources of both IRQ and FIQ Mode can be masked by INTC_INTMASK Register
- Provides INTC_SETMASK and INTC_UNMASK Registers, so as to support atom manipulation for INTC_INTMASK Register
- Performs priority arbitration for interrupt sources of IRQ Mode as follows:
  - ✧ First come first serve
  - ✧ If arrive simultaneously, grant the interrupt source having the highest priority, which is from 0(H) to 15(L) and configured in INTC_PRIORITY Registers
  - ✧ Furthermore, if multiple interrupt sources all have the same highest priority, grant the one having the minimum port number.

- Saves the result of priority arbitration in INTC_INTPND and INTC_INTOFFSET Registers, and the value of INTC_INTOFFSET register accords with INTC_INTPND register.
- Support software interrupt.
- If any 1'b1 in INTC_INTPND Register has not been masked, generates and holds a low-level interrupt report to ARM.

Generally speaking, ARM has 7 processor modes. Three of them are User Mode, IRQ Mode and FIQ Mode. ARM executes most tasks in User Mode. If the pin IRQn of ARM has been pulled down to low level, ARM enters IRQ Mode and usually this mode is used to process some common interrupts. If the pin FIQn of ARM has been pulled down to low level, ARM enters FIQ Mode. Since this mode has been optimized to have fast response speed, it is usually used to process some urgent interrupts.

4.4 Timer

VC0882 timer module supports 8 timers: 3 general-purpose timers, 4 dual timers and 1 watchdog timer. The timers operate from a unique 24MHz timer clock but with separate control signals for each timer, which give flexible controls.
. The VC0882 timer module has the following features:

- 3 general-purpose timers, 4 dual timers and 1 watchdog timer
- Programmable timer period and timer operation mode
- Individual interrupt for each timer
- Unique 24MHz clock for all timers
- 3 operation modes for general-purpose timers:
  - ➢ One-time operation (timer runs for one period then resets and stops)
  - ➢ Periodical operation (timer interrupts and automatically resets every time it reaches

maximum value)
  - Continuous operation (timer interrupts every time it reaches a specific value, then it continues to count)
- 3 operation modes for dual timers:
  - One-time operation (timer runs for one period then resets and stops)
  - Periodic operation (timer interrupts and automatically resets every time it reaches maximum value)
  - Continuous operation (timer interrupts every time it reaches a specific value, then it continues to count)
- watchdog timer is able to used as a general-purpose timer
- Capability of each timer is shown below:

Table 4-1 Timer Capability list

Capability	Timer0	Timer1	Timer2	Timer3	Timer4	Timer5	Timer6	Timer7
32-bit general-purpose timer		X	X					X
Dual 32-bit timer (chained)				X	X	X	X	
64-bit general-purpose timer	X							
Watchdog timer								X

Basically, timer module consists of a register sub-module, 3 general-purpose timers, 4 dual timers and a watchdog sub-module. The timer register sub-module, Timer_reg, is in charge of getting timer options through APB interface and sending the setup to the timers. The general-purpose timer sub-modules will work according to the setup from the register sub-module and generate interrupts to system interrupt controller. Watchdog sub-module is able to act as a watchdog timer for the system as well as a general-purpose timer. It is able to generate a warm reset after an interrupt without CPU clearance.

4.5 EFUSE

The EFUSE module is used to manage electrical fuse IP: program the electrical fuse IP, read programmed values after programming, read all values before programming (named “unload” process) and control this IP in power down or standby mode when it’s inactive.

There are two kinds of ways for above processes(PROGRAM, READ, UNLOAD, POWER_DOWN and STANDBY)：
- by APB bus in normal mode
- by PAD on ATE(automatic test equipment) in test mode

The EFUSE IP is organized as 128-bit by 8 one-time programmable electrical fuses with

random access interface. The EFUSE Module can manage this IP by APB bus in normal work or by PAD inputs in test mode. The electrical fuse is a type of non-volatile memory fabricated in standard COMS logic progress. The electrical fuse macro is widely used in chip ID, memory redundancy, security code, configuration setting, and feature selection, etc.

- There are two kinds of ways to manage the electrical fuse IP. This is selected by TEST pin:
  - ✧ by APB bus in normal mode
  - ✧ by PAD on ATE in test mode
- Software can control the electrical IP into power down or standby mode if the IP is inactive (No PROGRAM, READ and UNLOAD).
- Software can program 1bit at a time according to configured address.
- Software can read 1~8bytes at a time according to configured address and configured read byte length.

The following describes features of EFUSE IP:

- Embedded power-switch
- Provide power-down and standby mode
- Fully compatible with standard CMOS logic process
- Asynchronous signal interface
- Macro requiring both standard-Vt and high-Vt GO1 (Core device) transistors
- Macro also requiring GO2 (I/O device) transistors
- Programming condition:
  VQPS: 2.5+/-10%, VDD: 1.2V+/-10%
  Temp: 125^0C~-40^0C
  Program time: 4us~6us and typical program time is 5us
- Read condition:
  VQPS:2.5V+/-10% or 0V
  VDD=1.2V+/-10%
  Temp: 125^0C~-40^0C
- Provided macro for ESD protection, MUST be used in-pair with this electrical fuse IP

Chapter 05

Memory SubSystem

5 Memory Subsytem

5.1 Interconnection

INTERCONNECT is based on ARM AMBA3 (Advanced Microcontroller Bus Architecture) AXI (Advanced eXtensible Interface) Bus Protocol and connects all the AXI Master Modules and AXI Slave Modules of this chip together. Its main tasks are (1) decoding memory addresses according to the predefined memory mapping table, (2) routing Read Address, Write Address and Write Data from AXI Masters to AXI Slaves, as well as routing Read Data and Write Response from AXI Slaves to AXI Masters, so as to realize the chip-level information interchange, (3) arbitrating if competition exists when routing information from multiple sources to a unique destination.

- Be in compliance with ARM AMBA3 AXI Bus Protocol.
- Construct the INTERCONNECT with Synopsys DesignWare Fabric Components, such as DW_axi, DW_axi_x2x, and DW_axi_hmx.
- DW_axi is instantiated as MARB (Main ARBiter) and SARB (Sub ARBiter). MARB is used to do the top-level integration, while SARB is used to do the module-level or subsystem-level integration. MARB and SARB make up the backbone of this INTERCONNECT.
- Read Data Interleaving is supported.
- Write Data Interleaving is fixed to a depth of 1.
- Exclusive Access and Locked Access are not used, so that ARLOCK[1:0] and AWLOCK[1:0] are fixed to 2'b00.
- Cache Options are not used, so that ARCACHE[3:0] and AWCACHE[3:0] are fixed to 4'b0000.
- Protection Options are not used, so that ARPROT[2:0] and AWPROT[2:0] are fixed to 3'b000.
- Low-Power Interface is not used.
- Read Address Channel and Write Address Channel implement a user-defined arbitration strategy, called Class Based Round Robin + Pulse Width Modulation Arbitration Strategy (CBRR+PWM for short).
- Read Data Channel and Write Response Channel implement the general Round Robin Arbitration Strategy.
- Write Data Channel involves no arbitration because Write Data Interleaving has been fixed to a depth of 1.
- Extend Read Address Channel and Write Address Channel with 2-bit sideband signals respectively, i.e. ARSIDEBAND[1:0] and AWSIDEBAND[1:0], which are then used by the CBRR+PWM Arbitration Strategy.
- Place performance monitors for AXIBUS, ARBITER and DDRC.

5.2 DDR Controller

DDRC is mainly responsible for the following functions:

- As an AXI slave, receiving AXI transaction from AXI master (memory arbiter).
- The received AXI command may be split into two commands according to command split rule. Each AXI command need to be partitioned into one or multiple DDR bursts before it is queued.
- According to reorder rule, rescheduling the DDR commands for improving DDR efficiency.
- According to DDR protocol, write/read data to/from external DDR device.

The DDRC module supports the following features:

- Compatible with JEDEC standard LPDDR1, DDR2, DDR3
- Data rates up to 800 Mb/s (400 MHz) in 65LP
- Compatible with the AMBA 3 AXI protocol
- Compatible with the AMBA 3 APB protocol
- Supported AXI burst types: incremental and wrap
- AXI interface clock asynchronous to the DDRC core clock
- Support the following bus configurations:
  - ✧ AXI Data Bus width : Valid DDR Data Bus width = 2 : 1 (normal mode)
  - ✧ AXI Data Bus width : Valid DDR Data Bus width = 4 : 1 (half data path valid mode: for example, that AXI Data Bus width is 64 bits, DDR Data Bus width is 32, but only 16 bits of DDR Data Bus are valid ,other 16 bits are not used)
- Configurable AXI data bus widths of 64 bits
  - ✧ Corresponds to DDR data bus widths of 32 bits ,respectively
  - ✧ Corresponds to AXI burst size of 4,8,16 bytes, respectively
- Register programmable timing parameters support DDR2/DDR3/LPDDR1 comp- onents from various DRAM vendors
- Register programmable DDR burst length of 2,4 or 8
- Support LPDDR1/DDR2 read/write command interrupt access
- Advanced features such ODT, ZQ Calibration and *additive latency*
- Support for two CSs (chip select) with shared clock pins, command pins, address pins and data pins
- Support for DDR device density ranging from 64Mbit to 8Gbit
- Support 16 bit LPDDR1/DDR2/DDR3 device and 32bit LPDDR1 device
- Support 8 bit DDR2/DDR3 device
- Advanced command re-ordering and scheduling to maximize bus utilization
- Register programmable anti-starvation mechanisms according to SideBand Info- rmation
- Support single Refresh and Speculative Refresh
- Register programmable priority with up to four priorities according to SideBand Info- rmation
- Register programmable address mapping, including mapping based on row or mapping based on bank

- Supports autonomous DDR power down entry and exit based on programmable idle periods
- Support for self refresh entry on software command and automatic exit on DRAM access command arrival
- Automated Read DQS recognition with DDR PHY and Automated Dynamic DQS Drift Compensation
- Built-in DQS Gate Training with DDR PHY
- Support DDR3 DLL-off Mode
- Support LPDDR1 Deep Power Down Mode

5.3 Sram Controller

SRAMC module is the interface between AXI bus and SRAM. It works as an AXI slave as well as a SRAM controller. It receives AXI transactions from AXI bus and transforms them into SRAM control signals. When data come back from SRAM, SRAMC put them into AXI data channel according to AXI protocol.

- The core logic of SRAMC can work at a MAX clock frequency of 200MHz;
- “Rresp” and “Bresp” always be “OKEY”, it means that AXI interconnect must check the correctness of the address;
- AXI interface and core logic are asynchronous;
- AXI data bus width is fixed as 64 bits;
- SRAM data bus width is fixed as 16 bits;
- SRAM adderss width is fixed as 14 bits;
- AMBA AXI protocol related features:
  - Supports “incrementing” and “wrapping” burst type;
  - Supports burst length 1 to 16;
  - Supports narrow transfer;
  - Supports unaligned data transfers;
  - Supports multiple transaction ID;
  - Transactions complete in the order they were received even if they have different transaction ID;
  - “fixed” burst type is not supported;
  - Locked transfer is not supported;
  - Exclusive access is not supported;
  - Write data interleaving is not supported;
  - Low power interface is not supported;
- SRAM side
  - Supports byte write enable;
  - Supports delayed read data using “rdata_valid” input signal;
  - Can hold write command using “wen” signal;

- Can hold read command using “ren” signal;

5.4 Rom Controller

ROMC module is the interface between AXI bus and ROM. It works as an AXI slave as well as a ROM controller. It receives AXI transactions from AXI bus and transforms them into ROM control signals. When data come back from ROM, ROMC put them into AXI data channel according to AXI protocol.

- The core logic of ROMC can work at a MAX clock frequency of 200MHz;
- “Rresp” always be “OKEY”;
- AXI interface and core logic are asynchronous;
- Data bus width is 64 bits;
- Rom address width is 13 bits;
- Data bus width of AXI and memory must be the same;
- AMBA AXI protocol related feature;
  - Accepts only read transactions;
  - Supports “incremental” and “wrap” transaction type;
  - Supports burst length 1 to 16;
  - Supports narrow transfer;
  - Supports unaligned data transfers;
  - Supports multiple transaction ID;
  - Transactions complete in the order they were received even if they have different transaction ID;
  - “fixed” burst type is not supported;
  - Locked transfer is not supported;
  - Exclusive access is not supported;
  - Write data interleaving is not supported;
  - Low power interface is not supported;
- Supports only one ROM;

5.5 DMAC (Direct Memory Access Controller)

The VC0882 DMAC is a high-performance DMA controller. The DMAC is used to setup a direct transfer path between memories. The main advantage of DMA is that it can transfer the data without CPU intervention.

The DMAC supports one channel and only supports software request. You may begin to transfer memory data when the channel is idle. Software mode means ARM initiates the

transmission. DMAC will only give out the interrupt to ARM. Channel registers should be well configured before each transmission.

The VC0882 DMAC has the following features:

- Compliance to the AMBA 3.0 Specification---AXI protocol for integration into SoC implementation.
- One DMA channel which can support unidirectional transfer for software request.
- Memory-to-memory transfer. Supported memories are DDR SDRAM, internal SRAM, external dual port SRAM and external SRAM-like Devices such as Nor Flash or Ethernet Controller.
- Only support linear transfer.
- APB slave DMA programming interface. Software program the DMAC by writing to the DMA control registers over the APB slave interface.
- One AXI bus master for transferring data. Use these interfaces to transfer data when a DMA request goes active.
- Increment addressing for source and destination.
- Internal 32×64bits FIFO (one instance of a sync FIFO).
- Support programming max burst length.
- The source address and destination address for DMA request are byte aligned.
- Transfer length is byte-aligned.
- Transfer length is 8~16M bytes.
- Only little-endian support.
- Support LLI Mode. LLI address is 8byte-aligned (double word aligned) and may be stored in DDR SDRAM, internal SRAM, external dual port SRAM and external SRAM-like Devices such as Nor Flash.
- Indicate a transmission has completed by interrupt.
- Software can terminate transfer by configuring register, a terminate interrupt is used to indicate the termination completed.
- Indicate an error has occurred by an error interrupt. If error occurs, the transmission will not be stopped until all outstanding AXI transfer finished.

Chapter 06

Video SubSystem

6 Video SubSystem

6.1 Video Encoder

Supported standards and tools

The encoder supported standards, profiles and levels are presented in Table 6-1.

Table 6-1 encoder supported standards, profiles and levels

Standard	Profiles	Levels	Notes
H.264	Baseline Profile	Levels 1-3.1	Image size up to 1280x1024. B frame not supported.
MPEG-4	Simple Profile	Levels 0-5	Only simple profile tools are supported.
	Main Profile	Level 4	Image size up to 1280x1024.
H.263	Profile 0	Levels 10-70	Image size up to 1280x1024. Time code extensions not supported.
JPEG	Baseline		Image size up to 4672x3504.

The encoder supported H.264 video tools are shown in Table 6-2.

Table 6-2 encoder supported H.264 tools

Standard	Tools	Encoder support
H.264	Slices	I-Slice and P-Slice.
	Entropy encoding	CAVLC
	Basic	Constrained intra prediction. Maximum MV range +-16 pixels. MV accuracy 1/4 pixels. All block sizes from 4x4 to 16x16 supported. All intra modes supported.
	Number of reference frames	1
	Maximum number of slice groups	1

The encoder supported MPEG-4 video tools are shown in Table 6-3.

Table 6-3 encoder supported MPEG-4 tools

Standard	Tools	Encoder support
MPEG-4	Basic	I-VOP and P-VOP. Maximum MV range +-16 pixels.

		MV accuracy 1/2 pixels. 1 or 4 MV per macro block. DC prediction.
	Error resilience	Video packets. Data partitioning. Reversible VLC.
	Number of reference frames	1
	Quantization	Method 2
	Number of visual objects	1
	Short video header	Yes

The encoder supported H.263 video tools are shown in Table 6-4.

Table 6-4 encoder supported H.263 tools

Standard	Tools	Encoder support
H.263	Basic	I-VOP and P-VOP. Maximum MV range +-16 pixels. MV accuracy 1/2 pixels. 1 MV per macro block.
	Error resilience	GOB
	Number of reference frames	1

Encoding Features

The features of the encoder for each supported standard are different. There are shown as followed.

Table 6-5 H.264 features

Standard	Feature	Encoder support
H.264	Input data format	YCbCr 4:2:0 planar or semi-planar. YCbCr and CbYCrY 4:2:2 interleaved.
	Output data format	H.264 byte or NAL unit stream.
	Supported image size	96x96 to 1280x1024. Step size 4 pixels.
	Maximum frame rate	25 fps at 720x576 for PAL. 30 fps at 720x480 for NSTC. 30 fps at 1280x720. Note. The encoder can support 1280x1024 just at 15 fps.
	Maximum bit rate	10 Mbps.

Notes
1) Internally encoder handles images only in 4:2:0 formats.
2) Actual maximum frame rate will depend on the logic clock frequency and the system bus performance. The given figure 30 fps at 1280x720 requires logic clock frequency of 271 MHz. 15 fps at 1280x1024 requires logic clock frequency of 193 MHz.

Table 6-6 MPEG-4/H.263 features

Standard	Feature	Encoder support
MPEG-4 H.263	Input data format	YCbCr 4:2:0 planar or semi-planar. YCbCr and CbYCrY 4:2:2 interleaved.
	Output data format	MPEG-4/H.263 elementary video stream.
	Supported image size	96x96 to 1280x1024. Step size 4 pixels.
	Maximum frame rate	25 fps at 720x576 for PAL. 30 fps at 720x480 for NSTC. 30 fps at 1280x720. Note. The encoder can support 1280x1024 just at 15 fps.
	Maximum bit rate	10 Mbps.

Notes
1) Internally encoder handles images only in 4:2:0 formats.
2) Actual maximum frame rate will depend on the logic clock frequency and the system bus performance. The given figure 30 fps at 1280x720 requires logic clock frequency of 215 MHz. 15 fps at 1280x1024 requires logic clock frequency of 193 MHz.

Table 6-7 JPEG features

Standard	Feature	Encoder support
JPEG	Input data format	YCbCr 4:2:0 planar or semi-planar. YCbCr and CbYCrY 4:2:2 interleaved.
	Output data format	JFIF file format 1.02. Non-progressive JPEG.
	Supported image size	80x16 to 4672x3504. Step size 4 pixels.
	Maximum bit rate	Up to 28 million pixels per second.
	Thumbnail encoding	JPEG compressed thumbnails supported.

Pre-processing features

Pre-processing is pipelined with encoder and it can be used only with encoder. Pre-processing features are presented in Table below.

Table 6-8 pre-processing features

Feature	Encoder support
Color space conversion	YCbYCr or CbYCrY 4:2:2 Interleaved or semi-planar 4:2:0 to YCbCr 4:2:0.
Cropping	JPEG-from 4672x4672 to any supported encoding size. Video-from 1920x1920 to any supported encoding size.
Rotation	90 or 270 degrees.

Video stabilization features

Digital video stabilization detects and compensates undesired jitter effect on the video (For example, images from camera). Stabilization operates with the two input picture buffers simultaneously.

Video stabilization can be used pipelined with video encoding or in standalone mode when video encoding is disabled.

Video stabilization features are explained as followed.

Table 6-9 video stabilization features

Feature	Encoder support
Maximum stabilization move in pixels for two sequential input video pictures.	+-16 pixels.
Adaptive motion compensation filter.	From 6 to 40 sequential video pictures noticed in unwanted and wanted movement separation.
Offset around stabilized picture.	Minimum 8 pixels in standalone mode. Minimum 16 pixels when pipelined with video encoder. Recommended 64 pixels. Maximum not limited.

Connectivity features

The encoder supports AXI and APB bus interfaces, and different bus width from master interface and slave interface. And restrict maximum burst length on bus interface, and also the endian modes can be separately set for input and output data.

The encoder supports connectivity features presented below.

Table 6-10 connectivity features

Feature	Encoder support

APB slave interface	Yes. 32-bit bus width.
AXI master interface	Yes. 64-bit bus width.
Restricting maximum issued AXI burst length	Yes, to any value between from 1 to 16.
Interrupt method	Polling or level based interrupting.
32-bit little endian	Yes, byte order 3-2-1-0.
32-bit big endian	Yes, byte order 0-1-2-3.
64-bit little endian	Yes, byte order 7-6-5-4-3-2-1-0.
64-bit big endian	Yes, byte order 0-1-2-3-4-5-6-7.
Maxed 32-bit little endian in a 64-bit bus	Yes, byte order 3-2-1-0-7-6-5-4.
Maxed 32-bit big endian in a 64-bit bus	Yes, btye order 4-5-6-7-0-1-2-3.

6.2 Video Decoder

Video standard and profiles

Main standards and profiles description of decoder supported.

Table 6-11 profile and level

Standard	Decoder support
H.264 profile and level	Baseline Profile, levels 1 - 4.1 Main Profile, levels 1 - 4.1 High Profile, levels 1 - 4.1 Support I，P，B frame
SVC profile and level	Scalable Baseline Profile, base layer only Scalable High Profile, base layer only Support I, P, B frame.
MPEG-4 visual profile and level	Simple Profile, levels 0 – 6 Advanced Simple Profile, level 0-5 Support I, P, B frame
MPEG-2 profile and level	Main Profile, low, medium and high levels Support I, P, B frame
MPEG-1 profile and level	Main Profile, low, medium and high levels Support I, P, B frame
H.263 profile and level	Profile 0, levels 10-70. Image size up to 720x576. Support I，P frame.
Sorenson Spark profile and level	Bitstream version 0 and 1
VC-1 profile and level	Simple Profile, low, medium and high levels

	Main Profile, low, medium and high levels Advance Profile, levels 0-3 Support I, P, B frame
JPEG profile and level	Baseline interleaved
RV profile and level	RV8 RV9 RV10 Support I, P, B frame
VP6 profile and level	VP6.0 (Simple Profile) VP6.1 VP6.2 (Advanced Profile)
DivX profile and level	DivX Home Theater Profile Quanlified DivX3 DivX4 DivX5 DivX6

Some special function description:

Table 6-12 special function

Standard	Tool	Decoder support
H.263	Time code extensions	Not supported
H.264	Slice groups (FMO)	If more than one slice group used, SW performs entropy decoding
H.264	Arbitrary slice order	Supported, SW performs entropy decoding
H.264	Redundant slices	Supported, but not utilized; redundant slices are skipped by SW
H.264	Image cropping	Not performed by the decoder, cropping parameters are returned to the application
SVC	Enhancement layers	Not supported
MPEG-4	Data partitioning	Supported, SW performs entropy decoding
MPEG-4	Global motion compensation	Not supported
VC-1	Multi-resolution	Supported, upscaling will be performed by the post- processor
VC-1	Range mapping	Supported, range mapping will be performed by the post-processor
JPEG	Non-interleaved data order	Not supported

Decoder features

The features of the decoder for each supported standard are shown in following tables.

Table 6-13 H.264/SVC base layer features

Feature	Decoder support
Input data format	H.264 byte or NAL unit stream / SVC stream
Decoding scheme	Frame by frame (or field by field) Slice by slice
Output data format	YCbCr 4:2:0 semi-planar
Supported image size	48 x 48 to 1920 x 1088 Step size 16 pixels
Maximum frame rate	30 fps at 1920 x 1088
Maximum bit rate	As specified by H.264 HP level 4.1
Error detection and concealment	Supported

Table 6-14 MPEG-4/H.263/Sorenson Spark features

Feature	Decoder support
Input data format	MPEG-4 / H.263 / Sorenson Spark elementary video stream
Decoding scheme	Frame by frame (or field by field) Video packet by video packet
Output data format	YCbCr 4:2:0 semi-planar
Supported image size	48 x 48 to 1920 x 1088 (MPEG-4, Sorenson Spark) 48 x 48 to 720 x 576 (H.263) Step size 16 pixels
Maximum frame rate	30 fps at 1920 x 1088
Maximum bit rate	As specified by MPEG-4 ASP level 5
Error detection and concealment	Supported

Table 6-15 MPEG-2/MPEG-1 features

Feature	Decoder support
Input data format	MPEG-2 / MPEG-1 elementary video stream
Decoding scheme	Frame by frame (or field by field) Video packet by video packet
Output data format	YCbCr 4:2:0 semi-planar

Supported image size	48 x 48 to 1920 x 1088 Step size 16 pixels
Maximum frame rate	30 fps at 1920 x 1088
Maximum bit rate	As specified by MPEG-2 MP high level
Error detection and concealment	Supported

Table 6-16 JPEG features

Feature	Decoder support
Input data format	JFIF file format 1.02 YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
Decoding scheme	Input: buffer by buffer, from 5kB to 8MB at a time Output: from 1 MB row to 16 Mpixels at a time
Output data format	YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
Supported image size	48 x 48 to 8176 x 8176 (66.8 Mpixels) Step size 8 pixels
Maximum data rate	Up to 76 million pixels per second
Thumbnail decoding	JPEG compressed thumbnails supported
Error detection	Supported

Table 6-17 VC-1 features

Feature	Decoder support
Input data format	VC-1 stream
Decoding scheme	Frame by frame (or field by field) Slice by slice
Output data format	YCbCr 4:2:0 semi-planar
Supported image size	48 x 48 to 1920 x 1088 Step size 16 pixels
Maximum frame rate	30 fps at 1920 x 1088
Maximum bit rate	As specified by VC-1 AP level 3
Error detection and concealment	Supported

Table 6-18 RV features

Feature	Decoder support
Input data format	RV8, RV9 or RV10 stream
Decoding scheme	Frame by frame

	Slice by slice
Output data format	YCbCr 4:2:0 semi-planar
Supported image size	48 x 48 to 1920 x 1088 Step size 16 pixels
Maximum frame rate	30 fps at 1920 x 1088
Maximum bit rate	As specified by RV specification
Error detection and concealment	Supported

Table 6-19 VP6 features

Feature	Decoder support
Input data format	VP6.0 / VP6.1 / VP6.2 stream
Decoding scheme	Frame by frame
Output data format	YCbCr 4:2:0 semi-planar
Supported image size	48 x 48 to 1920 x 1088 Step size 16 pixels
Maximum frame rate	30 fps at 1920 x 1088
Maximum bit rate	As specified by VP6 specification
Error detection and concealment	Supported

Table 6-20 DivX feature

Feature	Decoder support
Input data format	Divx3, 4, 5 or 6 stream
Decoding scheme	Frame by frame Video packet by video packet
Output data format	YCbCr 4:2:0 semi-planar
Supported image size	48 x 48 to 1920 x 1088 Step size 16 pixels
Maximum frame rate	30 fps at 1920 x 1088
Maximum bit rate	As specified by the DivX specification
Error detection and concealment	Supported

Post-processing features

The post-processor (PP) features are described in following table. It is possible to run the post-processor combined with the decoder, or as a stand-alone IP block, when it can process image data from any external source.

Using combined mode reduces bus bandwidth, as PP can read its input data directly from the

decoder output without accessing external memory.

The post-processor output image can be alpha blended with two rectangular areas. If alpha blending is used in combined mode, the currently decoded image will be set as the background image.

Alpha blending can be used for creating transparent menus, subtitles and logos on top of the video playback. These overlay regions must be in the same color space, YCbCr or RGB, as the target format of the post-processor output image. If the two areas for alpha blending overlap, the second area overrides the first (the first area content is discarded). Alpha blending increases the bus load.

Table 6-21 post-processor features

Feature	Post-processor support
Input data format	Any format generated by the decoder in combined mode YCbCr 4:2:0 semi-planar YCbCr 4:2:0 planar YCbYCr 4:2:2 YCrYCb 4:2:2 CbYCrY 4:2:2 CrYCbY 4:2:2
Post-processing scheme	Frame by frame. Post-processor handles the image macroblock by macroblock, also in standalone mode.
Input image source	Internal source (combined mode) External source (standalone mode)
Output data format	YCbCr 4:2:0 semi-planar YCbYCr 4:2:2 YCrYCb 4:2:2 CbYCrY 4:2:2 CrYCbY 4:2:2 Fully configurable ARGB channel lengths and locations inside 32 bits, e.g. ARGB 32-bit (8-8-8-8), RGB 16-bit (2-6-5), ARGB 16-bit (4-4-4-4)
Input image size (combined mode)	48 x 48 to 8176 x 8176 (66.8 Mpixels) Step size 16 pixels
Input image size (stand-alone mode)	Width from 48 to 8176 Height from 48 to 8176

	Maximum size limited to 16.7 Mpixels Step size 16 pixels
Output image size	16 x 16 to 1920 x 1088 Horizontal step size 8 Vertical step size 2
Image up-scaling	Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel Arbitrary, non-integer scaling ratio separately for both dimensions Maximum output width is 3x the input width (within the maximum output image size limit) Maximum output height is 3x the input height – 2 pixels (within the maximum output image size limit)
Image down-scaling	Proprietary averaging filter Arbitrary, non-integer scaling ratio separately for both dimensions Unlimited down-scaling ratio (e.g. from 16Mpixel to QVGA)
YCbCr to RGB color conversion	BT.601-5 compliant BT.709 compliant User definable conversion coefficient
Dithering	2x2 ordered spatial dithering for 4, 5 and 6 bit RGB channel precision
Programmable alpha channel	Constant eight bit value can be set to the alpha channel of the 24-bit RGB output data to control the transparency of the output picture. The resulting 32-bit ARGB data can be used as input data for later alpha blending.
Alpha blending	Output image can be alpha blended with two rectangular areas. YCbCr semi-planar 4:2:0 PP output format is not supported when performing alpha blending. The supported overlay input formats are following: 1.8 bit alpha value + YCbCr 4:4:4, big endian channel order being A-Y-Cb-Cr, 8 bits each 2. 8 bit alpha value + 24 bit RGB, big endian channel order being A-R-G-B, 8 bits each
Deinterlacing	Conditional spatial deinterlace filtering. Supports only YCbCr 4:2:0 input format.

RGB image contrast adjustment	Segmented linear
RGB image brightness adjustment	Linear
RGB image color saturation adjustment	Linear
De-blocking filter for MPEG-4 simple profile /H263	Using a modified H.264 in-loop filter as a post-processing filter. Filtering has to be performed in combined mode.
Image cropping / digital zoom	User definable start position, height and width. Can be used with scaling to perform digital zoom. Usable only for JPEG or stand-alone mode.
Picture in picture	Output image can be written to any location inside video memory. Up to 1920 x 1088 sized displays supported.
Output image masking	Output image writing can be prevented on two rectangular areas in the image. The masking feature is exclusive with alpha blending; however it is possible to have one masking area and one blending area.
Image rotation	Rotation 90, 180 or 270 degrees Horizontal Vertical

Connectivity features

The decoder and post-processor support the connectivity features presented in following table. The usage of these features is described in more detail. Note that the endian modes can be separately set for input and output data, but they have no effect on RGB output data, as RGB channel order and their lengths are controlled separately.

Table 6-22 interface features

Feature	Decoder support
AXI master access	Yes,64-bit AXI 1.0
APB slave access	Yes, 32-bit AMBA 3 APB 1.0
Memory addressing	64-bit/32-bit aligned addressing, no byte addressing
Restricting the maximum issued AXI burst length	Yes, to any value between 1-16
Interrupt method	Polling or level based interrupting

32-bit little endian	Yes, byte order 3-2-1-0
32-bit big endian	Yes, byte order 0-1-2-3
64-bit little endian	Yes, byte order 7-6-5-4-3-2-1-0
64-bit big endian	Yes, byte order 0-1-2-3-4-5-6-7
Mixed 32-bit little endian in a 64-bit bus	Yes, byte order 3-2-1-0-7-6-5-4
Mixed 32-bit big endian in a 64-bit bus	Yes, byte order 4-5-6-7-0-1-2-3

6.3 Camera Interface

The camera interface (CIF) captures the dynamic video data stream or static image from camera sensor, and store the input into the memory after post-processing.

- Only support master type sensor module
- Only support 8-bit parallel data output from sensor
- Supported two camera sensors(only one works at the same time)
- Supported max sensor resolution: 4096x4096
- Supported max Pixel clock:100Mhz
- Supported max output image size (to memory): 4096x4096
- Support parallel interface for SYNC mode or ITU-R BT656 mode
- Support differential serial interface for MIPI CSI standard (support two data lanes)
- Max bandwidth of MIPI CSI interface: 2Gbps
- Support YCbCr422-format data/RAW image data/JPEG compressed data/RGB data (Bypass post-processing for RAW data/JPEG data/RGB data)
- Support test pattern for debugging
- Support cropping window of input image
- Support two post-processing paths for capture and display
- Support up-scaling for capture path/preview path
    - ✧ Max width of input image in capture path for up-scaling: 4096
    - ✧ Max width of input image in preview path for up-scaling: 2048
    - ✧ Max width of output image for up-scaling: 4096
    - ✧ Max x2 for X direction
    - ✧ Max x2 for y direction
    - ✧ Input format: YCbCr422
    - ✧ Output format: YCbCr422
- Support down-scaling for capture path/preview path
    - ✧ Max width of input image for down-scaling: 4096
    - ✧ Max width of output image for down-scaling: 4096
    - ✧ Max 1/128 for X direction
    - ✧ Max 1/128 for y direction
    - ✧ Input format: YCbCr422
    - ✧ Output format: YCbCr422

For capture path
- ✧ If scaling ratio for Y direction is in [1/128, 1/4], output width must not be more than 2048

For preview path
- ✧ If scaling ratio for Y direction is in (1/4, 1/2], output width must not be more than 2048
- ✧ If scaling ratio for Y direction is in [1/128, 1/4], output width must not be more than 1024

- Support the following special effect
  - ✧ Sepia
  - ✧ Special color
  - ✧ Negative
  - ✧ Mono color
  - ✧ Four block
  - ✧ Grid color
  - ✧ Embossing
  - ✧ Silhouette
  - ✧ Pencil Draw
  - ✧ Binary Effect
- Support 3-color OSD operation with size 480x24
- Support frame drop operation
- Support storage memory organization as YUV422 interleaved/YUV420 semi-planar format for input from sensor with YCbCr422/ ITU-R BT656 format
  - ✧ Support slice mode and frame mode
  - ✧ Only support little-endian storage organization
- Support direct storage for input from sensor with RAW data/JPEG data/RGB data
  - ✧ Only support frame mode
  - ✧ Only support little-endian storage organization
- Capture path support slice mode and frame mode
- Preview path only support frame mode
- Support auto-focus
  - ✧ Support max width of image for Auto-focus is 4096
  - ✧ Support max 8 rectangle windows for Auto-focus
  - ✧ When using Auto-focus, capture path is disabled for the sake of shared memory
- Support memory to memory path

6.4 Face Detection

The hardware design of face detection includes the calculation of integral and LAB (Locally Assembled Binary), which is composed of follows:

1) Support maximum sizer image width is 320 pixels, height is 240 pixels, minimum sizer image width is 24 pixels, and height is 24 pixels and no limitation for original image size.
2) Only support sizer image luminance format is row by row progressively.
3) Support 64bits AXI master interface.
4) Support 32bits APB slave interface.
5) Calculation of integral (x, y), and store the results to external memory through AXI bus interface.
6) Using Integral (x, y) results stored in external memory, calculate sum Y for both 3*3 and 2*2 blocks, compare the sum results of nine 3*3 or 2*2 blocks, get an 8-bit LAB, and then write it back to external memory.
7) Only support LABs image format is row by row progressively.

Actually the face detection include hardware module and software program, some function implement by software, which is composed as follows:

1) Support designate search window by software.
2) The maximum faces are not limitation in theory. At present in our system the maximum is 8.
3) Only support the smallest face haves 12x12 pixels resolution between two eyes.
4) About process 5~10 QVGA frames in a second.
5) Support detection of smile faces, but not wink faces.
6) Only report the eyes position.
7) Support the face in profile angle is -20 ~ 20 degrees, pitching angle is -30 ~ 30 degrees.
8) Support detection of black skin faces, actually need enough red pixels could be detected.
9) Support detection of color eyes and white hair.
10) The average value of luminance in image must surpass 16.
11) Support detection of face with glasses. The mask will decrease accuracy of detection.

6.5 LCD interface

LCD（Liquid Crystal Display） interface module is the interface between VC0882 and LCD panel. LCD interface module provides control signals and pixel data for LCD panels according to the timing requirements. It can support both DBI（Data Bus Interface） output mode and DPI （Display Pixel Interface） output mode.

- Supports Display Bus Interface (DBI) output mode, compliant to the MIPI(Mobile Industry Processor Interface) Alliance Display Bus Interface protocol v2.0.
  - Supports DBI Type A (Clocked E Mode) interface implementation;
  - Supports DBI Type B interface implementation;
  - Supports accessing (including writing and reading) in through mode;
  - Supports dual LCD panels work at different time(DBI & DBI, DBI&DPI)
  - Supports up to 24 bits per pixel (BPP) ;
  - Supports up to 24 bits interface with external device;
  - Supports flexible address mapping;
  - Supports flexible data mapping;
  - Supports flexible timing adjustment of control and data signals ;
  - Display size programmable up to 1080p(1920*1080) with configured interlaced or progressed mode;

- Supports Display Pixel Interface (DPI) output mode, compliant to the MIPI Alliance Display Pixel Interface protocol V2.0.
  - Display size programmable up to 1080p(1920 x1080) with configured interlaced or progressed mode;
  - Support for 12 & 16&18BPP&24BPP modes for RGB parallel output format (RGB444 , RGB565, RGB666,RGB888);
  - Support programmable pixel clock and asynchronous reset signal ;
  - Support flexible 3-wire and 4-wire serial interface(including write operation and read operation of panel registers)
  - Support parallel dpi interface with up to 24 bits interface;
  - Support CCIR656 interface (PAL mode and NTSC mode, 8 bit interface only);
  - Support CCIR601 interface.
  - Support UPS051&UPS052 interface (8 bit interface only).
  - Support 24BPP modes for UPS051&UPS052 interface.
  - Support 16BPP modes for CCIR656 and 24BPP modes for CCIR601.
  - Programmable 24-bit/18-bit/16-bit/12-bit/8-bit digital output interface
  - Supports various RGB format (RGB888, RGB565, RGB666, RGB555), YUV format (YUV444, YUV422) with 1X, 2X, 3X, 4X multiplexed output.
  - Support Max pixel rate up to 150MHz in DPI mode.

Note:
1) 1x for 1pixel/1 clock period, 2x for 1pixel/2 clock periods, 3x for 1pixel/3 clock periods, 4x for 1pixel/4 clock periods.
2) Dual panel work at the same time is not support. We can support dual panel in TDM mode. The dual panel is better to be dual DBI panel. Which panel will be used is selected by chip select signal separately. The other control and data pins are shared by these two panels. One DBI panel & one DPI panel can also be implemented, during which case, the DBI panel make use of the VSYNC blank time of DPI panel to refresh in through mode. It is hard for software to control the data flow.
3) The interlaced or progressive mode is configured in display engine mode
4) UPS051 represents RGB888 format with 1pixel/3 clock periods.
5) UPS052 represents RGB888 format with 1pixel/4 clock periods, the fourth clock data is invalid.
6) The Max pixel rate is up to 150MHz in DPI mode. It is also the max pixel clock. For 2X, the max pixel rate is 75MHz，For 3X, The max pixel rate is 50MHz.
7) When working in interlaced mode, only the odd lines will be refreshed in odd fields and only even lines will be refreshed in even fields. When working in progressive mode, all the valid lines in one frame will be refreshed including odd lines and even lines.

6.6 TV Encoder

- Support NTSC-M/J/4.43 and PAL- /B/D/G/H/M/N/I/Nc SDTV Composite signal output. (SECAM system and PAL-60 are not supported in CVBS Encoder)

Table 6-23 Supported NTSC/PAL Video Standards

No	Standards	Field Rate(Hz)	Number of Lines per frame	Active Lines per frame	Scan Type	Color Sub Carrier (MHz)	Blanking pedestal (IRE)	Line Frequency (KHz)
1	NTSC-M	60/1.001	525	480	Interlaced	3.58	7.5	15.734
2	NTSC-J	60/1.001	525	480	Interlaced	3.58	0	15.734
3	NTSC-443	60/1.001	525	480	Interlaced	4.43	7.5	15.734
4	PAL-B/D/G/H/I	50	625	576	Interlaced	4.43	0	15.625
5	PAL-M	60/1.001	525	480	Interlaced	3.58	7.5	15.734
6	PAL-N	50	625	576	Interlaced	4.43	7.5	15.625
7	PAL-Nc	50	625	576	Interlaced	3.58	0	15.625
8	PAL-60 (Not Supported)	60/1.001	525	480	Interlaced	4.43	7.5	15.734

9	SECAM-D/K/K1/L (Not Supported)	50	625	576	Interlaced	4.25(Db) 4.40(Dr)	0	15.625
10	SECAM-B/G (Not Supported)	50	625	576	Interlaced	4.25(Db) 4.40(Dr)	0	15.625

(Note: the letter, such as M,N,B,D,G,H,I,K, is related with the TV audio sub carrier)

1. Support YPbPr analog signals output on 480i/480p/576i/576p/720p/1080i/1080p systems

- Support programmable timing controller for various YPbPr resolutions. The Timing controller should be coincident with DE(Display Engine) timing controller
- Support internal test pattern for CVBS and YPbPr.
- Support Sync information from display engine as a timing slave mode.
- Support 10-bits video DAC for analog TV signal.

6.7 Display Engine

Display engine can read image pixel data stored in system memory (Frame Buffer, FBUF for abbreviation in later chapters) and transmit the processed image pixel data to LCD_IF or TV ENC module for displaying on the LCD panel or TV. The main function of display engine includes:

- Read image pixel data from at most 4 FBUF (at most 4 display layers + HW Cursor + Background)
- Convert the different format of SRC Image pixel data stored in FBUF to uniform format YUV444
- Implement overlay & alpha-blending operation to merge image pixel from different display layers
- Implement post-processing such as up-scaling, brightness/ contrast/ hue/ saturation/ adjustment, gamma, dithering, and etc.
- Convert the format of processed pixel data to proper format configured by SW
- Output pixel data and sync signals to TV Encoder or LCD_IF.
- Implement “capture with frame” function

Features

- Support MIPI DPI/MIPI DBI interface standard
- Support two DBI panels connection or one DPI panel plus one DBI panel connection (But the two panels can’t work at the same time.)
- Max panel resolution: 1600x1200 for TV/1920x1080 for LCD panel[1)]
- Max pixel rate up to 162MHz
- Support BT601 and BT609 color domain
- Programmable bits-per-pixel when output to LCD IF: 16/18/24-bpp such as YUV422, RGB565, RGB666, RGB888, and etc.

- Support programmable multi-cycle output mode: 1/2/3/4 cycles per pixel
- Support RGB-format pixel data output and YUV-format pixel data output with synchronous signals, and ITU-R BT656 format output
- Support interlace/non-interlace output
- Support 4 display layers plus background and HW cursor
  - ✧ Only support rectangle shape for all the layers
  - ✧ Max resolution of each display layer (from FBUF) is 1920x1080
  - ✧ Flexible cropping window from FBUF
  - ✧ Support mono-color background (YUV444 format), the resolution of background is always as same as display panel
  - ✧ Support HW cursor with max resolution 64x64
  - ✧ Supported image format and memory organization stored in FBUF
    - ■ Layer 1 & Layer 2:
      Semi-planar/Planar/Interleaved format for YUV422
      Semi-planar/Planar format for YUV420
    - ■ Layer 3 & Layer4:
      8-bpp
      RGB565
      Packed/Unpacked format for RGB888
      RGBA8888
      ARGB8888
    - ■ Only support little-endian organization
- Using Pipeline architecture to implement overlay & alpha-blending operation
  - ✧ Each pipeline phase merges two display layers, and the merged result enters the next pipeline phase
  - ✧ Each pipeline phase supports both overlay & alpha-blending operation
  - ✧ Support key color for overlay operation
  - ✧ Support INV/OR/AND/Transparent operation for overlay
  - ✧ Support pixel alpha value for ARGB8888/RGBA8888
  - ✧ Support global alpha value by configuring register
  - ✧ input format: YUV444
  - ✧ output format: YUV444
- Support up-scaling for overlay pixel data , which is output from overlay & alpha-blending unit
  - ✧ Max input size for up-scaling: 1920x1080
  - ✧ Max output size for up-scaling: 1920x1080
  - ✧ Max x6 for X direction
  - ✧ Max x6 for y direction
  - ✧ Input format: YUV444
  - ✧ Output format: YUV444
- Support brightness/contrast/hue/saturation adjustment
  - ✧ Input format: YUV444

- ✧ Output format: YUV444

- Support programmable gamma correction
  - ✧ Support R, G, B color components corrected separately (3 correction curve)
  - ✧ Input format: RGB888
  - ✧ Output format: RGB888
- Support dithering for less than 24-bit color display:
  - ✧ RGB888-> RGB565
  - ✧ RGB888-> RGB666
- Provide capture path to implement the function as “capture with frame”. For example, in some applications, it’s needed that capturing the image from sensor, then adding “some effect” on the captured image such as photo frame. This “effect” can be implemented by DE which merges the captured image from sensor and “effect” picture. After merging, DE need store the merged image to memory (Capture Buffer, CBUF for abbreviation in later chapters), so the “capture path” is used. Also, “the capture path” could be used for debugging.
- Supported image format and memory organization when writing to CBUF5)
  - ✧ Interleaved format for YUV422
  - ✧ Semi-planar format for YUV420
  - ✧ Unpacked format for RGB888
  - ✧ Only support little-endian organization

Table 6-24 Supported Max Size for Layers (from FBUF)

Layer Number	Image Pixel Format	Max Size
Layer1	YUV422	1080P
	YUV420	1080P
Layer2	YUV422	1080P
	YUV420	1080P
Layer3	YUV422	1080P
	YUV420	1080P
	8-bpp	1080P
	RGB565	1080P
	RGB888	1080P
	ARGB8888	1080P
	RGBA8888	1080P
Layer4	YUV422	1080P
	YUV420	1080P
	8-bpp	1080P
	RGB565	1080P
	RGB888	1080P
	ARGB8888	1080P
	RGBA8888	1080P

6.8 GPU

The GPU (Graphics Processing Unit) graphics IP core is designed to meet the market requirements for high performance 2D and 3D graphics and video decode and encode in mobile devices or consumer devices.

The GPU IP software stack fully supports for Android, Linux, and windows embedded platforms. It also supports the OpenGL ES 1.1 and the OpenGL ES 2.0 programmable API and OpenVG 1.1.

General Features

- 64 bit AXI interface for independent read and write data buses to memory
- Multiple burst length (support 8 bytes, 16 bytes, 32 bytes and 64 bytes) for AXI
- 4Kbytes addressable register space (could expand to 256Kbytes for future purpose)
- 32-bit data bus no burst
- Low power CMOS technology compatible
- Automatic clock gating for flip-flops and rams
- software controlled clock skipping
- Support up to 500Mhz
- Support virtual memory
- Support interrupt

Full-featured 3D Graphics Pipeline

- OpenGL ES 2.0 compliant, including extensions; OpenGL ES1.1; OpenVG 1.1
- IEEE 32-bit floating-point pipeline supports long shader instructions (maximum 256 instruction)
- Up to 256 threads per shader
- Up to 16 programmable Scalable Ultra-threaded, unified vertex and pixel shaders
- FSAA mechanisms: MSAA 4x, high quality FSAA 16x
- Vertex processing supported format: BYTE, UBYTE, SHORT, USHORT, INT, UINT, DEC, UDEC, FLOAT,FLOAT16,D3DCOLOR, FIXED16DOT16
- Primitive processing support triangle strip, fan, list, line strip and list, point list, quad
- Texture Processing: integer input texture formats: ARGB4444, XRGB4444, ARGB1555, XRGB1555, RGB565, ARGB8888, XRGB8888, RGBA4444, RGBA8888, YV12, NV12, YUY2, UYVY
- Texture processing: integer output texture formats: RGBA4444, RGBA5551, RGB565,

RGBA8888
- Texture mipmap support: 13 mipmap levels, programmable LOD biasing & replacement
- Texture filters: point sample, bi-linear, tri-linear, anisotropic (AF), percentage-closest filtering for depth textures
- Texture types: 2D, cubic environment map, projective, depth, HDR, bump map, displacement map, cube map
- Up to 8 programmable elements per vertex
- Dependent texture operation with high-performance
- Alpha blending
- Depth and stencil compare
- Support for 4 vertex shader and 8 pixel shader simultaneous textures
- Point sampling, bi-linear sampling, tri-linear filtering and cubic textures
- Resolve and fast clear
- 8K x 8K rendering target and texture size
- Low bandwidth at both high and low data rates
- Low CPU loading

Full-featured 2D Graphic Pipeline

- Bit blit, stretch blit, pattern blit and fast clear
- Line drawing
- Rectangle fill and clear
- Mono expansion for text rendering
- Anti-aliased font support
- ROP2, ROP3, ROP4
- Alpha blending
- 90/180/270 degree rotation
- Vertical and Horizontal mirror
- Transparency by monochrome mask, chroma key or pattern mask
- High quality 9-tap filter for scaling
- 32K x 32K coordinate system
- Color space conversion between YUV and RGB for both BT709 and BT601
- Clipping window
- Color Index Input conversion Support
- Filter Blit
- Input Formats: (Only Filter Blit support YUV input)
  - ✧ A1R5G5B5
  - ✧ A4R4G4B4
  - ✧ A8R8G8B8
  - ✧ X1R5G5B5
  - ✧ X4R4G4B4

- X8R8G8B8
- RGB565
- NV12 (semi-planer YUV420)
- NV16 (semi-planer YUV422)
- YUY2(package YUV422)
- UYVY(package YUV422)
- YV12(planer YUV420)
- 8-bit color index
- 1-bit monochrome

- The output data Formats:
  - A1R5G5B5
  - A4R4G4B4
  - A8R8G8B8
  - X1R5G5B5
  - X4R4G4B4
  - X8R8G8B8
  - RGB565

Chapter 07

Storage SubSystem

7 Storage SubSystem

7.1 USB OTG

The UOTG module is the high-speed universal serial bus dual-role subsystem module. It is composed of the USB 2.0 high-speed dual-role controller (UOTGC) and the high-speed single-port OTG PHY (single_port_otg_phy)

The function requirement of UOTG interface in VC0882 is list as following.

- Support USB Mass Storage in device mode
  - ✧ Provides production firmware download function
  - ✧ Provides access to SD/MMC card or NandFlash
  - ✧ Provides access to baseband resource (Nor-flash/SRAM)
- Support USB web camera in device mode
- Support USB PictBridge in device mode
- Support USB virtual serial port in device mode
- Support USB Virtual Ethernet Adapter in device mode
- Support USB Mass Storage in host mode
  - ✧ Provides access to USB-HDD/USB-DVDRW
- Support USB virtual serial port in host mode
- Support USB mouse in host mode.
- USB device speed could down to 1.1 by configuration
- Support USB charger detecting.
  - ✧ Support standard USB charger (DP and DM are shorted together in charger) detecting
  - ✧ Support non-standard USB charger (DP and DM are both floated in charger) detecting.

The UOTG includes the following features:

- Operates either as the host/peripheral in point-to-point communications with another USB function or as a function controller for a USB peripheral
- Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
- Supports point-to-point communications with one high-, full- or low-speed device
- Support control, interrupt, bulk, isochronous transfers
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
- Supports Suspend and Resume signaling
- Support remote wakeup in host mode
- Support 7 additional transmit endpoints and 7 additional receive endpoints
- The transfer type of each endpoint is configurable
- Configurable FIFOs, support dynamic FIFO sizing
- All endpoint FIFOs share a synchronous 4K bytes RAM
- Support for CPU access to FIFOs

- Support endpoints interrupt for transmitting or receiving packets
- Support for DMA access to FIFOs
- Support 8 DMA channels
- Support soft connect/disconnect
- Performs all transaction scheduling in hardware
- Supports off-chip charge pump regulator to generate 5 V for VBUS
- Support USB charger detecting.
  - ✧ Support standard USB charger (DP and DM are shorted together in charger) detecting
  - ✧ Support non-standard USB charger (DP and DM are both floated in charger) detecting

7.2 USB HOST

The UHOST module is the high-speed universal serial bus host subsystem module. It is composed of the high-speed single-port USB host controller (UHOSTEOC) and the high-speed single-port OTG PHY (single_port_otg_phy)

The main part of UHOSTEOC is an UHOSTIP which is a high-speed single-port USB2.0 host controller. It contains two independent, single-port host controllers that operate in parallel:

- The EHCI controller, based on the Enhanced Host Controller Interface (EHCI) specification for USB Release 1.0, is in charge of high-speed traffic (480M bit/s), over the UTMI interface.
- The OHCI controller, based on the Open Host Controller Interface (OHCI) specification for USB Release 1.0a is in charge of full-speed/low-speed traffic (12/1.5M bit/s, respectively), over a serial interface.

The single-port OTG PHY is owned by exactly one of the controllers at any time.

The UHOST includes the following features:

- High-speed single-port USB host controller. Support one USB downstream port.
- Fully compliant with the USB 2.0 specification, Enhanced Host Controller Interface (EHCI) Specification, Revision 1.0, and the Open Host Controller Interface (OHCI) Specification Release 1.0a.
- Supports high-speed, 480-Mbps transfers using an EHCI Host Controller, as well as full and low speeds through one integrated OHCI Host Controllers.
- The supported peripherals are determined by OS software.
- For VC0882, the following peripherals need to be supported: USB-HDD, USB-DVDRW, USB Mouse, USB Keyboard, USB Modem.

7.3 SDIO Controller

The MMC/SD/SDIO controller (**SDIO**) provides the host interface for supporting the standard MMC/SD/SDIO cards, which acts as a bridge between the host system bus and the MMC/SD/SDIO bus (referred to as “protocol bus”). The **SDIO** handles MMC/SD/SDIO protocols at the transmission level, it passes host bus transactions to the MMC/SD/SDIO cards by sending commands and performing data accesses to/from the cards.

VC0882 **SDIO** module has the following features:

- Compatible with SD Memory Card Spec 2.0 and supports SDHC up to 32GB card
- Compatible with SDIO Card Spec 2.0

a) Support SDIO Read Wait and Suspend/Resume operations

b) Support SDIO cards to interrupt the host, also support interrupt period

- Compatible with JESD84-A43 standard (MMC 4.3), up to 8-bit data bus
  - Support MMC boot operation
  - Support MMC bus testing procedure
- Support for SD Memory, SDIO, SD Combo, miniSD, MMC, MMC plus, MMC RS and Trans-Flash cards
  - Support dual voltage cards typically operating at 1.8V and 3V
  - Up to 200 Mbps of data transfer for SD/SDIO cards using 4-bit data bus
  - Up to 416 Mbps of data transfer for MMC cards using 8-bit data bus
- Support programmable protocol bus clock for different cards, up to 52MHz
- Support Single Block, Multi Block read and write, block size from 1 to 4096 bytes
- Support stop during the data transfer at block gap
- Support auto command transfer after completing the last data/non-data command transfer
- Support internal 2-channel DMA for both transmit and receive, up to 4 linked list item (referred to as “LLI”) register available for linked memory access
- Support two 32x32 bit FIFO for both transmit and receive
- Interrupt-based application interface to control software interaction

7.4 NAND Flash Controller

NAND Flash Controller (NFC) is designed for NAND flash interface. The NFC provides an interface between standard NAND Flash devices and the IC and hides the complexities of accessing a NAND Flash memory device. It provides an interface to 8-bit or 16-bit NAND flash devices (including SLC, MLC and TLC[1)]) with different page size from 512B to 16KB. The NAND interface supports a few functions, such as Page Reading, Page Writing, Block erasing, Reset operation and so on. The NFC module can support BCH (Bose, Chaudhuri & Hocquenghem Type of code) encode and decode operation. When sector size is 512B, the

4/8/16 bit ECC is supported, when sector size is 1024B, the 24/32/40/48 bit ECC is supported. Logically, NFC is mainly composed of three parts: MARB DMA interface, ECC codec and NAND flash control interface.
Note1): SLC: Single Level Cell; MLC: Multiple Level Cell; TLC: Triple Level Cell.

- Compliant to open NAND Flash Interface (ONFI) 1.0 Specification.
- Support mainly operation by hardware:
  - Support page program and page read operation
  - Support page cache program and page cache read operation
  - Support page random program and page random read operation
  - Support status read operation after page program operation
- Support mainly operation by software:
  - Support block erase operation
  - Support reset operation
  - Support plane program and plane read operation
  - Support status read operation[1)]
- Hardware BCH encoder and decoder are included.
  - Error detection/correction capability of 4/8/16 bits per 512 bytes
  - Error detection/correction capability of 24/32/40/48 bits per 1024 bytes
  - 8-bit parallel architecture and calculation based on 1-bit length
- The ECC calculation region is configurable (User data only or both user data and FTL[2)] data or bypass the ECC calculation for both user data and FTL data)
- Support SLC, MLC and TLC NAND flash.
- Support single command transfer by hardware and triggered by software
- Support single address transfer by hardware and triggered by software
- Support single data transfer(including reading and programming) by hardware and triggered by software
- Support auto checking whether page is erased or not by hardware during page reading operation
- Support address & command transfer of random operation by hardware when in FTL transfer
- Support interlaced storage of ECC and user data.
- Support Asynchronous Interface Bus Operation
  - Module frequency is 50Mhz for 8-bit interface, and interface clock is 50Mhz
  - Module frequency is 100Mhz for 16-bit interface, and interface clock is 50Mhz
- Support max 16 DMA operation consecutively during a page operation
  - 8KB for 512B/sector
  - 16KB for 1024B/sector
- Support FTL data length up to 32 byte[3)] when FTL ECC is enabled.
- Support max 4 consecutive page read/ page cache read by hardware
- Support max 4 consecutive page program/page cache program by hardware
- Support read NAND flash status by hardware after page program operation

- Support AXI BUS Interface.
- Support 8/16 bit data bus.
- Support 16 CS (chip select) signal interface.
- Support 2 RB(ready/busy) signal interface
- Support NAND DMA data transfer by hardware and command & address transfer by software.
- Support both NAND DMA data transfer and command & address transfer by hardware
- Support delay configuration (8bit registers from 0 to 0xFF nfc_mclk) between command and data.
- Support delay configuration (8bit registers from 0 to 0xFF nfc_mclk) between address and data.
- Support error correction by hardware itself before writing data to DRAM during NAND read operation[4)].
- Support configurable page address cycle number (four cycles or five cycles).
- Support 16bit nand flash composed by double chip 8bit nand flash.

Note1): The read status operation can be supported by software. During page program operation, the status operation is done by hardware itself after a page program is done.
Note2): FTL is file transfer layer. The address & command transfer of random operation by hardware is also used when only FTL data needs to be read or written, it can also be used for other type of data transfer for compatibility . But only one DMA random transfer supported for one page in one trigger operation, multiple random transfers are not supported during one trigger operation.
Note3): There is no FTL length restriction when there FTL does not participate in ECC calculating.
Note4): The operation is reading data from NAND and writing them to DRAM.

7.5 SPI (Serial Peripheral Interface)

The SPI controller module has the following features:
- Support *two* SPI controllers;
- Provide master/slave modes selectable by control registers;
- Full duplex synchronous serial data transfer;
- The frequency, polarity, and phase of SCLK are programmable;
- The polarity of SSN is programmable;
- MSB or LSB first data transfer mode is programmable for both 8-bit and 16-bit;
- Support SPI data transfer by APB mode and DMA mode;
- The max transfer length of DMA transfer is 2M bytes for master mode;
- 8X32 FIFO for both transmitting and receiving data;
- The max frequency of module clock (`spi_clk`) is 216MHz;
- The max transfer speed in master mode is 54MHz;

- The max transfer speed in slave mode is 27MHz;
- When work in master mode, one SPI master can connect up to 2 SPI slaves with *two* SSN and MISO.

Chapter 08

Peripheral SubSystem

8 Peripheral SubSystem

8.1 Audio Module

VC0882 Audio Subsystem (**AUD**) is responsible for the chip's audio playback and record. It mainly consists of 2 parts: Audio Interface and Audio Codec:

- Audio Interface (referred to as **AUDIF**): it acts as a bridge which handles data transfer between System Memory and Audio Codec, also supporting data format conversion and digital mixer
- Audio Codec (referred to as **ACOD**): it's a mixed analog/digital virtual component containing a stereo audio codec (ADC + DAC) and additional analog function offering an ideal mixed signal front end for low power and high quality audio applications

The **AUD** also provides 2 I2S/PCM Interfaces of master mode through VC0882 PADs to support optional outer devices connection, such as Bluetooth and the 3rd-party Audio Codec. With VC0882 Audio Subsystem, various applications can be implemented, such as music playback, microphone record, call in/out with background sound, call in/out with 2-way record, karaoke with record, FM radio with record, as well as WIFI phone call in/out.

The **AUDIF** module provides the following features:

- Provides 2 I2S/PCM Interfaces of master mode through VC0882 PADs, so as to connect external devices of slave mode
  - Transfers with MSB first and left alignment
  - Supports 8 I2S Formats and 4 PCM Formats
- Includes two 32-bit stereo digital mixer (produce Y = A + B result)
  - Supports processing left and right channel data separately
  - Supports overflow and underflow clip control
- Includes 1 Transmit DMA channel and 1 Transmit FIFO (32x32 bit), also supports software ping-pong buffer operation
- Includes 2 Receive DMA channels and 2 Receive FIFOs (32x32 bit), also supports software ping-pong buffer operation
- Supports 6 memory formats of audio raw data: Stereo-32bit, Stereo-16bit, Stereo-8bit, Mono-32bit, Mono-16bit, and Mono-8bit
- Supports only signed audio data processing
- Switches data path by multiplexers to implement various applications flexibly

The **ACOD** module provides the following features:

- Built-in PLL solution to better jitter issue

- 12MHz or 13MHz master clock supply
- Contains a high-quality 24-bit stereo ADC and a high-quality 24-bit stereo DAC
- Provides 6 mono differential line inputs with boost gain stage (0/4/8/12/16/20 dB), they can be used either for line in or microphone in application
- Includes 2 multiplexers in front of the input PGA to select the signal between the line inputs
- Provides 1 stereo single-end 16/32 Ohm headphone output
- Provides 2 mono differential line output that but they can't be driven simultaneously
- Provides 1 mono differential BTL 16/32 Ohm receiver output
- Provides stereo differential speaker output and one of them can also be configured to the mono differential BTL 8 ohm output
- Supports audio sampling rates (Fs) from 8KHz to 96KHz (88.2KHz not supported)
- Supports the Automatic Gain Control (AGC) function for better sound recording performances
- Built-in reduction of audible glitches systems
  - Patented pop-up noise reduction system
  - Provide soft mute mode to reduce audible parasites
  - Include zero-cross detection to minimize zipper noise
- Supports output short circuit protection
- Provides 2 microphone bias output
- Embedded low dropout linear regulator
- Internal voltage reference to generate all required internal voltages

8.2 UART

The UART (Universal Asynchronous Receiver/Transmitter) core provides serial communication capabilities, which allow communication with external devices, like another computer using a serial cable and RS232 protocol. The UART module performs all of the normal operations associated with start-stop asynchronous communication. Serial data is transmitted and received at standard bit rates using the internal baud rate generator. This core is designed to be maximally compatible with the industry standard National Semiconductors' 16550A device.

The UART controller module has the following features:

- Functional compatible with the 16550A.
- Full-duplex operation.
- Robust receive data sampling with noise filtering.
- 64-byte FIFO for receiver and 64-byte FIFO for transmitter.
  - Programmable interrupt trigger levels for FIFO.
  - "Old data" timer on receiver FIFO.
- Fully programmable serial interface.
  - Data bit: 7-bit or 8-bit.

  - Parity bit: None, Even, Odd, or Stick check.
  - Stop bit: 1-bit or 2-bit.
- Break condition detection and generation.
- Embody baud rate generator.
  - Programmable integer and fractional divisor for baud rate generation.
  - Programmable Baud rate computation method support up to 12Mbps baud rate.
  - Slow speed mode: Baud rate = (functional clock/16)/divisor.
  - Middle speed mode: Baud rate = (functional clock/8)/divisor.
  - High speed mode: Baud rate = (functional clock/4)/divisor.
- Complete status-reporting capability.
- Internal diagnostic capability.
  - Loop-back mode for self test.
  - Break condition, parity error and framing error simulation.
- Slow infrared asynchronous interface that conforms to the Infrared Data Association (IrDA) specification.
- Separate APB read/write operation for transmit and receive data.
- Separate DMA Operation for transmit and receive data services.
- Modem control functions with DSR, DCD, RI and DTR signals.
- Auto-flow control capability.
  - RTS controlled by UART receive FIFO.
  - CTS from external controls UART transmitter.
- Software-flow control capability.
  - Programmable XOFF character used to stop the UART transmitter.
  - Programmable XON character used to start the UART transmitter.

8.3 IIC Module

I2C is a two-wire, bi-directional serial bus, which provides a simple and efficient method of data exchange between devices. It is most suitable for applications requiring occasional communication over a short distance between many devices.

There are two separate I2C master controllers in VC0882, each of which provides an interface between the internal ARM processor and any external I2C-bus-compatible device that connects through the I2C serial bus. They use the same I2C master controller module. This document describes the I2C master controller module in VC0882.

The I2C master controller module has the following features:

- Master mode only
- Compliance with Philips I2C bus specification version 2.1
- Support for standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Support multi master mode

- 7-bit and 10-bit device addressing modes
- Support start/restart/stop
- Transaction based software interface
- Built-in 16-byte FIFO for buffered read or write
- The maximum transfer length of each transaction is 65535 for read or write operation. The zero transfer length means there is no data to be written out or no data to be read in for current transaction.
- Module enable/disable capability
- Programmable SCL clock generation
- 8-bit-wide data access
- Arbitration lost detection
- Bus busy detection
- Clock Stretching and Wait state generation
- Support PMU hardware directly communicates with external power management chip with five request channels and priority control. Support hardware round-robin arbitration and software arbitration. During software arbitration mode the software can has exclusive I2C bus control until it release the I2C bus.
- Not support CBUS address
- Not support high-speed mode

8.4 PWM

The PWM module is used to generate square waves with variable pulse width and frequency. The frequency of output signal ranges from 6K to 12MHz with 24MHz reference clock, and the output pulse ratio ranges from 0/256 to 255/256. The average DC voltage of PWM wave can be utilized to drive various devices, such as LED and motor. In VC0882, there are three PWM outputs. Each PWM output can be controlled by software independently.

The following lists the main features of PWM module:

- AMBA 3 APB (Advanced Peripheral Bus) register bus interface
- Supports up to 3 external channels
- The pulse ratio of the output waveform ranges from 0/256 to 255/256.
- The frequency of the output waveform ranges from 6KHz to 12MHz.

8.5 KeyPad

The KPD module supports the keypad that connects the column and row when their intersecting key is pressed. The KPD is a 16-bit interface peripheral and provides interface for R x C off-chip keypad matrix.

An off-chip keypad matrix is defined as an X-Y matrix where one key is pressed at a time or more keys are pressed simultaneously, the keypad definition is used for portable applications such as mobile phones, personal digital assistants, smart handheld devices, personal media players or other handheld applications.

The 16-bit keypad ports can be configured as output ports for C (column) or input ports for R (row) by writing to keypad control registers according to system application. R (row) is input of KPD module, while C (column) is output of KPD module.

The KPD is designed to simplify the software task of scanning a keypad matrix. With appropriate software support, the KPD is capable of detecting depress/release and decoding one or multiple keys pressed simultaneously on the keypad.

Logic in the KPD is capable of scanning the keypad matrix periodically, and storing up to three key-values pressed in the interrupt status register simultaneously. The KPD may generate a CPU interrupt any time when a key press or release is detected, if the interrupt is unmasked.

The following lists the main feature of KPD IP core:

- 32-bit AMBA-APB slave bus interface.
- Supports R x C external keypad matrix (R + C <= 16).
- Glitch suppression circuit designs for key depress/release detection.
- Port pins can be used as general purpose I/O.
- Supports software matrix scanning.
- Supports hardware matrix scanning.
- Supports programmable de-bounce time by KPD_DWR register.
- Supports periodic scan, the interval is programmable.
- Supports Short key-press, Long key-press, Continuous key-press and Combined key-press.
- Interval for Short key-press, Long key-press and Continuous key-press is programmable.
- Supports up to three combined key-presses at most and can store three key-values simultaneously.
- Supports interrupt status reading.
- Supports interrupt mask.
- Supports two types of interrupt process mode.

8.6 Touch Panel Interface

The TPI module is the touch panel interface controller module. It works with FESAR_TOP (which is also called TPIPHY) in PMU domain to realize following functions:

- Support resistive 4-wire touch panel in multi-touch mode

- Support resistive 5-wire touch panel in single-touch mode.
- Key scan function
- Battery measurement function
  - Battery voltage
  - Battery temperature
  - Battery ID

The TPI has the following features:

- Support resistive 4-wire touch panel in multi-touch mode.
  - ✧ Pen down and pen up detect for touch panel
  - ✧ Distinguish between single-touch and two-touch
  - ✧ X/Y coordinate, movement and touch pressure measurement for single-touch.
  - ✧ Zoom and rotate measurement for two-touch.
- Support resistive 5-wire touch panel in single-touch mode.
- Support key scan using just one pin
  - ✧ Key down detect for key scan
  - ✧ Key up detect for key scan
- Support battery measurement
  - ✧ Max battery voltage input is 5V
  - ✧ Max battery temperature voltage input is 2.4V
  - ✧ Max battery ID voltage input is 2.4V
- Internal 1.2V reference
- 10-bit low power SAR ADC (successive approximation register type ADC)
- Max sample rate is 125KHz
- Support two working modes
  - ✧ MANUAL sample with REGISTER transfer mode
  - ✧ AUTO sample with DMA transfer mode

Chapter 09

Electrical Parameters And Timing

9 Electrical Parameters and Timing

9.1 Absolute Maximum Ratings

Table 9-1 Absolute Maximum Ratings for BGA445

Symbol	Description	Min	Max	Unit
Digital				
VDD_CORE_ARM	ARM Core Digital Power	-0.3	1.5	V
VDD_CORE_VIDEO	Video Codec Core Power	-0.3	1.5	V
VDD_CORE_GPU	GPU Core Power	-0.3	1.5	V
VDD_CORE_CORE	Shutdown Domain Core Digital Power except ARM, Video Codec & GPU	-0.3	1.5	V
VDD_CORE_PMU	PMU Domain Core Logic Digital Power and ALL DIGITAL IO Core Power	-0.3	1.5	V
VDD_IO_SYS	SYS IO Digital Power	-0.3	3.0	V
VDD_IO_LCD	LCD I/O Digital Power	-0.3	3.6	V
VDD_IO_NF	NAND Flash I/O Digital Power	-0.3	3.6	V
VDD_IO_SD01	SDIO 0/1 I/O Digital Power	-0.3	3.6	V
VDD_IO_SD23	SDIO 2/3 I/O Digital Power	-0.3	3.6	V
VDD_IO_CS	Camera Sensor I/O Digital Power	-0.3	3.6	V
VDD_IO_DDR	DDR PHY I/O Power	-0.3	1.95	V
DDR_VREF	DDR PHY SSTL Reference Power	-0.3	0.975	V
VDD_EFUSE	On-chip Efuse Cell Power	-0.3	2.75	V
VDD_TP33	Touch Panel SAR ADC 3.3v Digital Power	-0.3	3.6	V
VDD_VDAC	VDAC Digital Power	-0.3	3.6	V
Analog				
VDDA_VDAC	VDAC Analog Power for Channel R/G/B	-0.3	3.6	V
VDDA_PLL12_1	PLL Analog Power 1	-0.3	1.5	V
VDDA_PLL12_2	PLL Analog Power 2	-0.3	1.5	V
VDDA_PLL12_3	PLL Analog Power 3	-0.3	1.5	V
VDDA_PLL12_4	PLL Analog Power 4	-0.3	1.5	V
VDDA_PLL12_5	PLL Analog Power 5	-0.3	1.5	V
VDDA_PLL12_6	PLL Analog Power 6	-0.3	1.5	V
VDDA_USBOTG33	USB OTG PHY Analog Power 3.3v	-0.3	3.6	V
VDDA_USBHOST33	USB HOST PHY Analog Power 3.3v	-0.3	3.6	V
VDDA_TP33	Touch Panel SAR ADC Analog Power	-0.3	3.6	V
VDDA_AUD_HP	AUD 2.5 V Power Supply For Headphone (from VDDA_AUD_VOUT)	-0.3	2.75	V
VDDA_AUD_OPA	AUD 3.3 V Power Supply For Speaker PA Macro and IO	-0.3	3.6	V

VDDA_AUD_RCV	AUD 3.3 V Power Supply For Receiver PA	-0.3	3.6	V
VDDA_AUD_VIN	AUD 3.3 V Power Supply Input	-0.3	3.6	V
Temperature				
t_{STR}	Storage Temperature	-40	125	^oC
t_{OP}	Operational Temperature	-20	70	^oC

9.2 Recommended Operating Conditions

Table 9-2 Recommended Operating Conditions for BGA445

Symbol	Description	Min	Typ	Max	Unit
Digital					
VDD_CORE_ARM	ARM Core Digital Power	1.0	1.2	1.5	V
VDD_CORE_VIDEO	Video Codec Core Power	1.0	1.2	1.5	V
VDD_CORE_GPU	GPU Core Power	1.0	1.2	1.5	V
VDD_CORE_CORE	Shutdown Domain Core Digital Power except ARM, Video Codec & GPU	1.0	1.2	1.5	V
VDD_CORE_PMU	PMU Domain Core Logic Digital Power and ALL DIGITAL IO Core Power	1.0	1.2	1.5	V
VDD_IO_SYS	SYS IO Digital Power	2.6	2.8	3.0	V
VDD_IO_LCD	LCD I/O Digital Power (1.8v)	1.7	1.8	1.9	V
	LCD I/O Digital Power (2.8v)	2.6	2.8	3.0	V
	LCD I/O Digital Power (3.3v)	3.0	3.3	3.6	V
VDD_IO_NF	NAND Flash I/O Digital Power (1.8v)	1.7	1.8	1.9	V
	NAND Flash I/O Digital Power (2.8v)	2.6	2.8	3.0	V
	NAND Flash I/O Digital Power (3.3v)	3.0	3.3	3.6	V
VDD_IO_SD01	SDIO 0/1 I/O Digital Power (1.8v)	1.7	1.8	1.9	V
	SDIO 0/1 I/O Digital Power (2.8v)	2.6	2.8	3.0	V
	SDIO 0/1 I/O Digital Power (3.3v)	3.0	3.3	3.6	V
VDD_IO_SD23	SDIO 2/3 I/O Digital Power (1.8v)	1.7	1.8	1.9	V
	SDIO 2/3 I/O Digital Power (2.8v)	2.6	2.8	3.0	V
	SDIO 2/3 I/O Digital Power (3.3v)	3.0	3.3	3.6	V
VDD_IO_CS	Camera Sensor I/O Digital Power (1.8v)	1.7	1.8	1.9	V
	Camera Sensor I/O Digital Power (2.8v)	2.6	2.8	3.0	V
	Camera Sensor I/O Digital Power (3.3v)	3.0	3.3	3.6	V
VDD_IO_DDR	DDR PHY I/O Power (1.5V)	1.425	1.5	1.575	
	DDR PHY I/O Power (1.8V)	1.7	1.8	1.9	V
DDR_VREF	DDR PHY SSTL Reference Power	0.7125	0.75	0.7875	

	(0.5 * VDD_IO_DDR)				
	DDR PHY SSTL Reference Power (0.5 * VDD_IO_DDR)	0.85	0.9	0.95	V
VDD_EFUSE	On-chip Efuse Cell Power	2.25	2.5	2.75	V
VDD_TP33	Touch Panel SAR ADC 3.3v Digital Power	3.0	3.3	3.6	
VDD_VDAC	VDAC Digital Power (2.5V)	2.25	2.5	2.75	V
	VDAC Digital Power (3.3V)	3.0	3.3	3.6	V
Analog					
VDDA_VDAC	VDAC Analog Power for Channel R/G/B (2.5V)	2.25	2.5	2.75	V
	VDAC Analog Power for Channel R/G/B (3.3V)	3.0	3.3	3.6	V
VDDA_PLL12_1	PLL Analog Power 1	1.0	1.2	1.5	V
VDDA_PLL12_2	PLL Analog Power 2	1.0	1.2	1.5	V
VDDA_PLL12_3	PLL Analog Power 3	1.0	1.2	1.5	V
VDDA_PLL12_4	PLL Analog Power 4	1.0	1.2	1.5	V
VDDA_PLL12_5	PLL Analog Power 5	1.0	1.2	1.5	V
VDDA_PLL12_6	PLL Analog Power 6	1.0	1.2	1.5	V
VDDA_USBOTG33	USB OTG PHY Analog Power 3.3v	3.0	3.3	3.6	V
VDDA_USBHOST33	USB HOST PHY Analog Power 3.3v	3.0	3.3	3.6	V
VDDA_TP33	Touch Panel SAR ADC Analog Power	3.0	3.3	3.6	V
VDDA_AUD_HP	AUD 2.5 V Power Supply For Headphone	Supplied by VDDA_AUD_VOUT			V
VDDA_AUD_OPA	AUD 3.3 V Power Supply For Speaker PA Macro and IO	2.7	3.3	3.6	V
VDDA_AUD_RCV	AUD 3.3 V Power Supply For Receiver PA	2.7	3.3	3.6	V
VDDA_AUD_VIN	AUD 3.3 V Power Supply Input	2.7	3.3	3.6	V
Temperature					
t_{STR}	Storage Temperature	-40		125	^oC
t_{OP}	Operational Temperature	-20		70	^oC

9.3 DC Characteristics

Analog IO

Table 9-3 Analog IO DC Electrical Specifications

Parameter	Description	Min.	Nom.	Max.	Units
$V_{I(core)}$	Input Voltage Range for the Cell with Thin Device (1.2v analog domain)	-0.3		1.32	V
$V_{I(IO)}$	Input Voltage Range for the Cell with Thick Device (2.5v analog domain)	-0.3		2.75	V
	Input Voltage Range for the Cell with Thick Device (3.3v analog domain)	-0.3		3.6	V

Table 9-4 Analog IO Pin Capacitance

Pin Name	Capacitance (pF)
AIO	0.2907 / 0.9088

Standard Digital IO

Table 9-5 Standard Digital IO DC Electrical Specifications

Parameter	Description	Min.	Nom.	Max.	Units
V_{IL}	Input Low Voltage	-0.3	0	0.8	V
V_{IH}	Input High Voltage (1.8v power)	1.3	1.8	2.1	V
	Input High Voltage (2.8v power)	1.7	2.8	3.0	V
	Input High Voltage (3.3v power)	2.0	3.3	3.6	V
V_T	Threshold Point (1.8v power)	0.76	0.82	0.90	V
	Threshold Point (2.8v power)	1.18	1.27	1.40	V
	Threshold Point (3.3v power)	1.39	1.50	1.65	V
V_{T+}	Schmitt Trigger Low to High Threshold Point (1.8v power)	0.88	0.95	1.04	V
	Schmitt Trigger Low to High Threshold Point (2.8v power)	1.37	1.48	1.61	V
	Schmitt Trigger Low to High Threshold Point (3.3v power)	1.62	1.75	1.90	V

V_{T-}	Schmitt Trigger High to Low Threshold Point (1.8v power)		0.64	0.59	0.78	V
	Schmitt Trigger High to Low Threshold Point (2.8v power)		1.00	1.09	1.22	V
	Schmitt Trigger High to Low Threshold Point (3.3v power)		1.18	1.29	1.44	V
I_I	Input Leakage Current @ V_I =3.3V or 0V				±10μ	A
I_{OZ}	Tri-state Output Leakage Current @ V_O =3.3V or 0V				±10μ	A
R_{PU}	Pull-up Resistor		34K	51K	81K	Ω
R_{PD}	Pull-down Resistor		35K	51K	88K	Ω
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage (1.8v power)		1.3			V
	Output High Voltage (2.8v power)		2.0			V
	Output High Voltage (3.3v power)		2.4			V
I_{OL}	Low Level Output Current @ V_{OL} (max)	04:04mA	4.9	7.5	10.0	mA
		08:08mA	10.0	15.2	20.2	mA
		12:12mA	15.1	22.9	30.4	mA
		16:16mA	20.2	30.6	40.6	mA
I_{OH}	High Level Output Current @ V_{OH} (min)	04:04mA	7.0	14.0	24.2	mA
		08:08mA	13.9	28.0	48.2	mA
		12:12mA	20.9	42.0	72.3	mA
		16:16mA	27.8	56.0	96.3	mA

Table 9-6 Standard Digital IO Pin Capacitance

Cell Name	Pin Name	Capacitance (pF)
Normal Digital IO	PAD	1.44 ~ 1.53

Table 9-7 2~30M OSC IO parameter

Cell Name	Capacitance (pF)	Requirement		Suggested Frequency (Mhz)
		Duty Cycle	Jitter	
2~30M OSC IO	1.4422	45% ~ 55%	300ps	26

MEMORY IO

LPDDR

Table 9-8 LPDDR DC Electrical Specifications

Parameter	Description	Min	Nom	Max	Units
$V_{IH(dc)}$	Input logic threshold High, Mobile DDR mode	0.7 * VDDQ			V
$V_{IL(dc)}$	Input logic threshold Low, Mobile DDR mode			0.3 * V_{DDQ}	V

Table 9-9 MEMORY IO (LPDDR) Pin Capacitance

Pin Name	Capacitance (pF)
PAD/PADP/PADN	2.1131

DDR2

Table 9-10 DDR2 DC Electrical Specifications

Parameter	Description	Min	Nom	Max	Units
$V_{IH(dc)}$	DC input voltage High	V_{REF} + 0.125		V_{DDQ} + 0.3	V
$V_{IL(dc)}$	DC input voltage Low	V_{SSQ} - 0.3		V_{REF} - 0.125	V
$V_{OH(dc)}$	DC output logic High	V_{DDQ} - 0.28			V
$V_{OL(dc)}$	DC output logic Low			V_{SSQ} + 0.28	V
R_{TT}	Input termination resistance (ODT) to V_{DDQ} / 2	120 60 40	150 75 50	180 90 60	ohm

Table 9-11 MEMORY IO (DDR2) Pin Capacitance

Pin Name	Capacitance (pF)
PAD/PADP/PADN	2.13~2.29

DDR3

Table 9-12 DDR3 DC Electrical Specifications

Parameter	Description	Min	Nom	Max	Units
$V_{IH(dc)}$	DC input voltage High	V_{REF} + 0.100		V_{DDQ}	V
$V_{IL(dc)}$	DC input voltage Low,	V_{SSQ} - 0.3		V_{REF} - 0.100	V
$V_{OH(dc)}$	DC output logic High	0.8*V_{DDQ}			V
$V_{OL(dc)}$	DC output logic Low			0.2 * V_{DDQ}	V
R_{TT}	Input termination resistance (ODT) to V_{DDQ}/2	100 54 36	120 60 40	140 66 44	ohm

Table 9-13 MEMORY IO (DDR3) Pin Capacitance

Pin Name	Capacitance (pF)
PAD/PADP/PADN	2.15~2.31
ZQ	0.91

USB Analog IO

Table 9-14 USB Analog IO DC Electrical Specifications

Parameter	Description	Min.	Nom.	Max.	Units
$V_{I(DP/DM/VBUS)}$	Input Voltage Range for DP/DM/VBUS	-0.3		5.25	V
$V_{I(ID/RREF/ANA\_TEST)}$	Input Voltage Range for ID/RREF/ANA_TEST	-0.3		2.75	V

9.4 CIF Interface Timing

Table 9-15 Sensor Interface Timing Conditions

Timing Condition Parameter		MIN	MAX	Unit
Input Conditions(CS_PCLK)				
t_r	Input clock rise time	0.5	2	ns
t_f	Input clock fall time	0.5	2	ns
Input Conditions(Excluding CS_PCLK)				
t_R	Input signal rise time	0.5	5	ns
t_F	Input signal fall time	0.5	5	ns

Table 9-16 Sensor Interface Electrical Characteristics

Parameter		MIN	MAX	Unit	Notes
t_p	Cycle time, CS_PCLK period	10		ns	(1)
t_{vs}	Setup time, Vsync valid before PCLK active edge	-0.6		ns	
t_{vh}	Hold time, Vsync valid after PCLK active edge	1.5		ns	
t_{hs}	Setup time, Hsync valid before PCLK active edge	0.9		ns	
t_{hh}	Hold time, Hsync valid after PCLK active edge	1.5		ns	
t_{ds}	Setup time, Data valid before PCLK active edge	0.3		ns	
t_{dh}	Hold time, Data valid after PCLK active edge	1.6		ns	

(1) Related to the input maximum frequency supported by the CIF module.

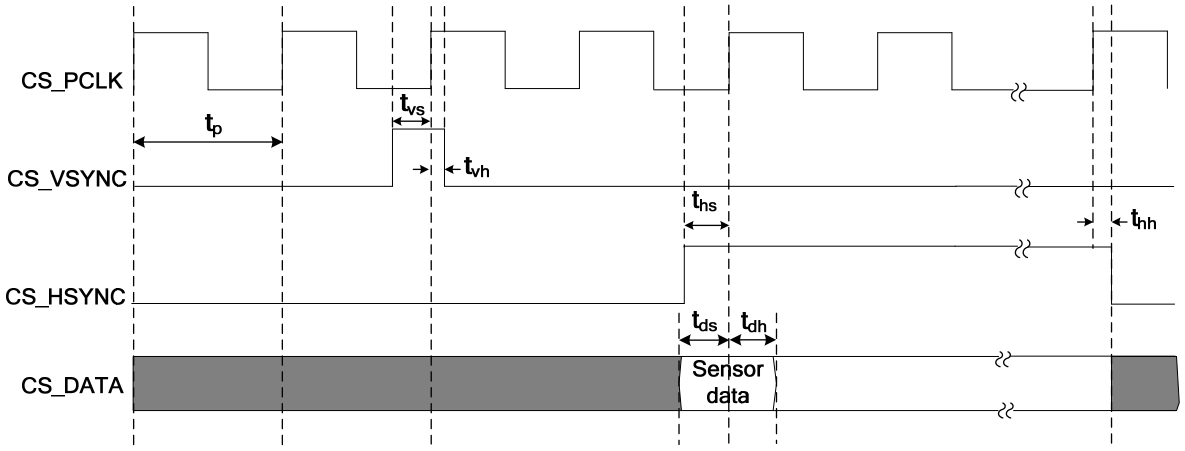

Figure 9-1 Sensor Interface Timing

9.5 SPI Interface Timing

Table 9-17 SPI Interface Timing Conditions

Timing Condition Parameter		MIN	MAX	Unit
Input Conditions				
t_R	Input signal rise time	0.5	5	ns
t_F	Input signal fall time	0.5	5	ns
Output Condition				
C_{load}	Output load capacitance		30	pf

SPI in Slave Mode

Table 9-18 SPI Interface Electrical Characteristics (Slave Mode)

Parameter		MIN	MAX	Unit	Notes
t_p	Cycle time, SPI_SCLK period	62.5		ns	(1)
t_{ss}	Setup time, SPI_SSN valid before SPI_SCLK active edge	3		ns	
t_{sh}	Hold time, SPI_SSN valid after SPI_SCLK active edge	1		ns	
t_{od}	Delay time, SPI_SCLK active edge to SPI_MISO shifted		38.7	ns	(2)
t_{oh}	Hold time, SPI MISO valid after SPI_SCLK active edge	31.2			(3)
t_{ds}	Setup time, SPI_MOSI valid before SPI_SCLK active edge	2		ns	
t_{dh}	Hold time, SPI_MOSI valid after SPI_SCLK active edge	1		ns	

(1) SPI_SCLK period should be at least 8 times as that of SPI module internal working clock in slave mode: T >= 8 Tm, Tm = 7.8ns

(2) t_{od} < 7.5+4Tm. In slave mode, SPI_SCLK is generated by external SPI device, so SPI need to do synchronization and glitch suppression before use. Time for synchronization and glitch suppression is 4 SPI module internal working clock period Tm. In the above table, Tm = 7.8ns

(3) t_{oh} > 4Tm. In slave mode, SPI_SCLK is generated by external SPI device, so SPI module need to do synchronization and glitch suppression before use. Time for synchronization and glitch suppression is 4 SPI module internal working clock period Tm. In the above table, Tm = 7.8ns

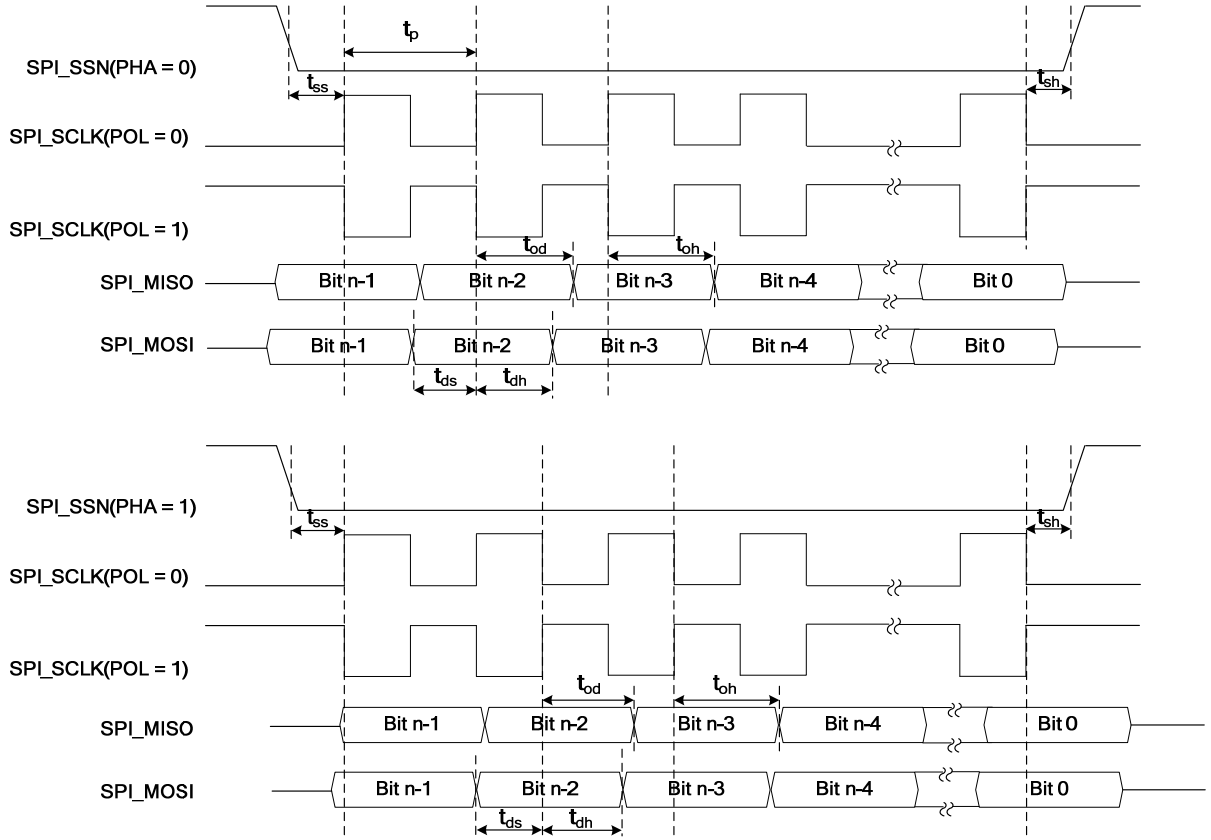

Figure 9-2 SPI Interface--Transmit and Receive in Slave Mode

SPI in Master Mode

Table 9-19 SPI Interface Electrical Characteristics (Master Mode)

Parameter		MIN	MAX	Unit	Notes
t_p	Cycle time, SPI_SCLK period	15.6		ns	(1)
t_{ss}	SPI_SSN active to SPI_SCLK first edge	62.4		ns	(2)
t_{sh}	SPI_SCLK last edge to SPI_SSN inactive	62.4		ns	(2)
t_{od}	Delay time, SPI_SCLK active edge to SPI_MOSI shifted		3.2	ns	
t_{oh}	Hold time, SPI_MOSI valid after SPI_SCLK active edge	-1		ns	
t_{ds}	Setup time, SPI_MISO valid before SPI_SCLK active edge	9.5		ns	
t_{dh}	Hold time, SPI_MISO valid after SPI_SCLK active edge	-3		ns	

(1) SPI_SCLK period should be at least 2 times as that of SPI module internal working clock in master mode: T >= 2 Tm

(2) Programmable by configuring SPI register, 4 SPI_SCLK period is default value and also for

recommendation. In the above table, SPI_SCLK period = 15.6ns

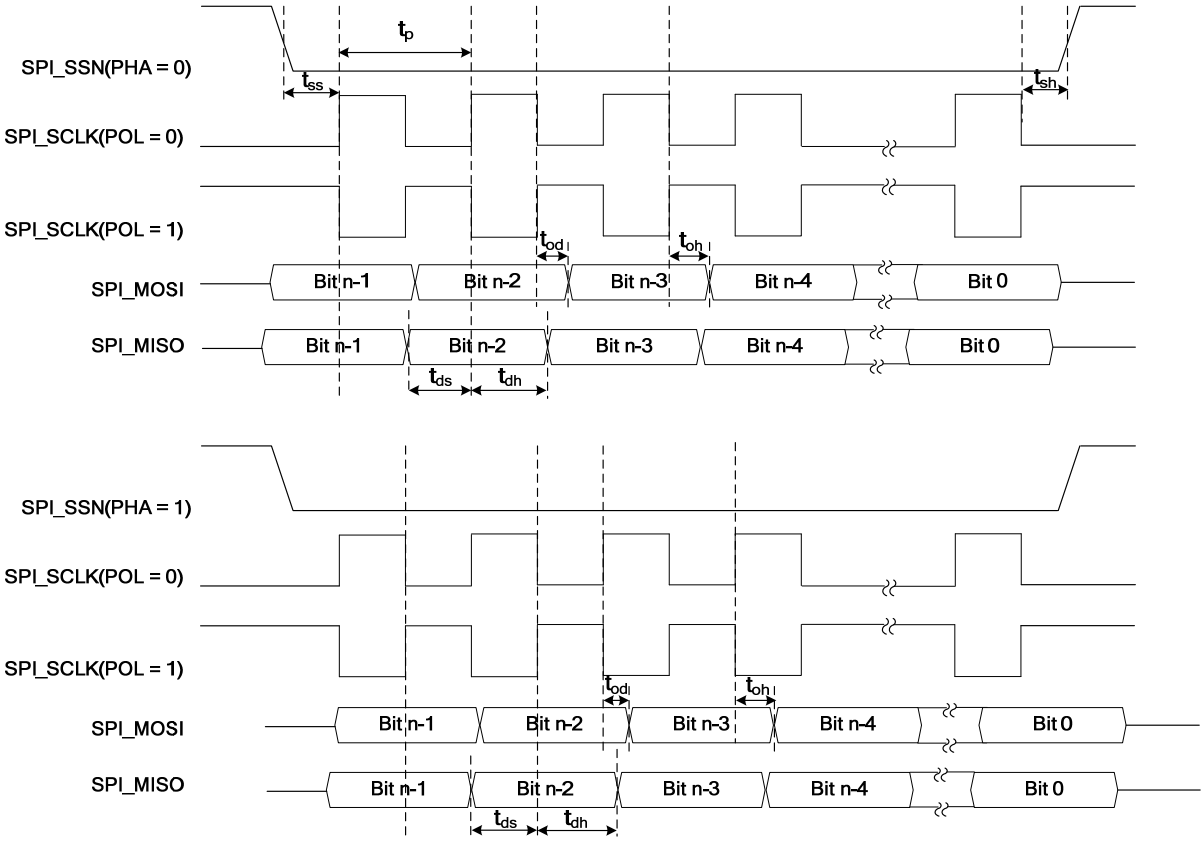

Figure 9-3 SPI Interface--Transmit and Receive in Master Mode

9.6 I2C Interface Timing

Table 9-20 I2C Interface Timing Conditions

Timing Condition Parameter		MIN	MAX	Unit
Input Conditions				
t_R	Input signal rise time	0.5	5	ns
t_F	Input signal fall time	0.5	5	ns
Output Condition				
C_{load}	Output load capacitance		20	pf

Table 9-21 I2C Interface Electrical Characteristics (Standard Mode)

Parameter		MIN	MAX	Unit
t_{CSCL}	Cycle time, SCL period	10		us
t_{WHSCL}	SCL high pulse width	4.0		us
t_{WLSCL}	SCL low pulse width	4.7		us
t_{S2SCL}	Setup time, SDA low to high when SCL high for stop bit	4.0		us
t_{H2SCL}	Hold time, SDA high to low when SCL high for start bit	4.0		us
t_{WBF}	I2C bus free time	4.7		us
t_{S2SDA}	SDA setup time	250		ns
t_{H2SDA}	SDA hold time	0		ns

Table 9-22 I2C Interface Electrical Characteristics (Fast Mode)

Parameter		MIN	MAX	Unit
t_{CSCL}	Cycle time, SCL period	2.5		us
t_{WHSCL}	SCL high pulse width	0.6		us
t_{WLSCL}	SCL low pulse width	1.3		us
t_{S2SCL}	Setup time, SDA low to high when SCL high for stop bit	0.6		us
t_{H2SCL}	Hold time, SDA high to low when SCL high for start bit	0.6		us
t_{WBF}	I2C bus free time	1.3		us
t_{S2SDA}	SDA setup time	100		ns
t_{H2SDA}	SDA hold time	0		ns

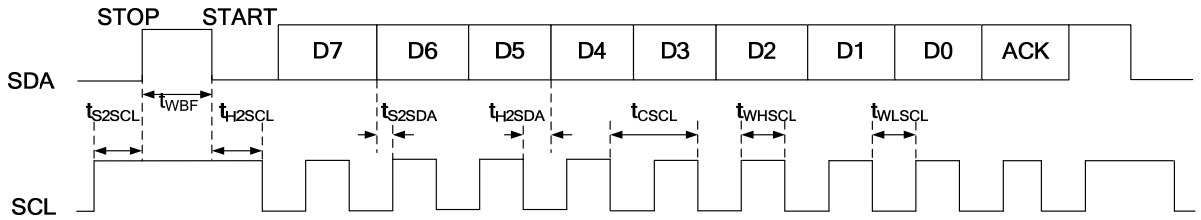

Figure 9-4 I2C Interface Timing

9.7 SDIO Interface Timing

Table 9-23 SDIO Interface Timing Conditions

Timing Condition Parameter		MIN	MAX	Unit
Input Conditions				
t_R	Input signal rise time	0.5	5	ns
t_F	Input signal fall time	0.5	5	ns
Output Condition				
C_{load}	Output load capacitance		40	pf

Table 9-24 SDIO Interface Electrical Characteristics

Parameter		MIN	MAX	Unit	Notes
t_p	Cycle time, SD_CLK period	20		ns	
t_w	Duration time, SD_CLK high	8		ns	(1)
t_{su}	Setup time, input data valid before SD_CLK active edge	4.6		ns	
t_{IH}	Hold time, input data valid after SD_CLK active edge	0		ns	
t_{OD}	Delay time, SD_CLK active edge to data output transition		12	ns	(2)
t_{OH}	Hold Time, data output valid after SD_CLK active edge	2		ns	(2)
t_{CMDD}	Delay time, SD_CLK active edge to command output transition		12	ns	(2)
t_{CMDH}	Hold Time, command output valid after SD_CLK active edge	2		ns	(2)

(1) Duty cycle of SDIO_CLK is 40% of the clock cycle.
(2) The same value in both normal and high speed mode

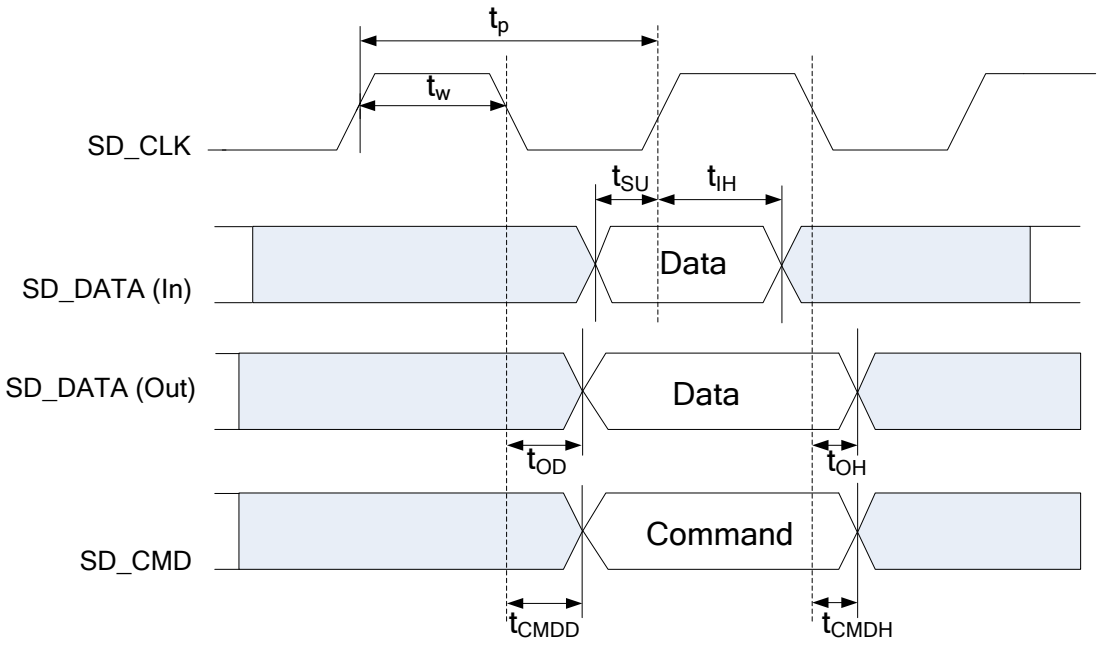

Figure 9-5 SDIO Interface Normal Timing

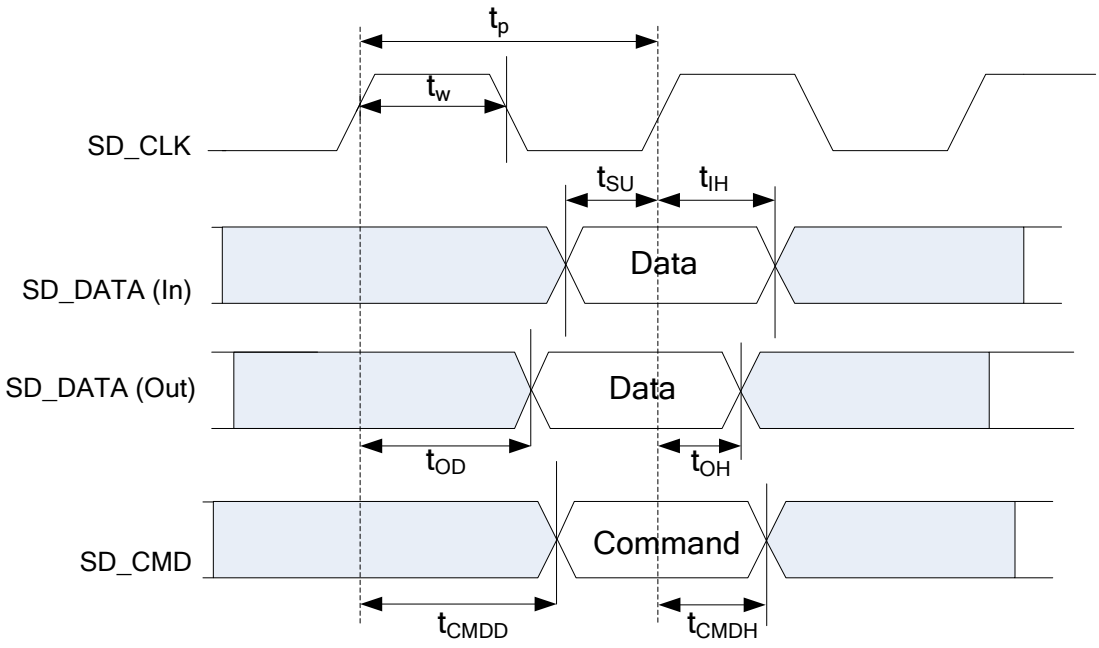

Figure 9-6 SDIO Interface High Speed Timing

9.8 NFC Interface Timing

Table 9-25 NFC Interface Timing Conditions

Timing Condition Parameter		MIN	MAX	Unit
Input Conditions				
t_R	Input signal rise time	0.5	5	ns
t_F	Input signal fall time	0.5	5	ns
Output Condition				
C_{load}	Output load capacitance		40	pf

Table 9-26 NFC Interface Electrical Characteristics

Parameter		MIN	MAX	Unit	Notes
t_{WC}	WEN cycle time	20		ns	(1)
t_{WP}	WEN pulse width	9		ns	
t_{RP}	REN pulse width	20		ns	(1)
t_{RC}	REN cycle time	9		ns	
t_{CLS}	CLE setup time	80		ns	(2)
t_{CLH}	CLE hold time	80		ns	(2)
t_{CS}	CEN setup time	80		ns	(2)
t_{CH}	CEN hold time	80		ns	(2)
t_{ALS}	ALE setup time	80		ns	(2)
t_{ALH}	ALE hold time	80		ns	(2)
t_{DOS}	Data output setup time	10		ns	
t_{DOA}	Data output delay time for access		2	ns	
t_{DOH}	Data output hold time	8.6		ns	(3)
t_{DIS}	Data input setup time	3.3		ns	
t_{DIH}	Data input hold time	0		ns	

(1) Related to the output maximum frequency supported by the NFC module.

(2) Programmable by configuring NFC register, as least 4 write/read cycles are for recommendation. In the above table, write/read cycle period = 20ns.

(3) t_{DOH} > -0.365 + min (t_{WP}), relative to the rise edge of WEN, the actual output delay time shall be combined with 1/2 of write cycle time, i.e., the minimum write pulse, here min (t_{WP}) = 9ns.

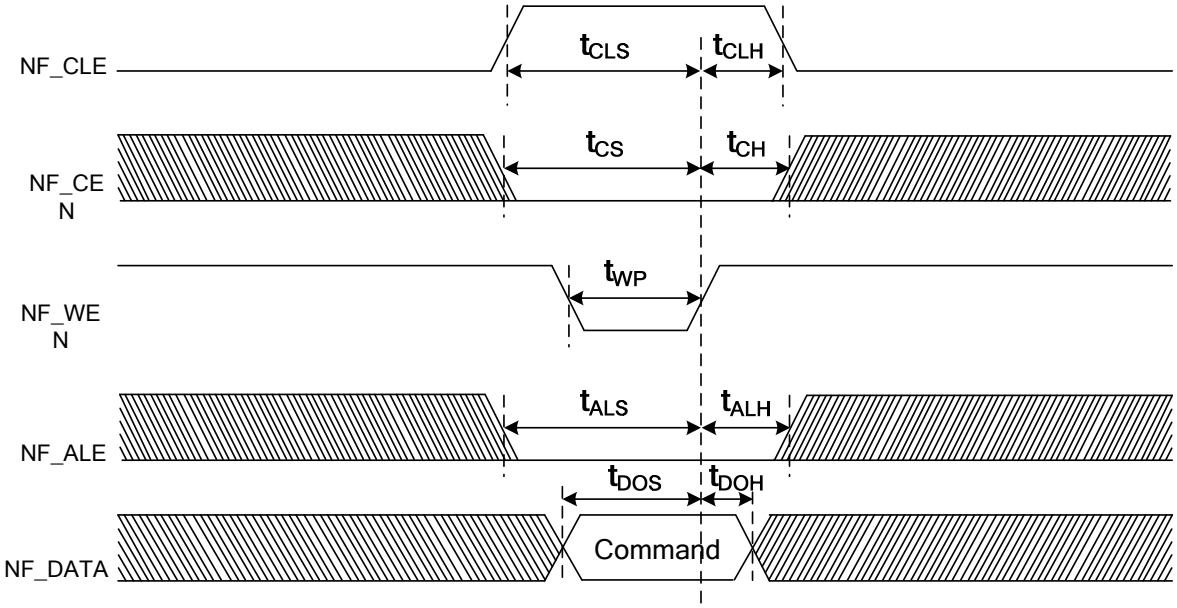

Figure 9-7 NFC Command Latch Timing

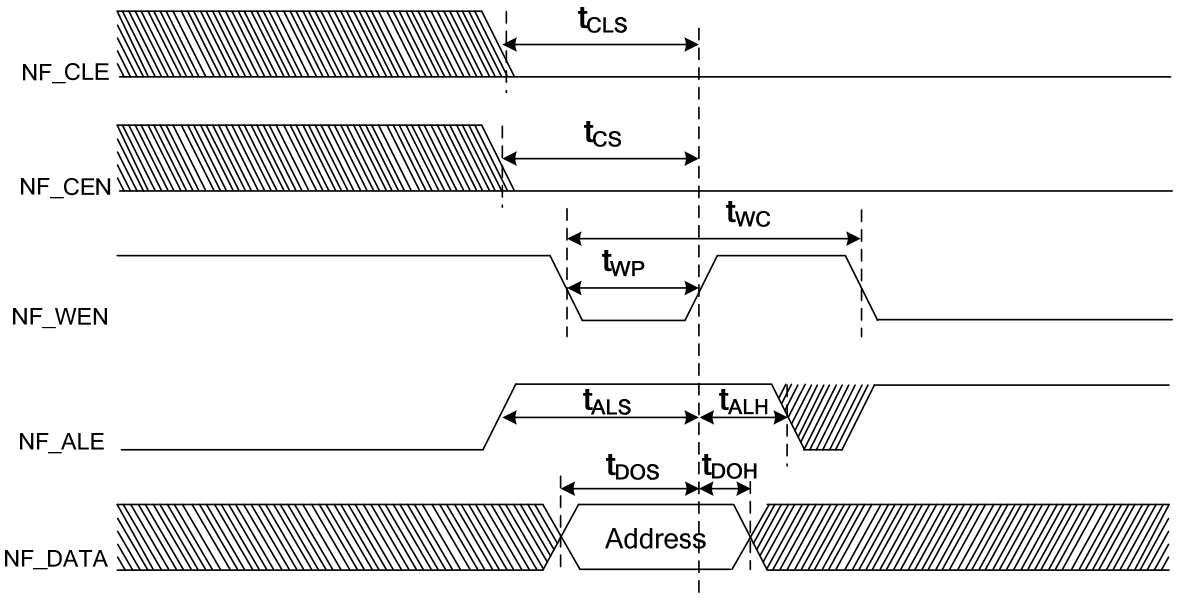

Figure 9-8 NFC Address Latch Timing

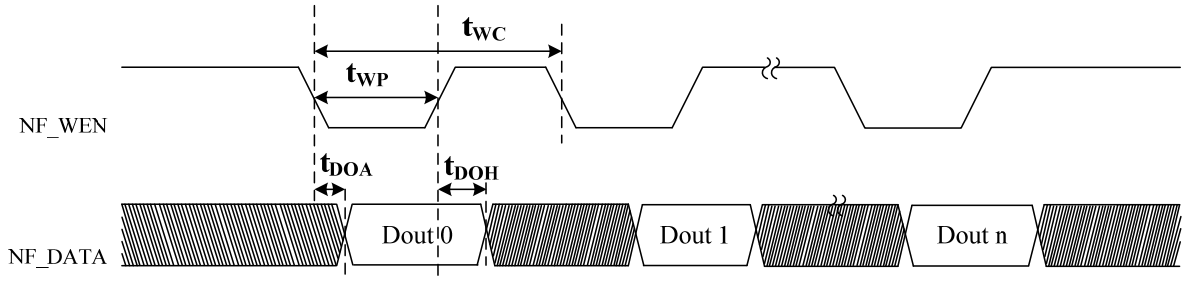

Figure 9-9 NFC Data Output Timing

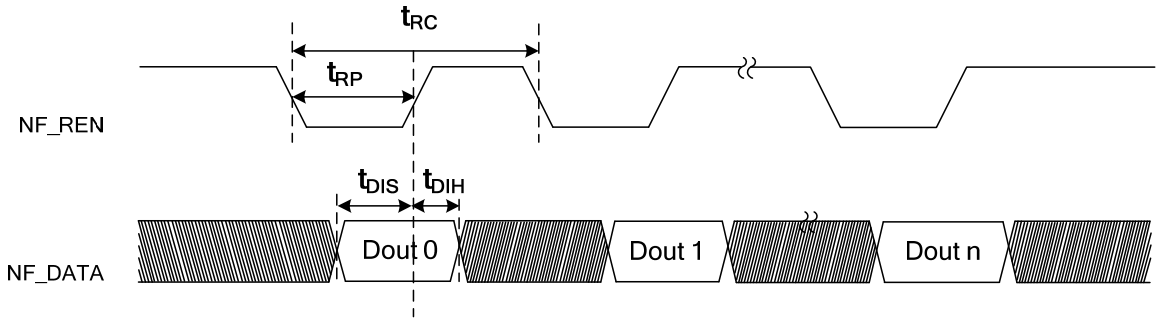

Figure 9-10 NFC Standard Data Input Timing

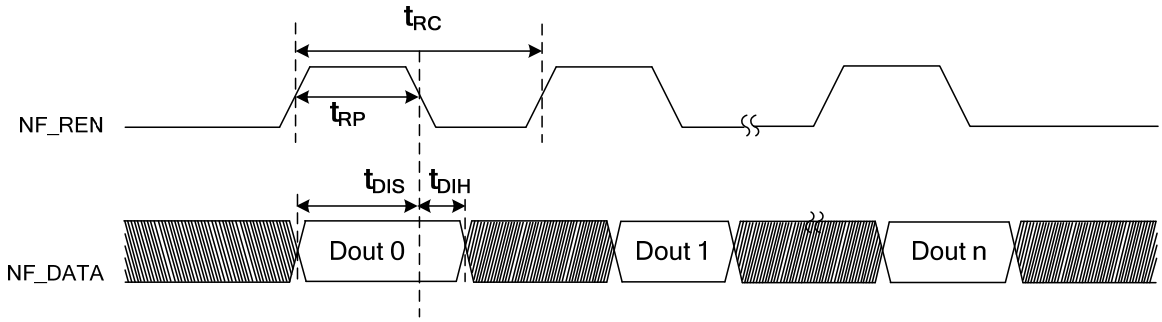

Figure 9-11 NFC EDO Data Input Timing

9.9 AUD Interface Timing

Table 9-27 Audio Interface Timing Conditions

Timing Condition Parameter		MIN	MAX	Unit
Input Conditions				
t_R	Input signal rise time	0.5	5	ns
t_F	Input signal fall time	0.5	5	ns
Output Condition				
C_{load}	Output load capacitance		20	pf

Table 9-28 Audio Interface Electrical Characteristics

Parameter		MIN	MAX	Unit	Notes
t_{sclk}	AUD_SCK period	162.5	1953	ns	(1)
t_{wsdly}	Delay time, AUD_SCK active edge to AUD_WS transition	1	6.2	ns	
t_{sdodly}	Delay time, AUD_SCK active edge to AUD_SDO_DAC transition	1	8.6	ns	
t_{sdistp}	AUD_SDI_ADC setup time	11.2		ns	
t_{sdihld}	AUD_SDI_ADC hold time	0		ns	

(1) AUD_SCK = 64 x fs , where max(fs) = 96KHz and min(fs) = 8KHz. (fs means frequency of sample)

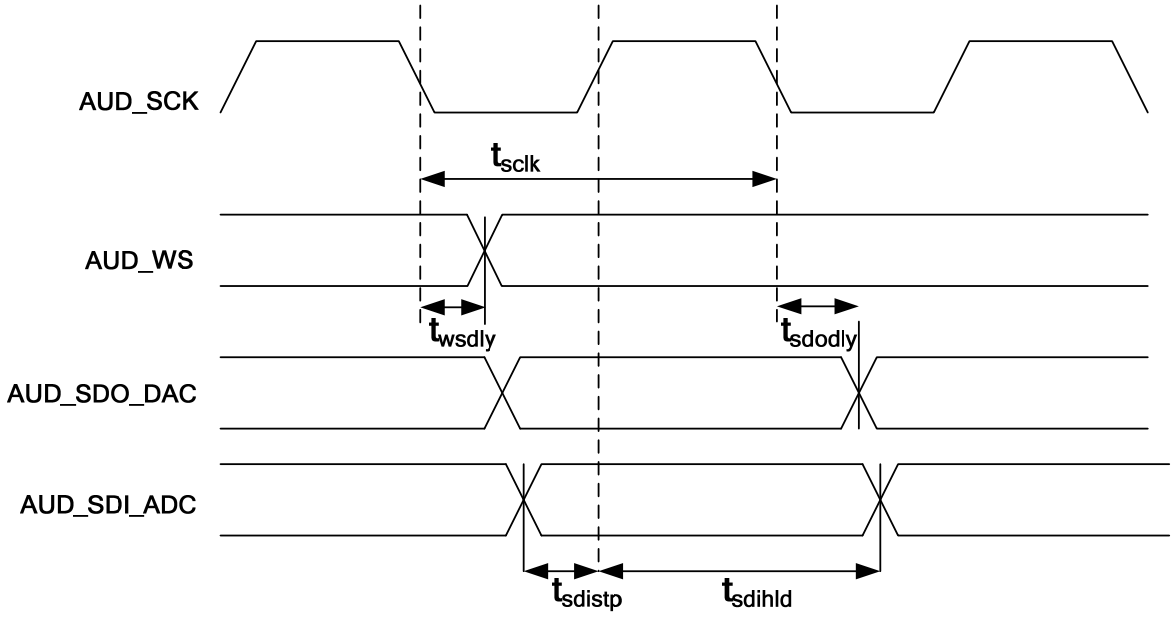

Figure 9-12 Timing Specification of I2S/PCM Serial Interface to External Devices

9.10 LCD Interface Timing

Table 9-29 LCD Interface Timing Conditions

Timing Condition Parameter		MIN	MAX	Unit
Input Conditions				
t_R	Input signal rise time	0.5	5	ns
t_F	Input signal fall time	0.5	5	ns
Output Condition				
C_{load}	Output load capacitance		20	pf

LCD Serial Interface

Table 9-30 LCD Interface Electrical Characteristics (Serial Interface)

Parameter		MIN	MAX	Unit	Notes
t_{LSCL}	SCL low level pulse width	40		ns	(1)(2)
t_{HSCL}	SCL high level pulse width	40		ns	(1)(3)
t_{DS}	SDA setup time	30.5		ns	(1)(4)
t_{DH}	SDA hold time	30		ns	(1)(5)
t_{CSS}	CS setup time	30.5		ns	(1)(6)
t_{CSH}	CS hold time	36		ns	(1)(7)
t_{AS}	DCX setup time	29		ns	(1)(8)
t_{AH}	DCX hold time	30		ns	(1)(9)

(1) The setup and hold time can be configured by the internal register of VC0882, the value listed in the table are the parameter range which VC0882 can support at most, the hold/setup need of the panel should not exceed the max hold/setup value. The value in the table above is calculated when T_{PCLK} is 40ns. PCLK is the refresh clock of panel.

(2) The width of t_{LSCL} is n*T_{PCLK}, in which n can be configured between 1 and 128 by the internal register SCK_WIDTH.

(3) The width of t_{HSCL} is n* T_{PCLK}, in which n can be configured by the internal register SCK_WIDTH.

(4) The SDA setup time t_{DS} = n* T_{PCLK} -9.5, in which n can be configured from 1 to 128 by the internal register SCK_WIDTH. For example, if the panel need of SDA setup time is 120ns and T_{PCLK} is 40ns, so we can configure the n to 4 or even larger. For n=5, the t_{DS} =150.5ns, which is larger than 120ns.

(5) The SDA hold time t_{DH} = n* T_{PCLK} -10, in which n can be configured from 1 to 128 by the internal register SCK_WIDTH. We should configure the n parameter according to the panel need. For example, if the panel need of SDA hold time is 120ns and T_{PCLK} is 40ns, so we can configure the n to 4 or even larger. For n=4, the t_{DH} =150ns, which is larger than 120ns.

(6) The CS setup time t_{CSS} = n* T_{PCLK} -9.5, in which n can be configured from 1 to 128 by the internal register

SCK_WIDTH.

(7) The CS hold time t_{CSH} = n* T_{PCLK} -4, in which n can be configured from 1 to 128 by the internal register SCK_WIDTH.

(8) The DCX setup time t_{AS} = n* T_{PCLK} -11, in which n can be configured from 1 to 128 by the internal register SCK_WIDTH.

(9) The DCX hold time t_{AH} = n* T_{PCLK} -10, in which n can be configured from 1 to 128 by the internal register SCK_WIDTH.

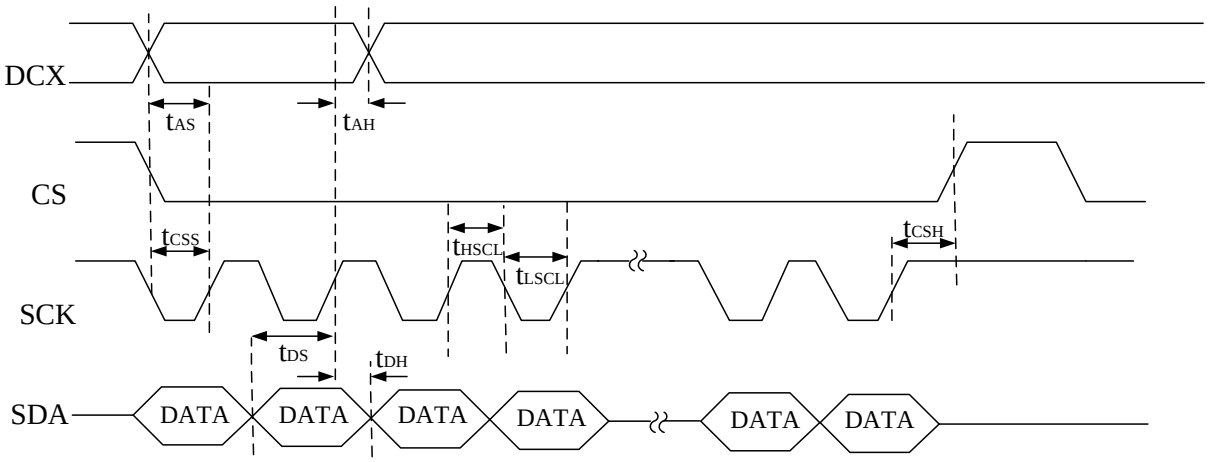

Figure 9-13 LCD Serial Interface Timing

Data Output for DPI Panel

Table 9-31 LCD Interface Electrical Characteristics (Data Output for DPI Panel)

Parameter		MIN	MAX	Unit	Notes
t_p	LCD_PCLK period	6.17		ns	
t_{duty}	LCD_PCLK output clock duty cycle	40%	60%		
t_{odr}	Delay time, LCD_PCLK rise edge to data transition		2.7	ns	
t_{ohf}	Hold time, data valid after LCD_PCLK fall edge	1.74		ns	(1)
t_{odf}	Delay time, LCD_PCLK fall edge to data transition		2.9	ns	
t_{ohr}	Hold time, data valid after LCD_PCLK rise edge	1.88		ns	(2)

(1) $t_{ohf} > -0.72 + 1/2t_p$, relative to the next edge of LCD_PCLK, the actual output delay time shall be combined with 1/2 of pixel cycle time, the duty cycle 40% shall also be considered.

(2) $t_{ohr} > -0.58 + 1/2t_p$, relative to the next edge of LCD_PCLK, the actual output delay time shall be combined with 1/2 of pixel cycle time, the duty cycle 40% shall also be considered.

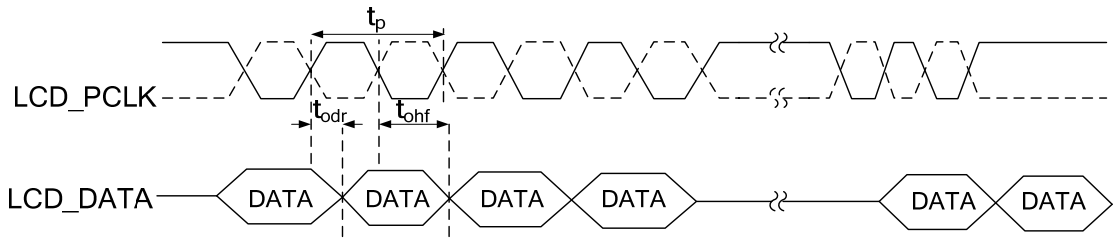

Figure 9-14 Data Output Timing for DPI Panel (falling edge capture)

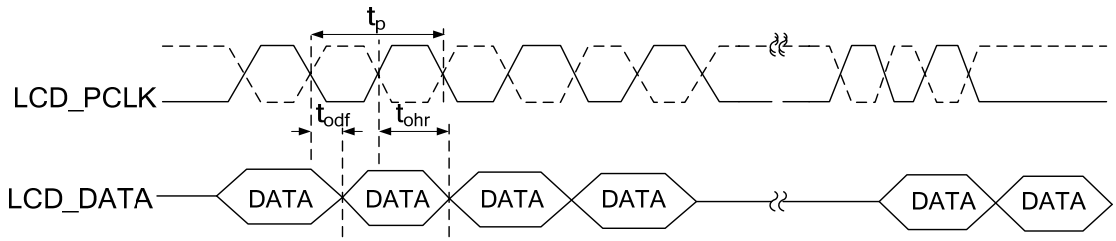

Figure 9-15 Data Output Timing for DPI Panel (rising edge capture)

Interface Timing with DBI Panel

DBI Write Operation

Table 9-32 LCD Interface Electrical Characteristics (DBI Panel for Write Operation)

Parameter		MIN	MAX	Unit	Notes
t_{WLW}	Write low level pulse width	40		ns	(1)(2)
t_{WHW}	Write high level pulse width	40		ns	(1)(3)
t_{AS}	Address setup time	35.5		ns	(1)(4)
t_{AH}	Address hold time	37		ns	(1)(5)
t_{DSW}	Write data setup time	35.5		ns	(1)(6)
t_{DHW}	Write data hold time	30.5		ns	(1)(7)
t_{CS}	Chip select setup time	35		ns	(1)(8)
t_{CH}	Chip select hold time	37		ns	(1)(9)

(1) The setup and hold time can be configured by the internal register of VC0882, the value listed in the table are the parameter range which VC0882 can support at most, the hold/setup need of the panel should not exceed the max hold/setup value. The value in the table above is calculated when T_{PCLK} is 40ns. PCLK is the internal working clock of LCDIF module.

(2) The width of t_{WLW} is n*T_{PCLK}, in which n can be configured from 1 to 31 by the internal register WRC.

(3) The width of t_{WHW} is n*T_{PCLK}, in which n can be configured from 1 to 62 by the internal register WSC and DHC

(4) The Address setup time t_{AS} = n*T_{PCLK} -4.5, in which n can be configured from 1 to 31 by the internal register

WSC. If the panel setup need is 100ns, n can be configured to 3, then the t_{AS} = (3*40 -4.5) = 115.5n, which is larger then 100n.

(5) The Address hold time t_{AH} = n*T_{PCLK} -3, in which n can be configured from 1 to 31 by the internal register DHC. If the panel setup need is 60ns, n can be configured to 2, then the t_{AH} = (2*40 -3) = 87n, which is larger then 60n.

(6) The Write data setup time t_{DSW} = n*T_{PCLK} - 4.5, in which n can be configured from 1 to 62 by the internal register WSC and WRC.

(7) The Write data hold time t_{DHW} = n*T_{PCLK} - 9.5, in which n can be configured from 1 to 31 by the internal register DHC.

(8) The Chip select setup time during write t_{CS} = n*T_{PCLK} - 5, in which n can be configured from 1 to 62 by the internal register WSC and WRC.

(9) The Chip select hold time t_{CH} = n*T_{PCLK} - 3, in which n can be configured from 1 to 31 by the internal register DHC.

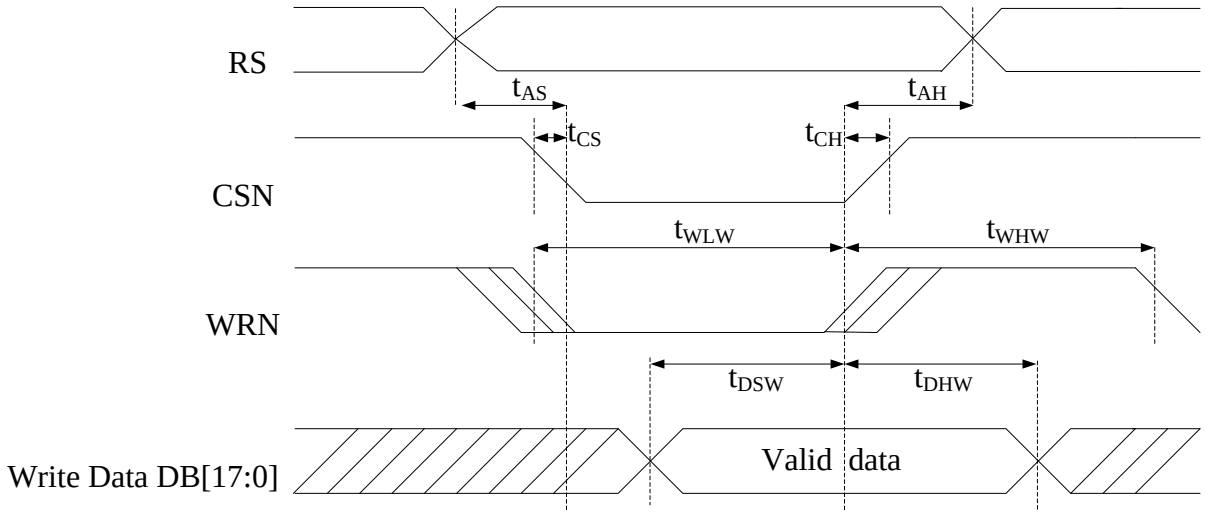

Figure 9-16 LCD Interface Timing for DBI Panel (Write Operation)

DBI Read Operation

Table 9-33 LCD Interface Electrical Characteristics (DBI Panel for Read Operation)

Parameter		MIN	MAX	Unit	Notes
t_{RLW}	Read low level pulse width	40		ns	(1)(2)
t_{RHW}	Read high level pulse width	40		ns	(1)(3)
t_{AS}	Address setup time	35.5		ns	(1)(4)
t_{AH}	Address hold time	38.5		ns	(1)(5)
t_{RACC}	Read data access time	10		ns	(1)(6)
t_{DH}	Read data hold time	-15		ns	(1)(7)
t_{CS}	Chip select setup time	35		ns	(1)(8)
t_{CH}	Chip select hold time	38		ns	(1)(9)

(1) The setup and hold time can be configured by the internal register of VC0882, the value listed in the table are

the parameter range which VC0882 can support at most, the hold/setup need of the panel should not exceed the max hold/setup value. The value in the table above is calculated when T_{PCLK} is 40ns. PCLK is the internal working clock of LCDIF module.

(2) The width of t_{RLW} is n*T_{PCLK}, in which n can be configured from 1 to 31 by the internal register RAC.

(3) The width of t_{RHW} is n*T_{PCLK}, in which n can be configured from 1 to 62 by the internal register RAC and ROC.

(4) The Address setup time during Read t_{AS} = n*T_{PCLK} -4.5, in which n can be configured from 1 to 31 by the internal register RSC. If the panel setup need is 100ns, n can be configured to 3, then the t_{AS} = (3*40 -4.5) = 115.5n, which is larger then 100n.

(5) The Address hold time during Read t_{AH} = n*T_{PCLK} -1.5, in which n can be configured from 1 to 31 by the internal register DHC. If the panel setup need is 60ns, n can be configured to 2, then the t_{AH} = (2*40 -1.5) = 78.5n, which is larger then 60n.

(6) The Read data access time we can tolerate is t_{RACC} = n*T_{PCLK} -30, in which n can be configured from 1 to 31 by the internal register RAC. The panel access time should not exceed t_{RACC}. For example, if the panel access time is 100n, the n can be configured to 4 or larger. When n=4, t_{RACC} =130ns, which is larger than 100ns.

(7) The Read data hold time t_{DH} = -15, which means the read data output from panel can be ahead of the posedge of RD 15ns.

(8) The Chip select setup time during Read t_{CS} = n*T_{PCLK} -5, in which n can be configured from 1 to 62 by the internal register RAC and RSC.

(9) The Chip select hold time during Read t t_{CH} = n*T_{PCLK} -2, in which n can be configured from 1 to 31 by the internal register ROC.

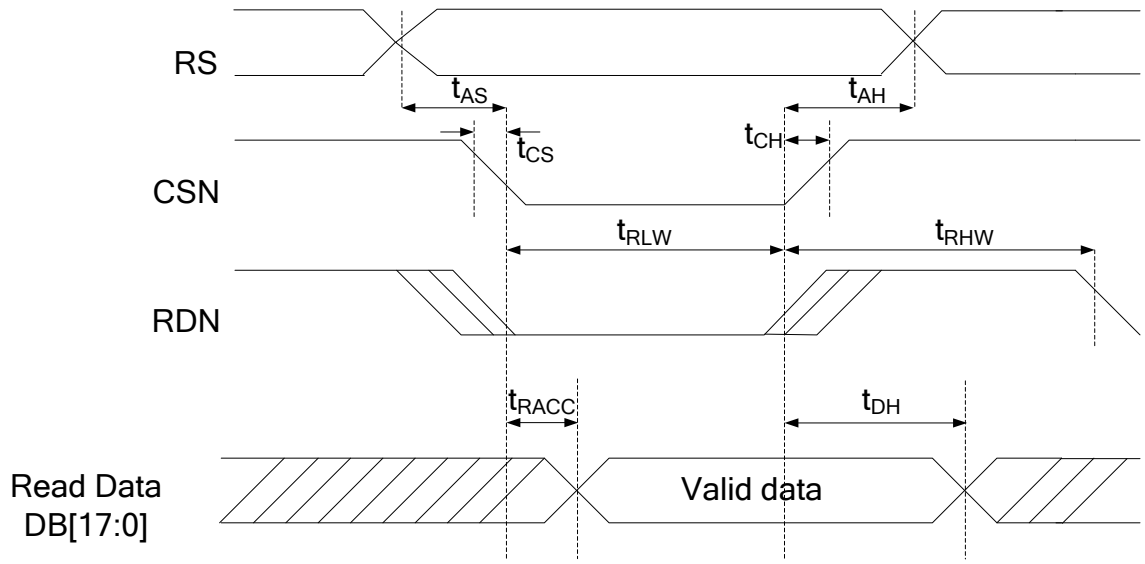

Figure 9-17 LCD Interface Timing for DBI Panel (Read Operation)