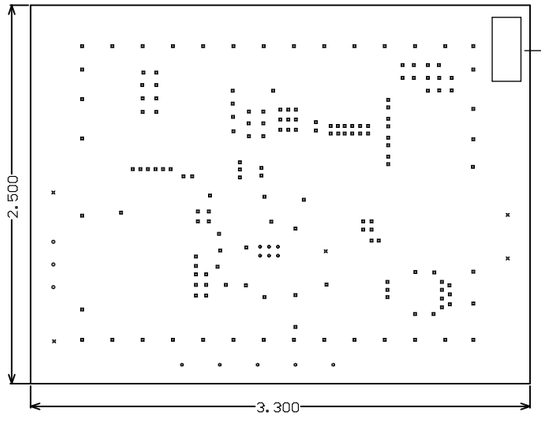
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric1		8.00mil	4.2	
5	Inner Layer 1	Copper	2.80mil		
6	Dielectric 3		36.80mil	4.2	
7	Inner Layer 2	Copper	2.80mil		
8	Dielectric 2		8.00mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



PLACE MFGRS LOGO, UL FLAMMABILITY RATING, Tg TEMP, AND DATE CODE HERE BOTTOM SIDE

Symbol	Quantity	Finished Hole Size	Plated	Hole Type
	6	8.00mil (0.203mm)	PTH	Round
	162	12.00mil (0.305mm)	PTH	Round
	5	40.00mil (1.016mm)	PTH	Round
	3	43.31mil (1.100mm)	PTH	Round
	5	98.43mil (2.500mm)	PTH	Round
	181 Total			

DESIGN INFORMATION

MIN. TRACK WIDTH: 10 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 20 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

MATERIAL: 4 Layer Board
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH MIN COPPER THICKNESS: [X] 1MIL [ ] OTHER _____
BOARD FINISH:
SILKSCREEN: [X] TOP [ ] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR:
[X] GREEN [ ] BLUE [ ] OTHER _____
SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG
[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____
ARRAY/PANEL: [X] CUT AND TRIM PER MECH LAYER 1
[ ] N.C. ROUTE [ ] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] UL 94V-0 [X] RoHS [ ] OTHER _____
ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [X] NONE [ ] REQUIRED [ ] PER ORDER
MANUFACTURER'S UL: [ ] RAIL [ ] METAL [X] SILK

TEXAS INSTRUMENTS

PROJECT TITLE: TPS92691 SEPIC LED Driver
DESIGNED FOR: Public Release
FILE NAME: PMP15027_E3.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PMP15027	REV: E3	SVN REV: Not In VersionControl
LAYER NAME = [illegible]ions			
PLOT NAME = Fabrication Drawing	GENERATED : 6/30/2017 3:46:15 PM	TEXAS INSTRUMENTS	

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

ENGINEER:	LAYOUT BY:
Clint Jensen	Kerry Murphy
SCALE: 1.00	ALTIUM DESIGNER VERSION: 16.1.9.221