LDC1000 电感数字转换器

查询样品: LDC1000

特性

- 无磁体操作
- 亚微米高精度
- 可调感测范围（通过线圈设计实现）
- 更低的系统成本
- 远程传感器放置（从恶劣环境中将 **LDC** 去耦合）
- 高耐久性（借助于遥控操作）
- 对于环境干扰的不敏感性（诸如污垢、灰尘、水、油）
- 电源电压，模拟：**4.75V** 至 **5.25V**
- 电源电压，**IO**：**1.8V** 至 **5.25V**
- 电源电流（无 **LC** 谐振回路）：**1.7mA**
- **Rp** 分辨率：**16** 位
- **L** 分辨率：**24** 位
- **LC** 频率范围：**5kHz** 至 **5MHz**

应用范围

- 电传线控系统
- 轮齿计数
- 流量计
- 按钮开关
- 笔记本电脑
- 游戏控制器
- 多功能打印机
- 数码照相机
- 医疗设备

说明

电感感测是一种遥控的、短程感测技术，此项技术能够在灰尘、污垢、油和潮湿环境中实现导体目标的低成本、高分辨率感测，这使得它在恶劣环境中非常可靠。通过使用可在印刷电路板 (PCB) 上被创建为一个感测元件的线圈，LDC1000 可实现超低成本系统解决方案。

电感感测技术可实现线性/角位置、位移、运动、压缩、振动、金属成分以及市面上包括汽车、消费类、计算机、工业用、医疗用和通信应用在内的很多其它应用的高精度测量。 电感感测以低于其它竞争对手解决方案的成本提供更佳的性能和可靠性。

LDC1000 是世界上第一个电感数字转换器，从而在一个低功耗、小封装尺寸解决方案内提供电感感测的优势。 此产品采用一个小外形尺寸无引线 (SON)-16 封装，并且提供了几种运行模式。 一个串行外设接口 (SPI) 简化了到微控制器 (MCU) 的连接。

TYPICAL APPLICATION

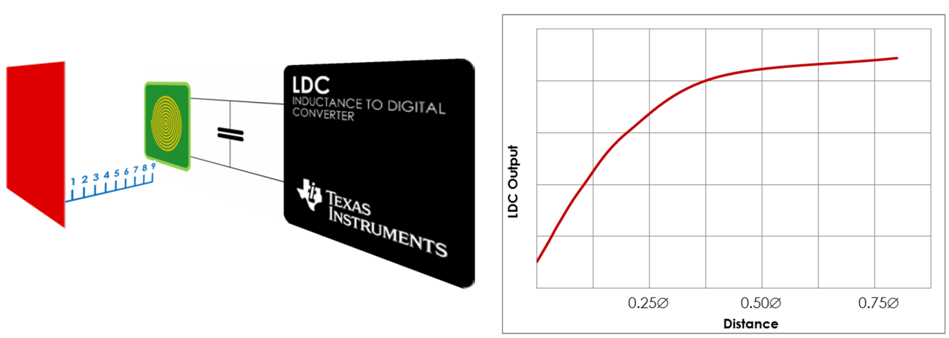

Figure 1. Axial Distance Sensing

English Data Sheet: SNOSCX2

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BLOCK DIAGRAM

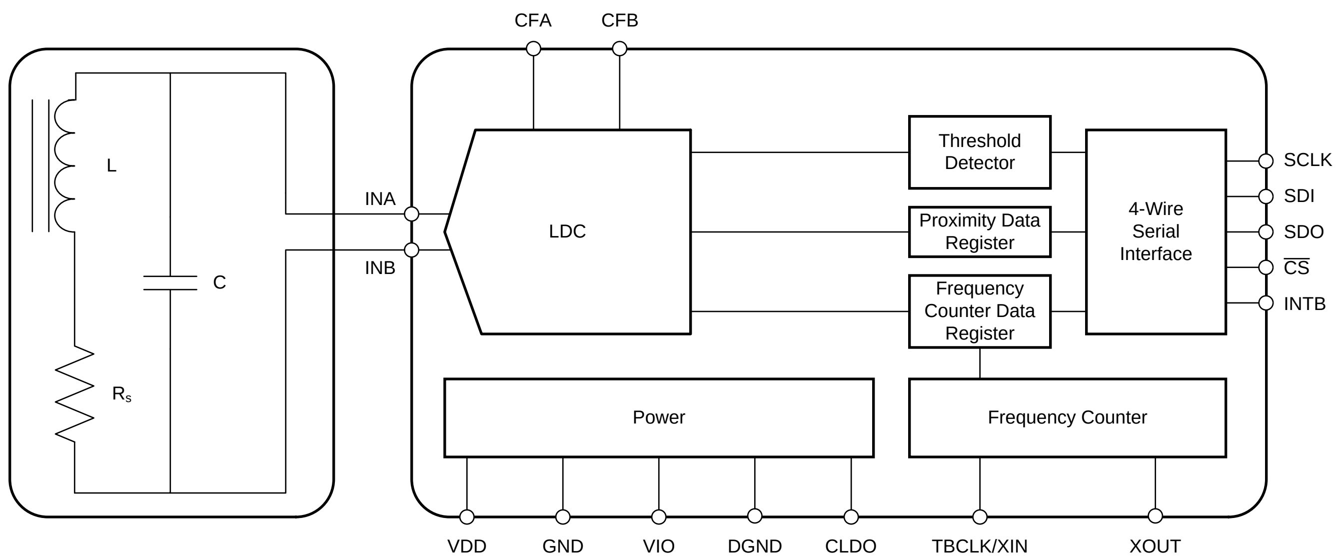

Figure 2. LDC1000 Block Diagram

TYPICAL APPLICATION SCHEMATIC

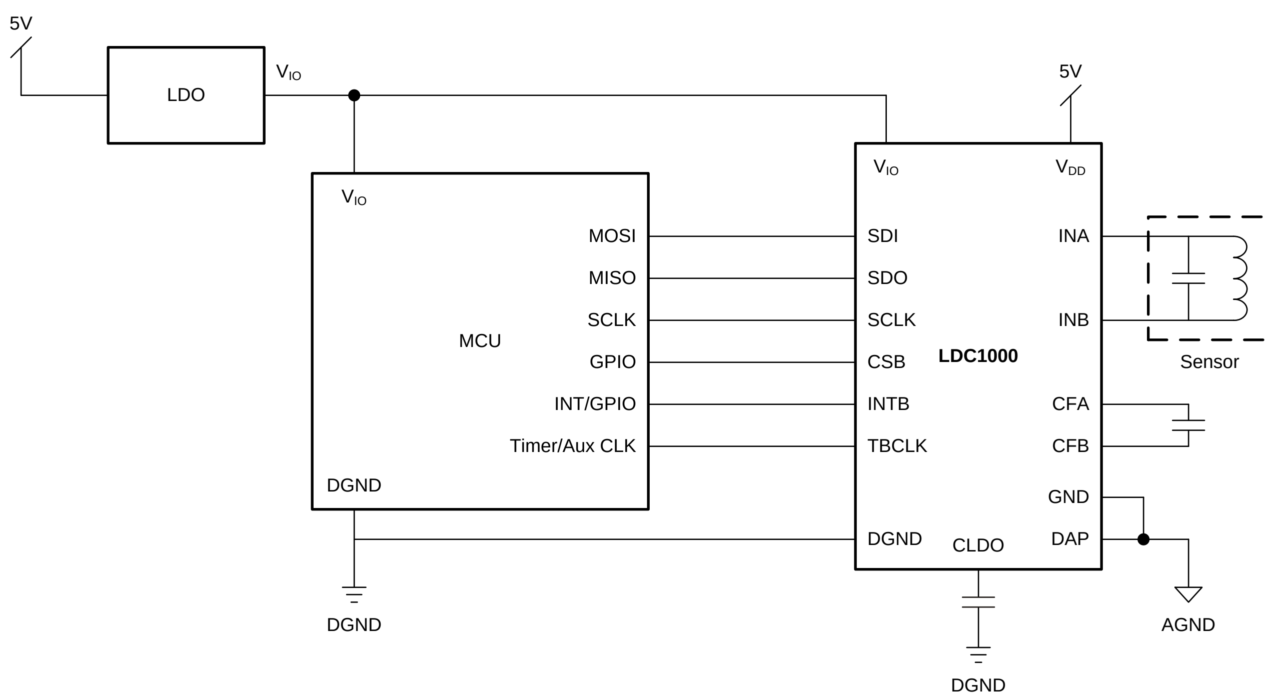

Figure 3. Typical Application Schematic

CONNECTION DIAGRAM

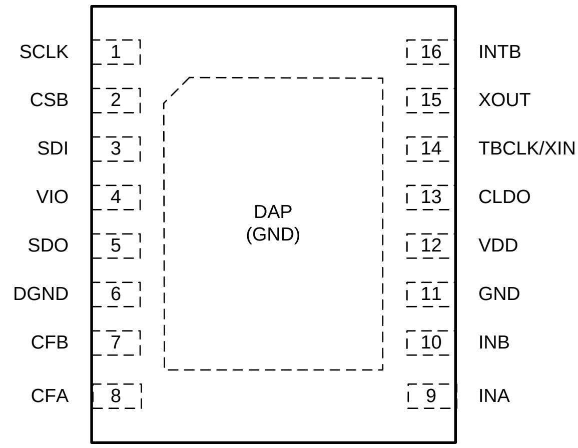

Figure 4. LDC1000 Pin Diagram SON-16

Table 1. Pin Description(1)

PIN NAME	PIN NO.	PIN TYPE	FUNCTION
SCLK	1	DO	SPI clock input. SCLK is used to clock-out/clock-in the data from/into the chip
CSB	2	DI	SPI CSB. Multiple devices can be connected on the same SPI bus and CSB can be used to select the device to be communicated with
SDI	3	DI	SPI Slave Data In (Master Out Slave In). This should be connected to the Master Out Slave In of the master
VIO	4	P	Digital IO Supply
SDO	5	DO	SPI Slave Data Out (Master In Slave Out).It is high-z when CSB is high
DGND	6	P	Digital ground
CFB	7	A	LDC filter capacitor
CFA	8	A	LDC filter capacitor
INA	9	A	External LC Tank. Connected to external LC tank
INB	10	A	External LC Tank. Connected to external LC tank
GND	11	P	Analog ground
VDD	12	P	Analog supply
CLDO	13	A	LDO bypass capacitor. A 56nF capacitor should be connected from this pin to GND
TBCLK/XIN	14	DI/A	External time-base clock/XTAL. Either an external clock or crystal can be connected
XOUT	15	A	XTAL. Crystal out. Recommended to connect 8Mhz crystal between XIN and XOUT with 20pF cap from each pin to ground. Should be floating when external clock is used
INTB	16	DO	Configurable interrupt. This pin can be configured to behave in 3 different ways by programing the INT pin mode register. Either threshold detect, wakeup, or DRDYB
DAP	17	P	Connect to GND

(1) DO: Digital Output, DI: Digital Input, P: Power, A: Analog

ABSOLUTE MAXIMUM RATINGS(1)

ESD Tolerance(2)	Human Body Model	1kV
	Charge Device Model	250V
Analog Supply Voltage (VDD – GND)		6V
IO Supply Voltage (VIO – GND)		6V
Voltage on any Analog Pin		-0.3V to VDD + 0.3V
Voltage on any Digital Pin		-0.3V to VIO + 0.3V
Input Current on INA and INB		8mA
Junction Temperature, TJ(3)		+150°C
Storage Temperature Range , T_{stg}		-65°C to +150°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
(3) The maximum power dissipation is a function of TJ(MAX), θJA, and the ambient temperature, TA. The maximum allowable power dissipation at any ambient temperature is PDMAX = (TJ(MAX) - TA)/ θJA. All numbers apply for packages soldered directly onto a PC board. The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	MAX	UNIT
Analog Supply Voltage (VDD – GND)		4.75	5.25	V
IO Supply Voltage (VIO – GND)		1.8	5.25	V
VDD-VIO		>=0		V
Operating Temperature, TA		-40	125	°C
Package Thermal Resistance(2)	SON (θ_{JA})		28	°C/W

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of TJ(MAX), θJA, and the ambient temperature, TA. The maximum allowable power dissipation at any ambient temperature is PDMAX = (TJ(MAX) - TA)/ θJA. All numbers apply for packages soldered directly onto a PC board. The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS[(1)]

Unless otherwise specified, all limits ensured for TA = TJ = 25°C, VDD = 5.0V, VIO = 3.3V[(2)]

SYMBOL	PARAMETER	CONDITIONS/ COMMENTS	MIN[(3)]	TYP[(4)]	MAX[(3)]	UNITS
POWER						
V_{DD}	Analog Supply Voltage		4.75	5	5.25	V
V_{IO}	IO Supply Voltage	VIO≤VDD	1.8	3.3	5.25	V
I_{DD}	Supply Current, VDD	Does not include LC tank current		1.7	2.3	mA
I_{VIO}	IO Supply Current	Static current			14	uA
I_{DD_LP}	Low-Power Mode Supply Current	With out LC Tank		250		uA
t_{START}	Start-Up Time	From POR to ready-to-convert. Crystal not used for frequency counter		2		ms
LDC						
f_{sensor_MIN}	Minimum sensor frequency			5		kHz
f_{sensor_MAX}	Maximum sensor frequency			5		MHz
A_{sensor_MIN}	Minimum sensor amplitude			1		VPP
A_{sensor_MAX}	Maximum sensor amplitude			4		VPP
t_{REC}	Recovery time	Oscillation start-up time after RP under-range condition		10		$1/f_{sensor}$
R_{p_MIN}	Minimum Sensor Rp Range			798		Ω
R_{p_MAX}	Maximum Sensor Rp Range			3.93M		Ω
R_{p_RES}	Rp Measurement Resolution			16		Bits
t_{S_MIN}	Minimum Response Time	Minimum programmable settling time of digital filter		$192\times1/f_{sensor}$		s
t_{S_MAX}	Maximum Response Time	Maximum programmable settling time of digital filter		$6144\times1/f_{sensor}$		s
EXTERNAL CLOCK/CRYSTAL FOR FREQUENCY COUNTER						
Crystal	Frequency			8		MHz
	Startup time			30		ms
External Clock	Frequency				8	MHz
	Clock Input High Voltage				V_{IO}	V

(1) Electrical Characteristics Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that TJ = TA. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where TJ > TA. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) The maximum power dissipation is a function of TJ(MAX), θJA, and the ambient temperature, TA. The maximum allowable power dissipation at any ambient temperature is PDMAX = (TJ(MAX) - TA)/ θJA. All numbers apply for packages soldered directly onto a PC board. The package thermal impedance is calculated in accordance with JESD 51-7.
(3) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

ELECTRICAL CHARACTERISTICS[1] (continued)

Unless otherwise specified, all limits ensured for TA = TJ = 25°C, VDD = 5.0V, VIO = 3.3V[2]

SYMBOL	PARAMETER	CONDITIONS/ COMMENTS	MIN[3]	TYP[4]	MAX[3]	UNITS
DIGITAL I/O CHARACTERISTICS						
V_{IH}	Logic "1" Input Voltage		$0.8 \times V_{IO}$			V
V_{IL}	Logic "0" Input Voltage				$0.2 \times V_{IO}$	V
V_{OH}	Logic "1" Output Voltage	ISOURCE=400uA		V_{IO}-0.3		V
V_{OL}	Logic "0" Output Voltage	ISINK=400uA			0.3	V
I_{IOHL}	Digital IO Leakage Current		-500		500	nA

TIMING DIAGRAMS

Unless otherwise noted, all limits specified at TA = 25°C, VDD=5.0, VIO=3.3, 10pF capacitive load in parallel with a 10kΩ load on SDO. Specified by design; not production tested.

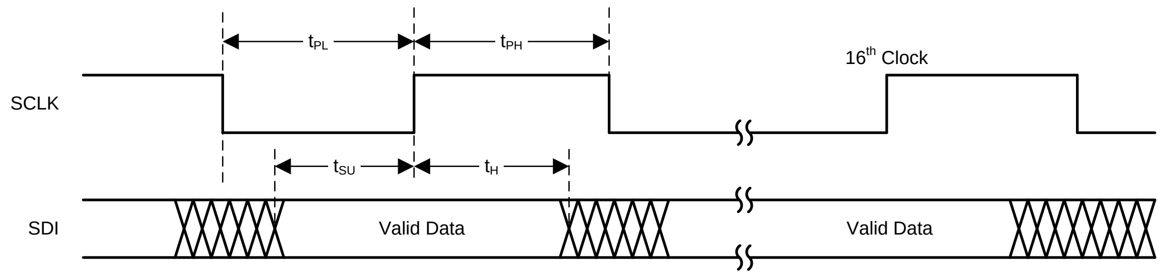

Figure 5. Write Timing Diagram

Table 2.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
F_{SCLK}	Serial Clock Frequency				4	MHz
t_{PH}	SCLK Pulse Width High	F_{SCLK}=4Mhz	0.4/Fsclk			s
t_{PL}	SCLK Pulse Width Low	F_{SCLK}=4Mhz	0.4/Fsclk			s
t_{SU}	SDI Setup Time		10			ns
t_H	SDI Hold Time		10			ns

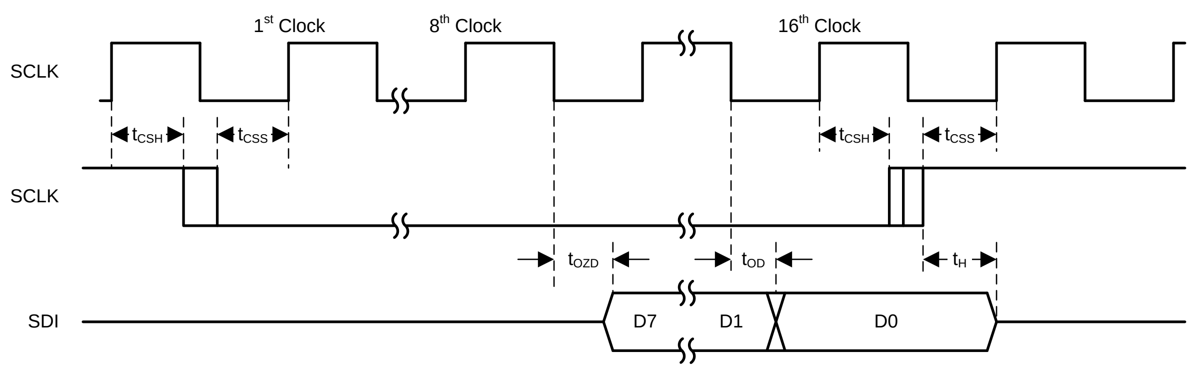

Figure 6. Read Timing Diagram

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_{ODZ}	SDO Driven-to-Tristate Time	Measured at 10% / 90% point			20	ns
t_{OZD}	SDO Tristate-to-Driven Time	Measured at 10% / 90% point			20	ns
t_{OD}	SDO Output Delay Time				20	ns
t_{CSS}	CSB Setup Time		20			ns
t_{CSH}	CSB Hold Time		20			ns
t_{IAG}	Inter-Access Gap		100			ns
t_{DRDYB}	Data ready pulse width	Data ready pulse at every 1/ODR if no data is read		$1/f_{sensor}$		s

THEORY OF OPERATION

Inductive Sensing

An AC current flowing through a coil will generate an AC magnetic field. If a conductive material, such as a metal target, is brought into the vicinity of the coil, this magnetic field will induce circulating currents (eddy currents) on the surface of the target. These eddy currents are a function of the distance, size, and composition of the target. These eddy currents then generate their own magnetic field, which opposes the original field generated by the coil. This mechanism is best compared to a transformer, where the coil is the primary core and the eddy current is the secondary core. The inductive coupling between both cores depends on distance and shape. Hence the resistance and inductance of the secondary core (Eddy current), shows up as a distant dependent resistive and inductive component on the primary side (coil). The figures below show a simplified circuit model.

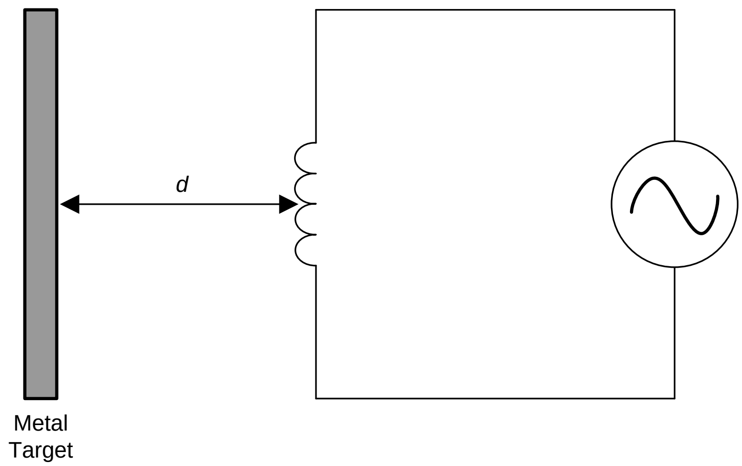

Figure 7. Inductor with a Metal Target

Eddy currents generated on the surface of the target can be modeled as a transformer as shown in Figure 8. The coupling between the primary and secondary coils is a function of the distance and conductor's characteristics. In Figure 8, the inductance Ls is the coil's inductance, and Rs is the coil's parasitic series resistance. The inductance L(d), which is a function of distance d, is the coupled inductance of the metal target. Likewise, R(d) is the parasitic resistance of the eddy currents.

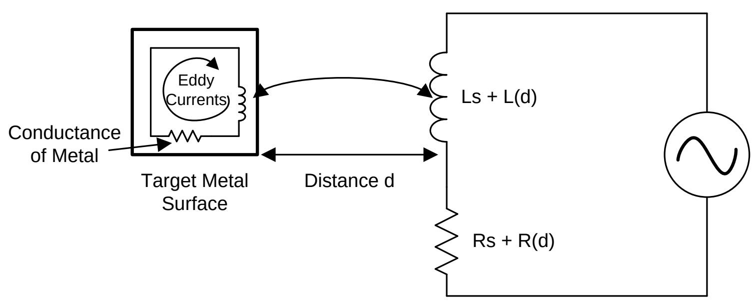

Figure 8. Metal Target Modeled as L and R with Circulating Eddy Currents

Generating an alternating magnetic field with just an inductor will consume a large amount of power. This power consumption can be reduced by adding a parallel capacitor, turning it into a resonator as shown in Figure 9 . In this manner the power consumption is reduced to the eddy and inductor losses Rs+R(d) only.

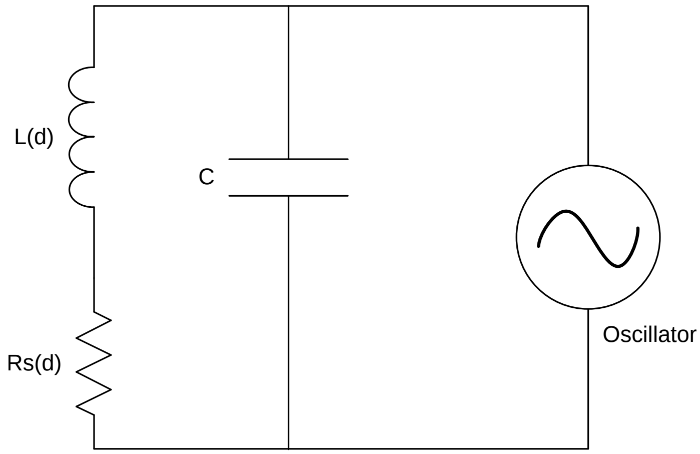

Figure 9. LC Tank Connected to Oscillator

The LDC1000 doesn't measure the series resistance directly; instead it measures the equivalent parallel resonance impedance Rp (see Figure 10). This representation is equivalent to the one shown in Figure 10 , where the parallel resonance impedance Rp(d) is given by: Rp(d)=(1⁄([Rs+R(d)])*([Ls+L(d)])⁄C.

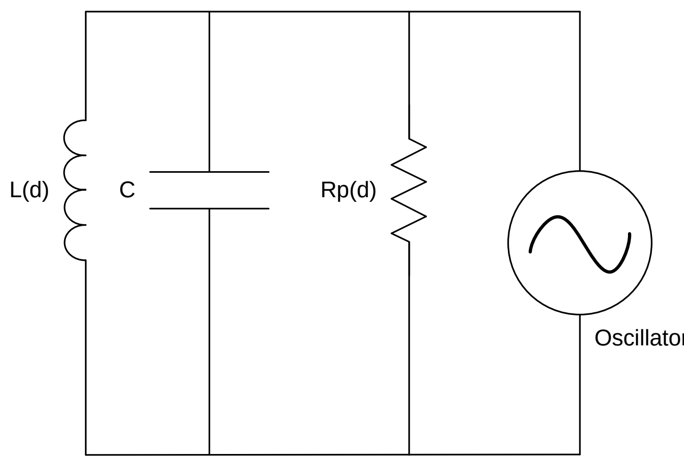

Figure 10. Equivalent Resistance of R_s in Parallel with LC Tank

Rp = (1/Rs)*(L/C).

Figure 11 below shows the variation in Rp as a function of distance for a 14mm diameter PCB coil(23 turns,4 mil trace width, 4mil spacing between trace,1oz Cu thickness,FR4). Target used is a Stainless steel 2mm thick.

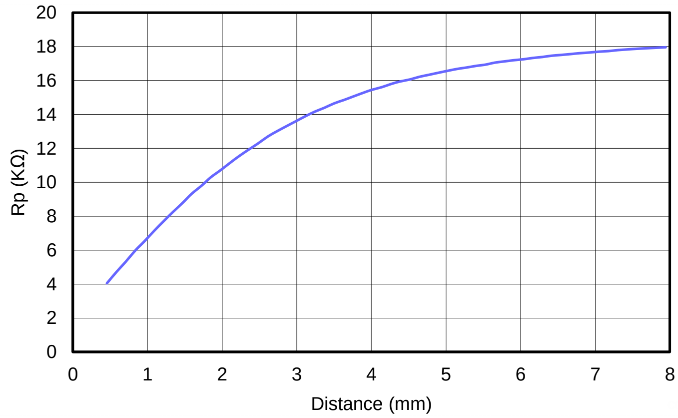

Figure 11. Typical Rp Vs Distance with 14mm PCB Coil

Measuring Parallel Resonance Impedance and Inductance with LDC1000

The LDC1000 is an Inductance-to-Digital Converter that simultaneously measures the impedance and resonant frequency of an LC resonator. It accomplishes this task by regulating the oscillation amplitude in a closed loop configuration to a constant level, while monitoring the energy dissipated by the resonator. By monitoring the amount of power injected into the resonator, the LDC1000 can determine the value of Rp; it returns this as a digital value which is inversely proportional to Rp. In addition, the LDC1000 can also measure the oscillation frequency of the LC circuit; this frequency is used to determine the inductance of the LC circuit. The oscillation frequency is returned as a digital value.

The LDC1000 supports a wide range of LC combinations, with oscillation frequencies ranging from 5kHz to 5MHz and Rp ranging from 798Ω to 3.93MΩ. This range of Rp can be viewed as the maximum input range of an ADC. As illustrated in Figure 11, the range of Rp is typically a much smaller than maximum input range supported by the LDC1000. To get better resolution in the desired sensing range, the LDC1000 offers programmable input range through the Rp_MIN and Rp_MAX registers. Refer to Calculation of Rp Min and Rp Max below for how to set these registers.

When the sensor's resonance impedance Rp drops below the programed Rp_MIN, the LDC's Rp output will clip at its full scale output. This situation could for example happen when a target comes too close to the coil.

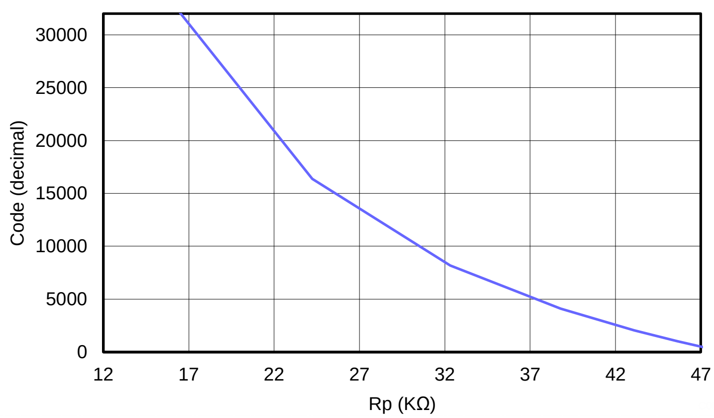

Figure 12. Transfer Characteristics of LDC1000 with Rp_MIN= 16.160 kΩ and Rp_MAX= 48.481 kΩ

The resonance impedance can be calculated from the digital output code as follows:

$R_P = (R_PMAX \times R_PMIN) / (R_PMIN \times (1-Y) + R_PMAX \times Y)$, in Ω.

Where:

- $Y = \text{Proximity Data}/2^{15}$
- Proximity data is the LDC output, register address 0x21 and 0x22. (1)

Example: If Proximity data (address 0x22:0x21) is 5000, Rp_MIN is 2.394 kΩ, and Rp_MAX is 38.785 kΩ ,the resonance impedance is given by:

$Y = 5000/2^{15} = 0.1526$

RP=(38785*2394)/(2394×(1-0.1526) + 38785×0.1526) =(92851290)/(2028.675 + 5918.591)

RP =11.683 kΩ

Figure 13 and Figure 14below show the change in RMS noise versus distance and a histogram of noise, with the target at 0.8mm distance from the sensor coil. Data was collected with a 14mm PCB coil(23 turns,4 mil trace width, 4mil spacing between trace,1oz Cu thickness,FR4) with a sensing range of 0.125mm to 1.125mm. At a distance of 0.8mm, the RMS noise is approximately 250nm.

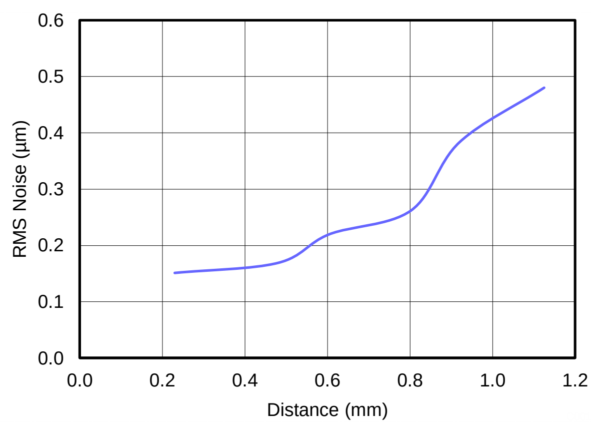

Figure 13. Typical RMS Noise Vs. Distance with PCB Coil

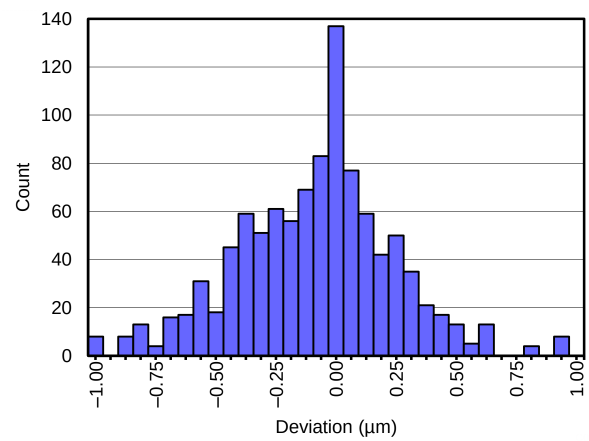

Figure 14. Histogram of Output Codes at 0.8mm Distance

Note that while the LDC1000 has high resolution, its absolute accuracy depends on offset and gain correction which can be achieved by two-point calibration.

Calculation of Rp Min and Rp Max

Different sensing applications may have a different ranges of the resonance impedance Rp to measure. The LDC1000 measurement range of Rp is controlled by setting 2 registers – Rp_MIN and Rp_MAX. For a given application, Rp must never be outside the range set by these register values, otherwise the measured value will be clipped. For optimal sensor resolution, the range of Rp_MIN to Rp_MAX should not be unnecessarily large. The following procedure is recommended to determine the Rp_MIN and Rp_MAX register values.

Rp_MAX

Rp_MAX sets the upper limit of the LDC1000 resonant impedance input range.

- Configure the sensor such that the eddy current losses are minimized. As an example, for a proximity sensing application, set the distance between the sensor and the target to the maximum sensing distance.
- Measure the resonant impedance Rp using an impedance analyzer.
- Multiply Rp by 2 and use the next higher value from Table 6.

For example, if Rp at 8mm is measured to be 18kΩ, 18000×2 = 36000. In Table 6, then 38.785kΩ is the smallest value larger than 36kΩ; this corresponds to Rp_MAX value of 0x11.

Note that setting Rp_MAX to a value not listed in Table 6 can result in indeterminate behavior.

Rp_MIN

Rp_MIN sets the lower limit of the LDC1000 resonant impedance input range.

- Configure the sensor such that the eddy current losses are maximized. As an example, for a proximity sensing application, set the distance between the sensor and the metal target to the minimum sensing distance.
- Measure the resonant impedance Rp using an impedance analyzer.
- Divide the Rp value by 2 and then select the next lower Rp value from Table 8.

For example, if Rp at 1mm is measured to be 5kΩ, 5000/2 = 2500. In Table 8 , 2.394kΩ is the smallest value lower than 2.5kΩ; this corresponds to Rp_MIN value of 0x3B.

Note that setting Rp_MIN to a value not listed on Table 8 can result in indeterminate behavior. In addition, Rp_MIN powers on with a default value of 0x14 which must be set to a value from Table 8 prior to powering on the LDC.

Measuring Inductance

LDC1000 measures the sensor's frequency of oscillation by a frequency counter. The frequency counter timing is set by an external clock or crystal. Either the external clock(8MHz typical) from microcontroller can be provided on the TBCLK pin or a crystal can be connected on the XTALIN and XTALOUT pins. The clock mode is controlled through Clock Configuration register (address 0x05). The sensor resonance frequency is derived from the frequency counter registers value (see registers 0x23 through 0x25) as follows:

Sensor frequency, f_{sensor} = (1/3)*(Fext/Fcount)*(Response Time)

where Fext is the frequency of the external clock or crystal, Fcount is the value obtained from the Frequency Counter Data register(address 0x23,0x24,0x25), and Response Time is the programmed response time (see LDC configuration register, address 0x04).

The Inductance can be calculated as follows:

$$L=1/[C*(2*\pi*f_{sensor})^2], \quad (2)$$

where C is the parallel capacitance of the resonator.

Example: If Fext=6Mhz, Response time=6144, C=100pF and measured Fcount= 3000 (dec) (address 0x23 through 0x25)

f_{sensor}=(1/3)*(6000000/3000)*(6144)= 4.096Mhz

Now using, $L=1/[C*(2*\pi*f_{sensor})^2]$

Inductance, L = 15.098uH

The accuracy of measurement largely depends upon the choice of the external time-base clock (TBCLK) or the crystal oscillator (XIN/XOUT).

Output Data Rate

Output data rate of LDC1000 depends on the sensor frequency, f_{sensor} and 'Response Time' field in LDC Configuration register(Address:0x04).

Output data rate=(f_{sensor})/(Response Time/3), Sample per second(SPS)

Example: If f_{sensor}=5Mhz and Response Time=192

Output data rate= (5M)/(192/3)= 78.125 KSPS

Choosing Filter Capacitor (CFA and CFB Pins)

The Filter capacitor is critical to the operation of the LDC1000. The capacitor should be low leakage, temperature stable, and it must not generate any piezoelectric noise (the dielectrics of many capacitors exhibit piezoelectric characteristics and any such noise is coupled directly through Rp into the converter). The optimal capacitance values range from 20pF to 100nF. The value of the capacitor is based on the time constant and resonating frequency of the LC tank.

If a ceramic capacitor is used, then a C0G (or NP0) grade dielectric is recommended; the voltage rating should be ≥10V. The traces connecting CFA and CFB to the capacitor should be as short as possible to minimize any parasitics.

For optimal performance, the chosen filter capacitor, connected between pins CFA and CFB, needs to be as small as possible, but large enough such that the active filter does not saturate. The size of this capacitor depends on the time constant of the sense coil, which is given by L/Rs, (L=inductance, Rs=series resistance of the inductor at oscillation frequency). The larger this time constant, the larger filter capacitor is required. Hence, this time constant reaches its maximum when there is no target present in front of the sensing coil.

The following procedure can be used to find the optimal filter capacitance:

1. Start with a large filter capacitor. For a ferrite core coil, 10nF is usually large enough. For an air coil or PCB coil, 100pF is usually large enough.
2. Power on the LDC and set the desired register values. Minimize the eddy currents losses by ensuring there is maximum clearance between the target and the sensing coil.
3. Observe the signal on the CFB pin using a scope. Since this node is very sensitive to capacitive loading, it is recommended to use an active probe. As an alternative, a passive probe with a 1kΩ series resistance between the tip and the CFB pin can be used.
4. Vary the values of the filter capacitor until that the signal observed on the CFB pin has an amplitude of approximate 1V peak-to-peak. This signal scales linearly with the reciprocal of the filter capacitance. For example, if a 100pF filter capacitor is applied and the signal observed on the CFB pin has a peak-to-peak value of 200mV, the desired 1V peak-to-peak value is obtained using a 200mV / 1V * 100pF = 20pF filter capacitor.

The waveforms below were taken on the CFB pin with a 14mm, 2 layer PCB coil(23 turns,4 mil trace width, 4mil spacing between trace,1oz Cu thickness,FR4):

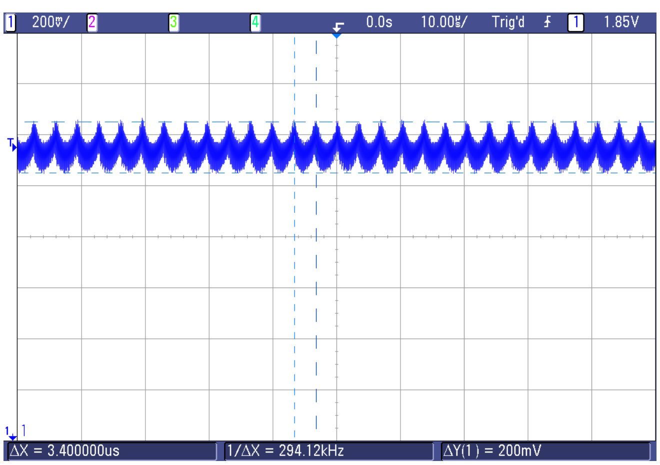

Figure 15. Waveform on CFB with 100pF

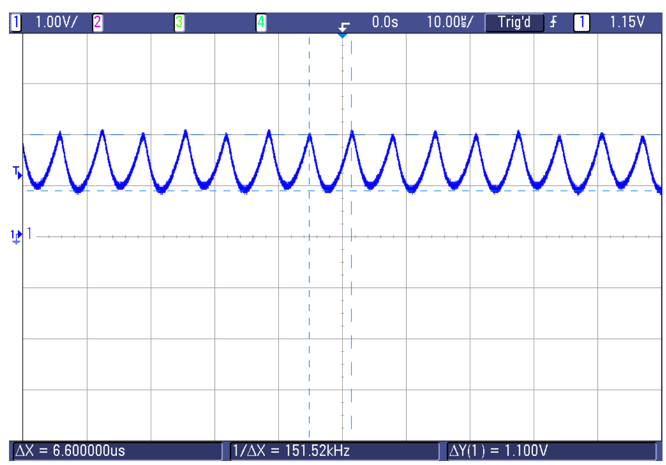

Figure 16. Waveform on CFB with 20pF

PROGRAMMABLE REGISTERS

Table 3. Register Map[(1)(2)(3)]

<table>
<tr><th>Register Name</th><th>Address</th><th>Direction</th><th>Default</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td>Device ID</td><td>0x00</td><td>RO</td><td>0x80</td><td colspan="8">Device ID</td></tr>
<tr><td>Rp_MAX</td><td>0x01</td><td>R/W</td><td>0x0E</td><td colspan="8">Rp Maximum</td></tr>
<tr><td>Rp_MIN</td><td>0x02</td><td>R/W</td><td>0x14</td><td colspan="8">Rp Minimum</td></tr>
<tr><td>Sensor Frequency</td><td>0x03</td><td>R/W</td><td>0x45</td><td colspan="8">Min Resonating Frequency</td></tr>
<tr><td>LDC Configuration</td><td>0x04</td><td>R/W</td><td>0x1B</td><td colspan="3">Reserved(000)</td><td colspan="2">Amplitude</td><td colspan="3">Response Time</td></tr>
<tr><td>Clock Configuration</td><td>0x05</td><td>R/W</td><td>0x01</td><td colspan="6">Reserved(000000)</td><td>CLK_SEL</td><td>CLK_PD</td></tr>
<tr><td>Comparator Threshold High LSB</td><td>0x06</td><td>R/W</td><td>0xFF</td><td colspan="8">Threshold High LSB</td></tr>
<tr><td>Comparator Threshold High MSB</td><td>0x07</td><td>R/W</td><td>0xFF</td><td colspan="8">Threshold High MSB</td></tr>
<tr><td>Comparator Threshold Low LSB</td><td>0x08</td><td>R/W</td><td>0x00</td><td colspan="8">Threshold Low LSB</td></tr>
<tr><td>Comparator Threshold Low MSB</td><td>0x09</td><td>R/W</td><td>0x00</td><td colspan="8">Threshold Low MSB</td></tr>
<tr><td>INTB Pin Configuration</td><td>0x0A</td><td>R/W</td><td>0x00</td><td colspan="5">Reserved(00000)</td><td colspan="3">INTB_MODE</td></tr>
<tr><td>Power Configuration</td><td>0x0B</td><td>R/W</td><td>0x00</td><td colspan="7">Reserved(0000000)</td><td>PWR_MODE</td></tr>
<tr><td>Status</td><td>0x20</td><td>RO</td><td></td><td>OSC Dead</td><td>DRDYB</td><td>Wake-up</td><td>Comparator</td><td colspan="4">Do not Care</td></tr>
<tr><td>Proximity Data LSB</td><td>0x21</td><td>RO</td><td></td><td colspan="8">Proximity Data[7:0]</td></tr>
<tr><td>Proximity Data MSB</td><td>0x22</td><td>RO</td><td></td><td colspan="8">Proximity Data[15:8]</td></tr>
<tr><td>Frequency Counter Data LSB</td><td>0x23</td><td>RO</td><td></td><td colspan="8">ODR LSB</td></tr>
<tr><td>Frequency Counter Data Mid-Byte</td><td>0x24</td><td>RO</td><td></td><td colspan="8">ODR Mid Byte</td></tr>
<tr><td>Frequency Counter Data MSB</td><td>0x25</td><td>RO</td><td></td><td colspan="8">ODR MSB</td></tr>
</table>

(1) Values of Bits which are unused should be set to default values only.
(2) Registers 0x01 through 0x05 are Read Only when the part is awake (PWR_MODE bit is SET)
(3) R/W: Read/Write. RO: Read Only. WO: Write Only.

Register Description

Table 4. Revision ID

Address = 0x00, Default=0x80, Direction=RO		
Bit Field	**Field Name**	**Description**
7:0	Revision ID	Revision ID of Silicon.

Table 5. Rp_MAX

Address = 0x01, Default=0x0E, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:0	Rp Maximum	Maximum Rp that LDC1000 needs to measure. Configures the input dynamic range of LDC1000. See Table 6 for register settings.

Table 6. Register settings for Rp_MAX

Register setting	Rp (kΩ)
0x00	3926.991
0x01	3141.593
0x02	2243.995
0x03	1745.329
0x04	1308.997
0x05	981.748
0x06	747.998
0x07	581.776
0x08	436.332
0x09	349.066
0x0A	249.333
0x0B	193.926
0x0C	145.444
0x0D	109.083
0x0E	83.111
0x0F	64.642
0x10	48.481
0x11	38.785
0x12	27.704
0x13	21.547
0x14	16.160
0x15	12.120
0x16	9.235
0x17	7.182
0x18	5.387
0x19	4.309
0x1A	3.078
0x1B	2.394
0x1C	1.796
0x1D	1.347
0x1E	1.026
0x1F	0.798

Table 7. Rp_MIN

Address = 0x02, Default=0x14, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:0	Rp Minimum	Minimum Rp that LDC1000 needs to measure. Configures the input dynamic range of LDC1000. See Table 8 for register settings.(1)

(1) This Register needs a mandatory write as it defaults to 0x14.

Table 8. Register Settings for Rp_MIN

Register setting	Rp (kΩ)
0x20	3926.991
0x21	3141.593
0x22	2243.995
0x23	1745.329
0x24	1308.997
0x25	981.748
0x26	747.998
0x27	581.776
0x28	436.332
0x29	349.066
0x2A	249.333
0x2B	193.926
0x2C	145.444
0x2D	109.083
0x2E	83.111
0x2F	64.642
0x30	48.481
0x31	38.785
0x32	27.704
0x33	21.547
0x34	16.160
0x35	12.120
0x36	9.235
0x37	7.182
0x38	5.387
0x39	4.309
0x3A	3.078
0x3B	2.394
0x3C	1.796
0x3D	1.347
0x3E	1.026
0x3F	0.798

Table 9. Sensor Frequency(1)(2)

Address = 0x03, Default=0x45, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:0	Min Resonating Frequency	Sets the minimum resonating frequency to approximately 20% below the lowest resonating frequency of the sensor with no target in front. Use the formula below to determine the value of register.

(1) **N** = 68.94 * $\log_{10}$(F/2000)
F = 20% below resonating frequency, Hz
N = Register Value. Round to nearest value.

(2) **Example:**
Sensor Frequency: 1MHz
F = 0.8*1Mhz=800Khz
N = 68.94 * $\log_{10}$(800KHz/2000)= Round to nearest(179.38)=179 (Value to be programmed in Sensor Frequency register)

Table 10. LDC Configuration

Address = 0x04, Default=0x1B, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:5	Reserved	Reserved to 0
4:3	Amplitude	Sets the oscillation amplitude 00:1V 01:2V 10:4V **11:Reserved**
2:0	Response Time	000: Reserved 001: Reserved 010: 192 **011: 384** 100: 768 101: 1536 110: 3072 111: 6144

Table 11. Clock Configuration

Address = 0x05, Default=0x01, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:2	Reserved	Reserved to 0
1	CLK_SEL	1:External Crystal used for Frequency Counter (XIN/XOUT). **0:External Time-Base Clock used for Frequency Counter (TBCLK).**
0	CLK_PD	**1:Disable External time base clock. Crystal Oscillator Power Down.** 0:Enable External time base clock.

Table 12. Comparator Threshold High LSB

Address = 0x06, Default=0xFF, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:0	Threshold High LSB Threshold High[7:0]	Least Significant byte of Threshold High Register. This register is a buffer. Read will reflect the current value of Threshold High [7:0] .See register 0x07 for details on Updating the Threshold High register.

Table 13. Comparator Threshold High MSB

Address = 0x07, Default=0xFF, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:0	Threshold High MSB Threshold High[15:8]	Most Significant byte of Threshold High Register. Write to this register copies the contents of 0x06 register and Writes to Threshold High register[15:0]. Read will return Threshold high [15:8]. To Update Threshold high register write register 0x06 first and then 0x07.

Table 14. Comparator Threshold Low LSB

Address = 0x08, Default=0x00, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:0	Threshold Low LSB Threshold Low[7:0]	Least Significant byte of Threshold Low Value. This register is a buffer. Read will reflect the current value of Threshold Low [7:0]. See register 0x09 for details on Updating the Threshold Low register.

Table 15. Comparator Threshold Low MSB

Address = 0x09, Default=0x00, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:0	Threshold Low MSB Threshold Low[15:8]	Most Significant byte of Threshold Low Register. Write to this register copies the contents of 0x08 register and Writes to Threshold Low register[15:0]. Read will return Threshold Low [15:8]. To Update Threshold low register write register addr 0x08 first and then 0x09.

Table 16. INTB Pin Configuration

Address = 0x0A, Default=0x00, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:3	Reserved	Reserved to 0
2:0	Mode	100: DRDYB Enabled on INTB pin
		010: INTB pin indicates the status of Comparator output
		001: Wake-up Enabled on INTB pin
		000: All modes disabled
		All other combinations are Reserved

Table 17. Power Configuration

Address = 0x0B, Default=0x00, Direction=R/W		
Bit Field	**Field Name**	**Description**
7:1	Reserved	Reserved to 0
0	PWR_MODE	**0:Stand-By mode** 1:Active Mode. Conversion is Enabled

Table 18. Status

Address = 0x20, Default=NA, Direction=RO		
Bit Field	**Field Name**	**Description**
7	OSC status	1:Indicates oscillator overloaded and stopped
		0:Oscillator working
6	Data Ready	0:Data is ready to be read
		1:No new data available
5	Wake-up	0:Wake-up triggered. Proximity data is more than Threshold High value.
		1:Wake-up disabled
4	Comparator	0:Proximity data is more than Threshold High value
		1:Proximity data is less than Threshold Low value
3:0	Do not Care	

Table 19. Proximity Data LSB

Address = 0x21, Default=NA, Direction=RO		
Bit Field	**Field Name**	**Description**
7:0	Proximity Data[7:0]	Least Significant Byte of Proximity Data

Table 20. Proximity Data MSB

Address = 0x22, Default=NA, Direction=RO		
Bit Field	**Field Name**	**Description**
7:0	Proximity data [15:8]	Most Significant Byte of Proximity data

Table 21. Frequency Counter LSB

Address = 0x23, Default=NA, Direction=RO		
Bit Field	**Field Name**	**Description**
7:0	ODR LSB (ODR[7:0])	LSB of Output data rate. Sensor frequency can be calculated using the output data rate. Please refer to the Measuring Inductance.

Table 22. Frequency Counter Mid-Byte

Address = 0x24, Default=NA, Direction=RO		
Bit Field	**Field Name**	**Description**
7:0	ODR Mid byte (ODR[15:8])	Middle Byte of Output data rate

Table 23. Frequency Counter MSB

Address = 0x25, Default=NA, Direction=RO		
Bit Field	**Field Name**	**Description**
7:0	ODR MSB (ODR[23:16])	MSB of Output data rate

Care must be taken to ensure that Proximity Data[15:0] and Frequency Counter[23:0] are all from same conversion. Conversion data is updated to these registers only when a read is initiated on 0x21 register. If the read is delayed between subsequent conversions, these registers are not updated until another read is initiated on 0x21.

DIGITAL INTERFACE

The LDC1000 utilizes a 4-wire SPI interface to access control and data registers. The LDC1000 is an SPI slave device and does not initiate any transactions.

SPI Description

A typical serial interface transaction begins with an 8-bit instruction, which is comprised of a read/write bit (MSB, R=1) and a 7 bit address of the register, followed by a Data field which is typically 8 bits. However, the data field can be extended to a multiple of 8 bits by providing sufficient SPI clocks. Refer to the Extended SPI Transactions section below.

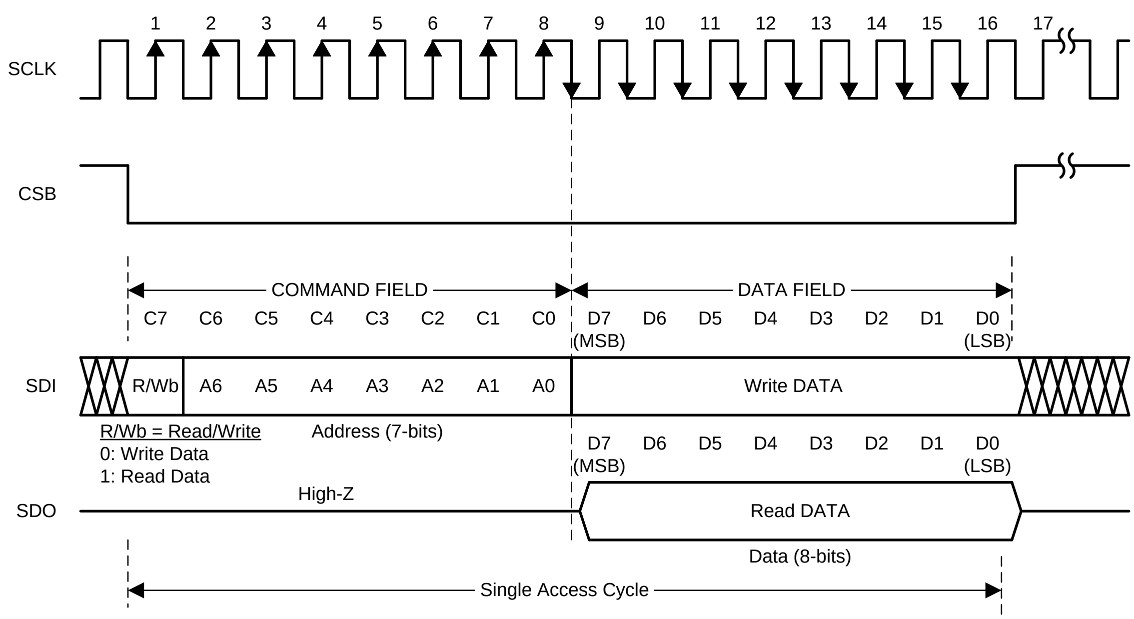

Figure 17. Serial Interface Protocol

Each assertion of chip select bar (CSB) starts a new register access. The R/Wb bit in the command field configures the direction of the access; a value of 0 indicates a write operation and a value of 1 indicates a read operation. All output data is driven on the falling edge of the serial clock (SCLK), and all input data is sampled on the rising edge of the serial clock (SCLK). Data is written into the register on the rising edge of the 16th clock. It is required to deassert CSB after the 16th clock; if CSB is deasserted before the 16th clock, no data write will occur.

Extended SPI Transactions

A transaction may be extended to multiple registers by keeping the CSB asserted beyond the stated 16 clocks. In this mode, the register addresses increment automatically. CSB must be asserted during 8*(1+N) clock cycles of SCLK, where N is the amount of bytes to write or read during the transaction.

During an extended read access, SDO outputs the register contents every 8 clock cycles after the initial 8 clocks of the command field. During an extended write access, the data is written to the registers every 8 clock cycles after the initial 8 clocks of the command field.

Extended transactions can be used to read 16-bits of Proximity data and 24-bits of frequency data all in one SPI transaction by initiating a read from register 0x21.

INTB Pin Modes

The INTB pin is a configurable output pin which can be used to drive an interrupt on an MCU. The LDC1000 provides three different modes on INTB Pin:

1. Comparator Mode
2. Wake-Up Mode
3. DRDY Mode

LDC1000 has a build-in High and Low trigger threshold registers which can be as a comparator with programmable hysteresis or a special mode which can be used to wake-up an MCU. These modes are explained in detail below.

Comparator Mode

In the Comparator mode, the INTB pin is asserted or de-asserted when the proximity register value increases above Threshold High or decreases below Threshold Low registers respectively. In this mode, the LDC1000 essentially behaves as a proximity switch with programmable hysteresis.

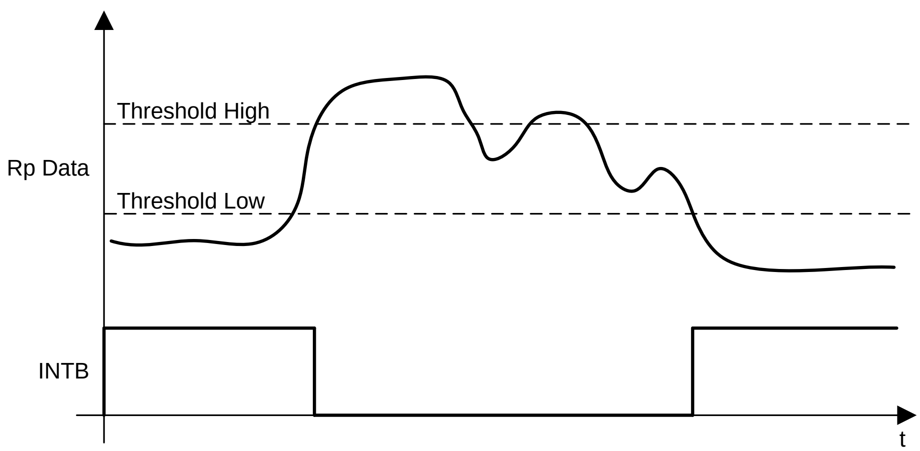

Figure 18. Behavior of INTB Pin in Comparator Mode

Wake-Up Mode

In Wake-Up mode, the INTB pin is asserted when proximity register value increases above Threshold High and de-asserted when wake-up mode is disabled in INTB pin mode register.

This Mode can be used to wake-up an MCU which is asleep, to conserve power.

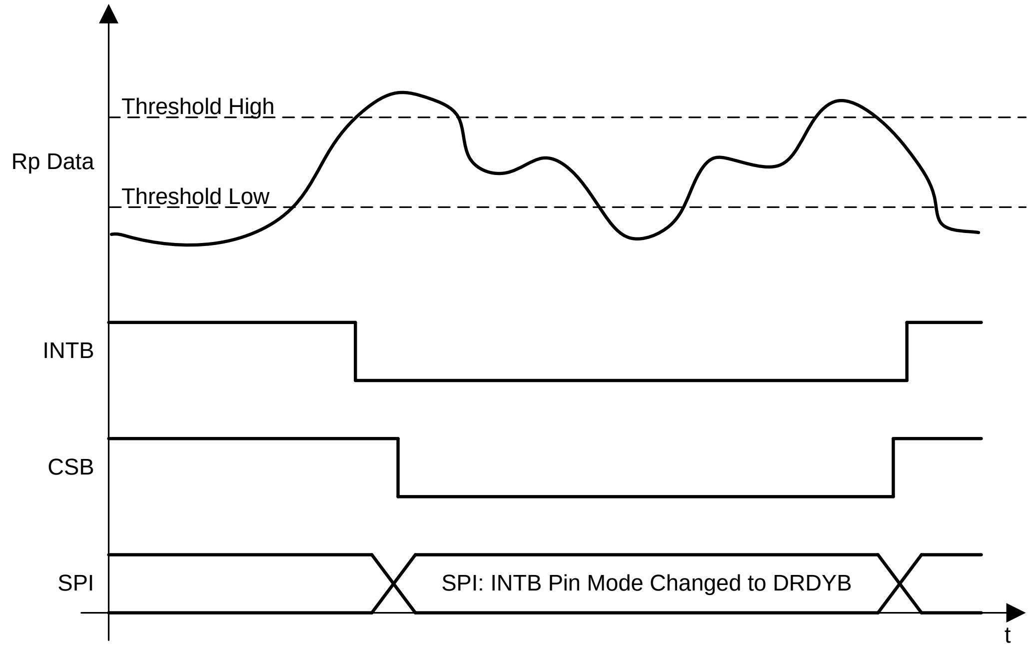

Figure 19. Behavior of INTB Pin in Wake-Up Mode

DRDYB Mode

In DRDY mode (default), the INTB pin is asserted every time the conversion data is available and de-asserted once the read command on register 0x21 is registered internally; if the read is in progress, the pin is pulsed instead.

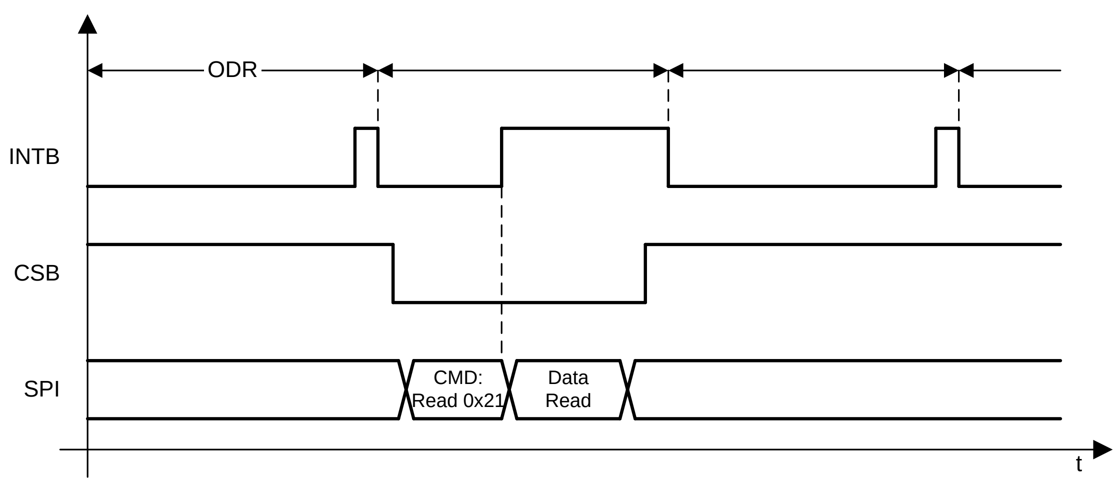

Figure 20. Behavior of INTB Pin in DRDYB Mode

TYPICAL APPLICATIONS

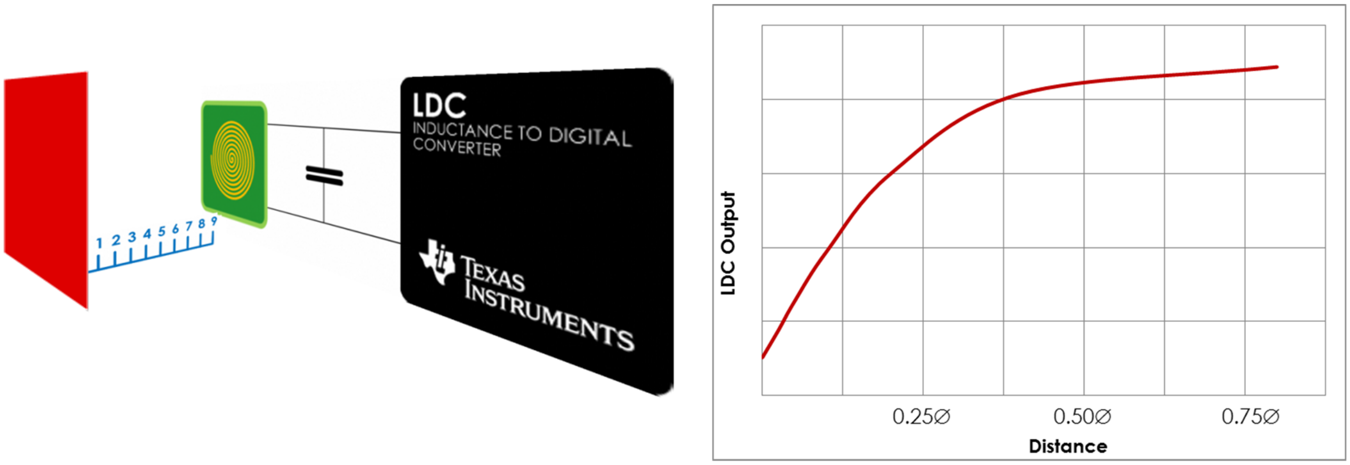

Figure 21. Axial Distance Measurement

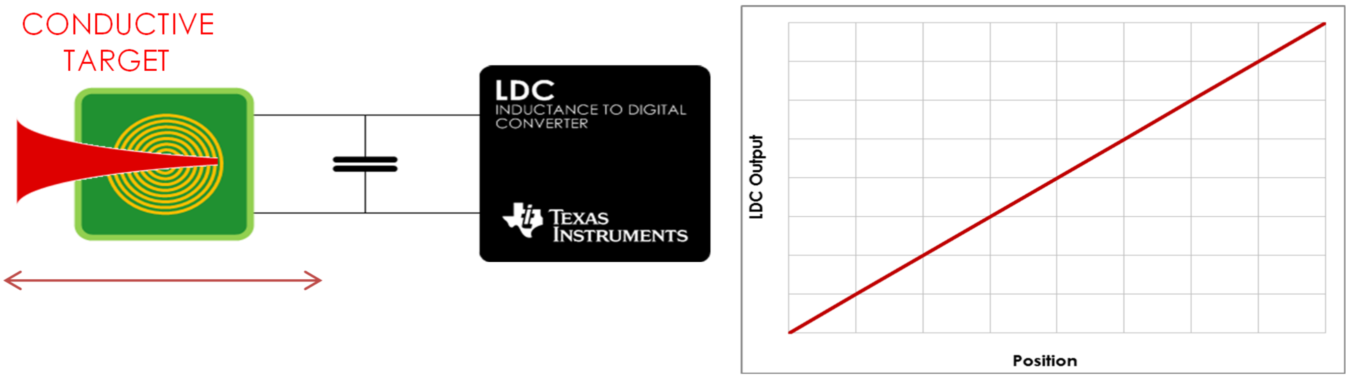

Figure 22. Linear Position Sensing

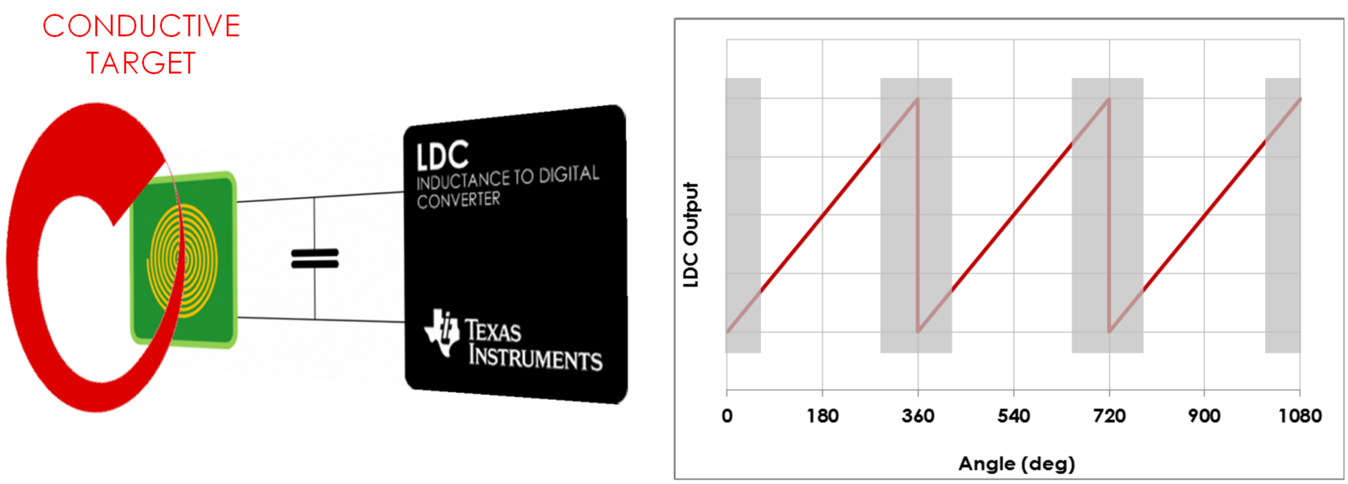

Figure 23. Angular Position Sensing

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LDC1000NHRJ	ACTIVE	WSON	NHR	16	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LDC1000	Samples
LDC1000NHRR	ACTIVE	WSON	NHR	16	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LDC1000	Samples
LDC1000NHRT	ACTIVE	WSON	NHR	16	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LDC1000	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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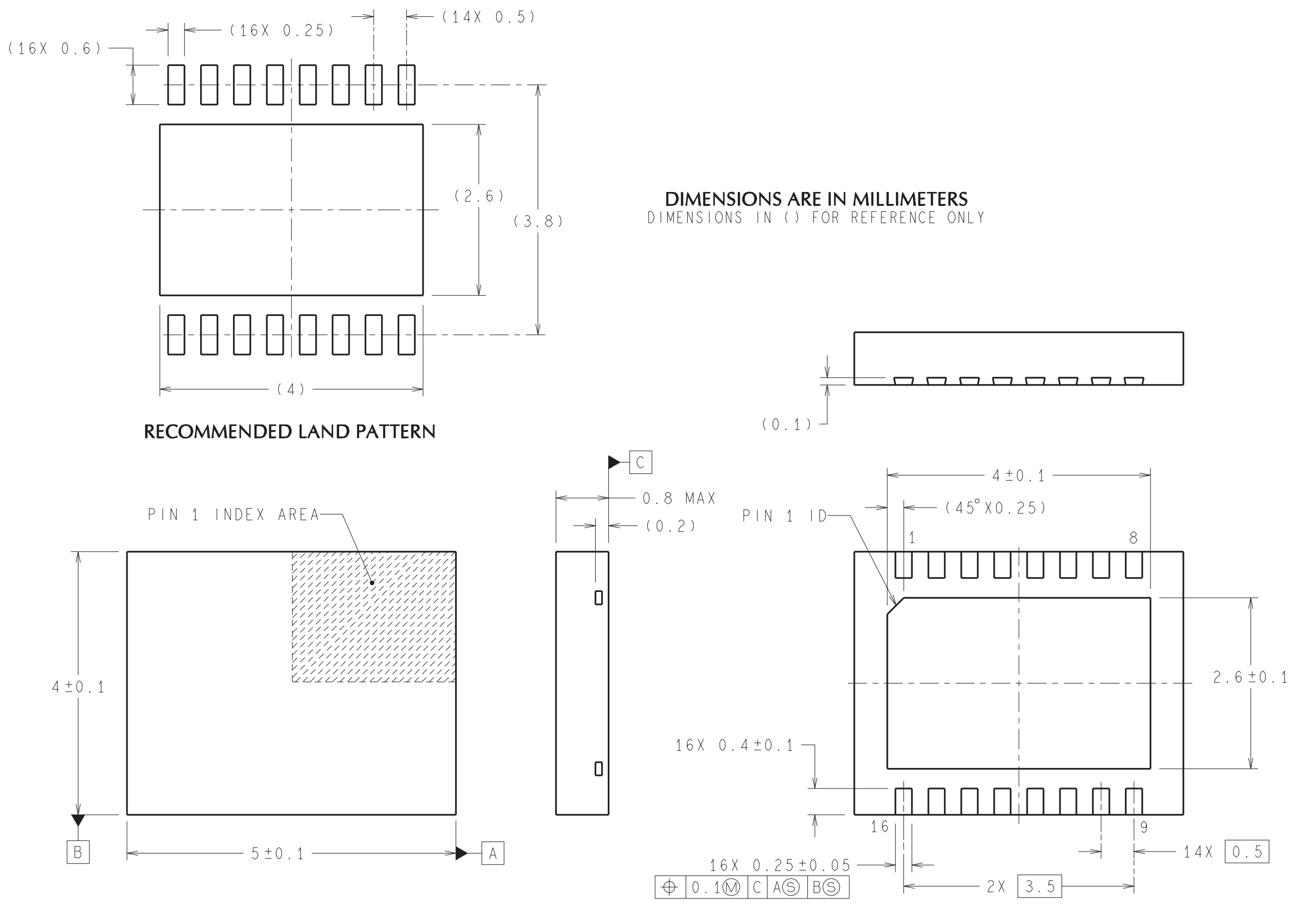

SDA16B (Rev A)

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