Features

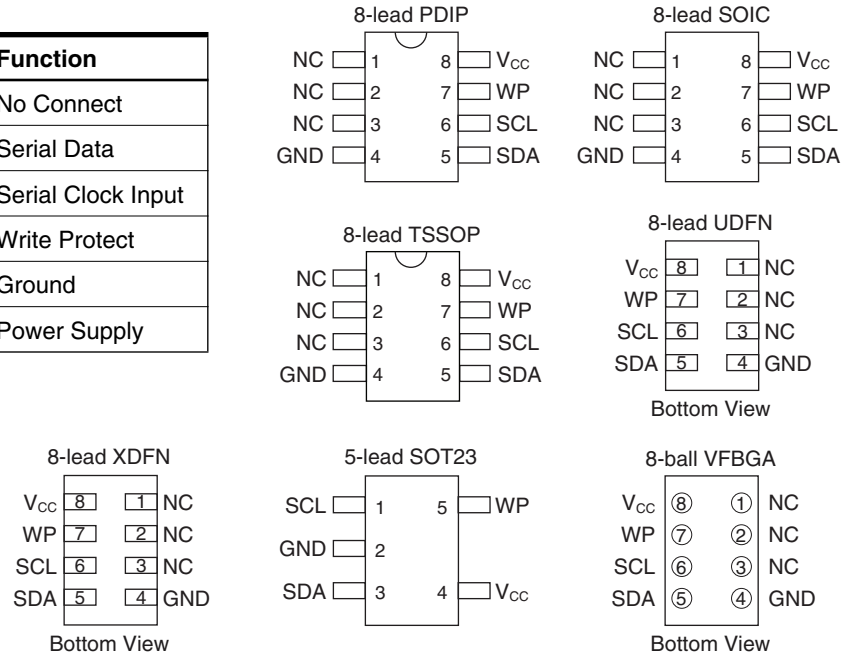
- **Low-voltage and Standard-voltage Operation**
  - **V_{CC} = 1.7V to 5.5V**
- **Internally Organized 2048 x 8 (16K)**
- **Two-wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bidirectional Data Transfer Protocol**
- **1MHz (5V, 2.5V), 400kHz (1.7V) Compatibility**
- **Write Protect Pin for Hardware Data Protection**
- **16-byte Page Write Modes**
- **Partial Page Writes Allowed**
- **Self-timed Write Cycle (5ms max)**
- **High-reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
- **8-lead PDIP, 8-lead JEDEC SOIC, 8-lead TSSOP, 8-lead UDFN, 8-lead XDFN, 5-lead SOT23 and 8-ball VFBGA Packages**
- **Lead-free/Halogen-free**
- **Die Sales: Wafer Form, Tape and Reel, and Bumped Wafers**

Description

The Atmel® AT24C16C provides 16,384-bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 2,048 words of 8-bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT24C16C is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead TSSOP, 8-lead UDFN, 8-lead XDFN, 5-lead SOT23, and 8-ball VFBGA Packages and is accessed via a Two-wire serial interface. In addition, the AT24C16C operates from 1.7V to 5.5V.

Figure 0-1. Pin Configurations

Pin Name	Function
NC	No Connect
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
GND	Ground
VCC	Power Supply



Two-wire Serial Electrically Erasable and Programmable Read-only Memory

16K (2048 x 8)

Atmel AT24C16C

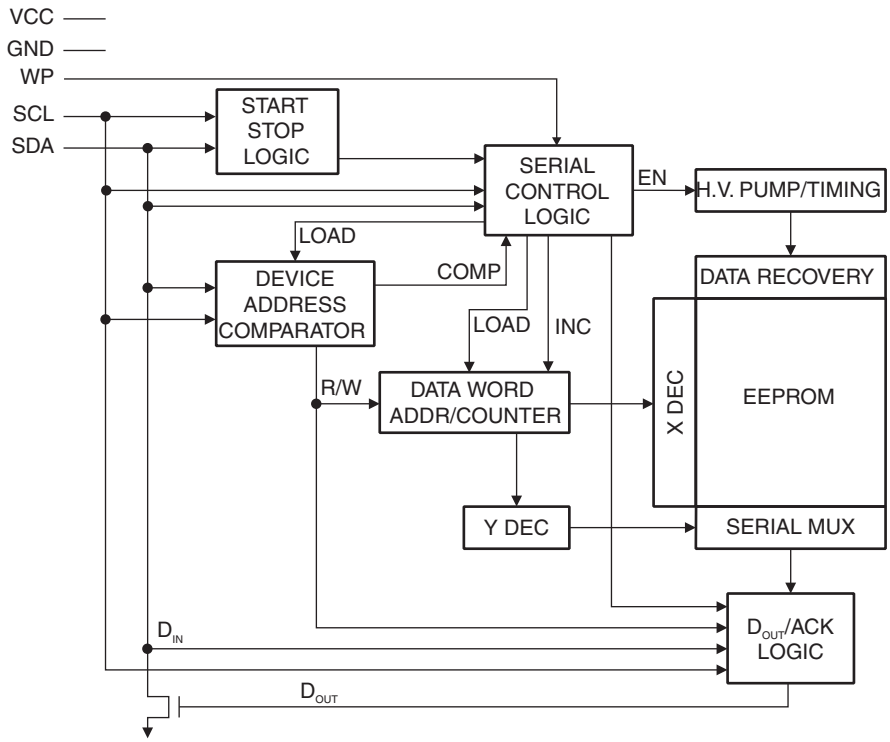
8719A–SEEPR–9/10

Absolute Maximum Ratings

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 0-2. Block Diagram



1. Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES: The Atmel® AT24C16C does not use the device address pins, which limits the number of devices on a single bus to one.

WRITE PROTECT (WP): The AT24C16C has a write protect pin that provides hardware data protection. The write protect pin allows normal read/write operations when connected to ground (GND). When the write protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in <blue>Table 1-1.

Table 1-1. Write Protect

WP Pin Status	Part of the Array Protected
	24C16C
At V_{CC}	Full (16K) Array
At GND	Normal Read/Write Operations

2. Memory Organization

Atmel AT24C16C, 16K SERIAL EEPROM: Internally organized with 128 pages of 16-bytes each, the 16K requires an 11-bit data word address for random word addressing.

Table 2-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25·C, f = 1.0MHz, V_{CC} = +1.7V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested

Table 2-2. DC Characteristics

Applicable over recommended operating range from: T_{AI} = –40·C to +85·C, V_{CC} = +1.7V to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.7		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V	READ at 400kHz		1.0	2.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V	WRITE at 400kHz		2.0	3.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.7V	V_{IN} = V_{CC} or V_{SS}			1.0	µA
		V_{CC} = 5.5V				6.0	
I_{LI}	Input Leakage Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}			0.10	3.0	µA
I_{LO}	Output Leakage Current V_{CC} = 5.0V	V_{OUT} = V_{CC} or V_{SS}			0.05	3.0	µA
V_{IL}	Input Low Level[1]			–0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low Level	V_{CC} = 1.7V	I_{OL} = 0.15mA			0.2	V
V_{OL2}	Output Low Level	V_{CC} = 3.0V	I_{OL} = 2.1mA			0.4	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested

Table 2-3. AC Characteristics (Industrial Temperature)

Applicable over recommended operating range from T_{AI} = –40·C to +85·C, V_{CC} = +1.7V to +5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	1.7V		2.5V, 5.0V		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3		0.4		µs
t_{HIGH}	Clock Pulse Width High	0.6		0.4		µs
t_I	Noise Suppression Time(1)		50		50	ns
t_{AA}	Clock Low to Data Out Valid	0.05	0.9	0.05	0.55	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	1.3		0.5		µs
$t_{HD.STA}$	Start Hold Time	0.6		0.25		µs
$t_{SU.STA}$	Start Set-up Time	0.6		0.25		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	100		100		ns
t_R	Inputs Rise Time(1)		0.3		0.3	µs
t_F	Inputs Fall Time(1)		300		100	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		0.25		µs
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance(1)	25°C, Page Mode, 3.3V	1,000,000				Write Cycles

Notes: 1. This parameter is characterized and is not 100% tested

2. AC measurement conditions:
   R_L (connects to V_{CC}): 1.3 kΩ (2.5V, 5.0V), 10 kΩ (1.7V)
   Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}
   Input rise and fall times: ≤ 50ns
   Input and output timing reference voltages: 0.5 V_{CC}

3. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see <blue>Figure 3-4 on page 7). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see <blue>Figure 3-5 on page 8).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see <blue>Figure 3-5 on page 8).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The Atmel® AT24C16C features a low-power standby mode which is enabled:
(a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

2-WIRE SOFTWARE RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be protocol reset by following these steps:

1. Create a start bit condition
2. Clock nine cycles
3. Create another start bit followed by stop bit condition as shown below

Figure 3-1. Software Reset

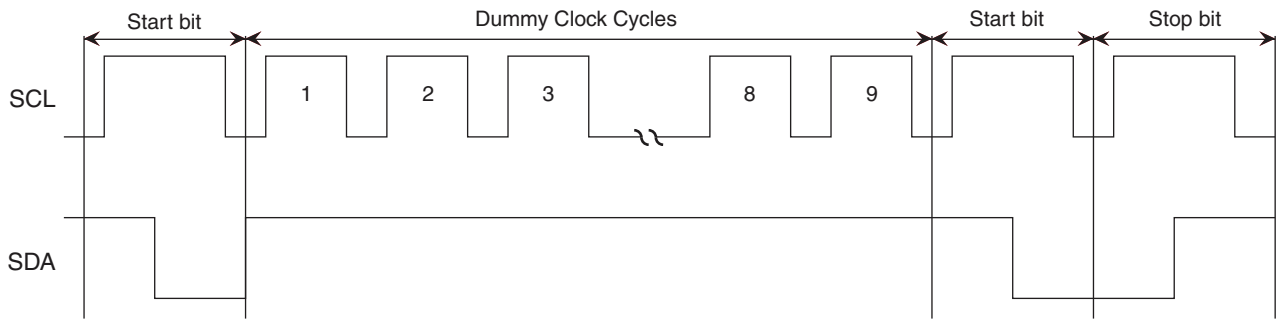


Figure 3-2. Bus Timing
SCL: Serial Clock, SDA: Serial Data I/O®

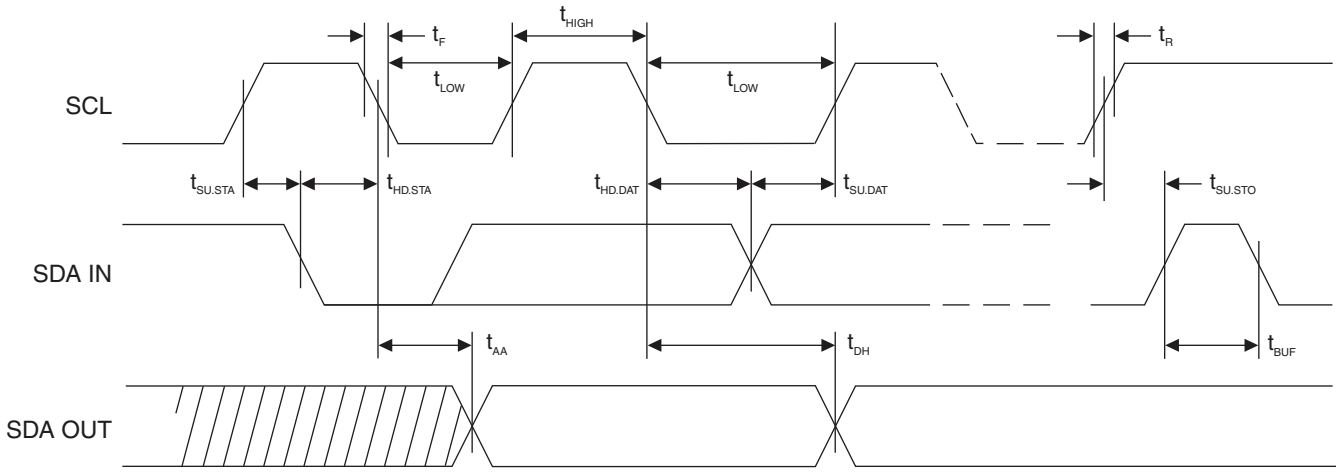
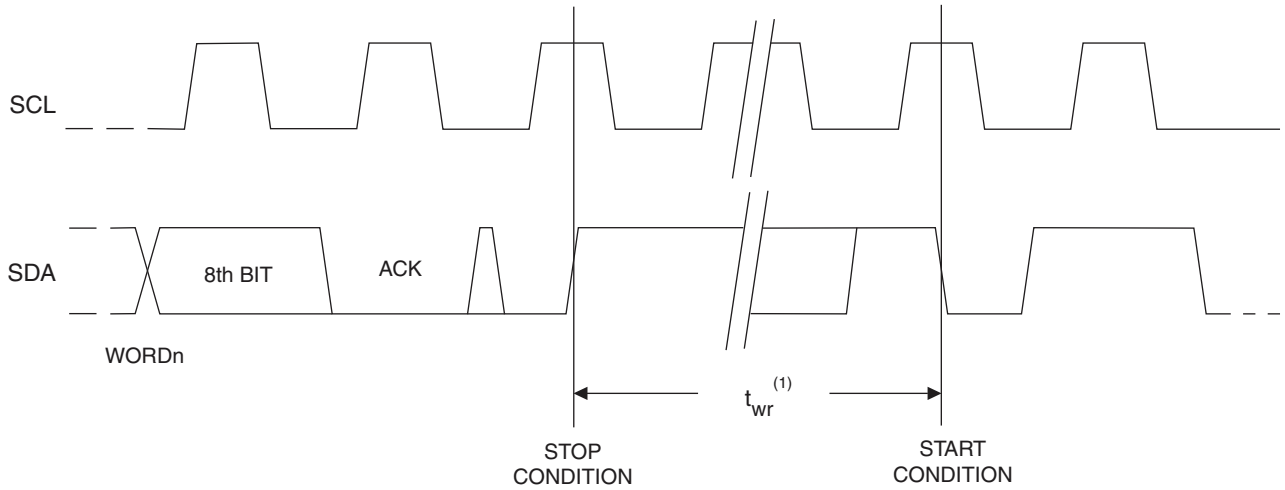


Figure 3-3. Write Cycle Timing
SCL: Serial Clock, SDA: Serial Data I/O



Note: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle

Figure 3-4. Data Validity

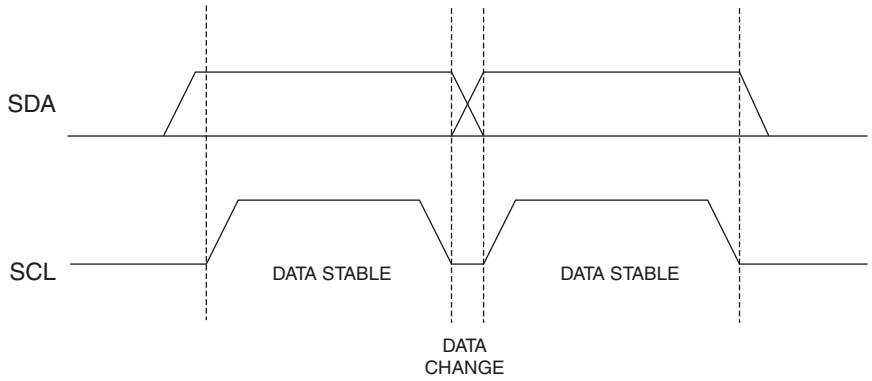


Figure 3-5. Start and Stop Definition

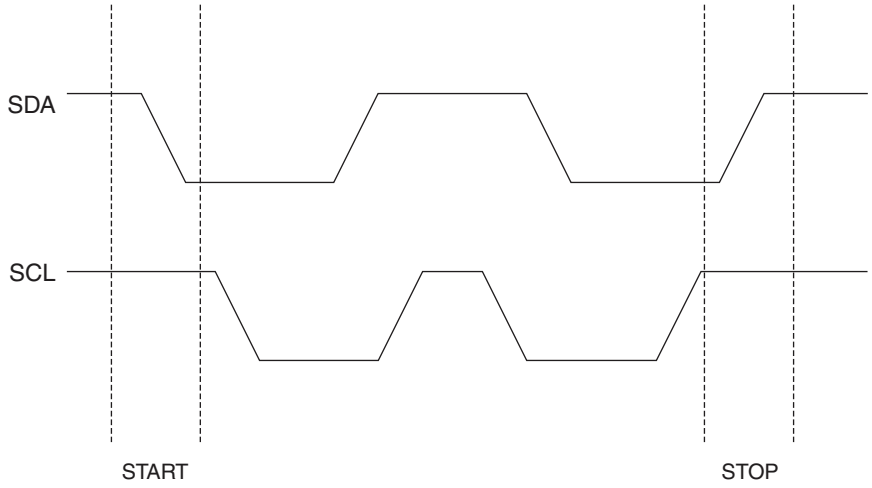
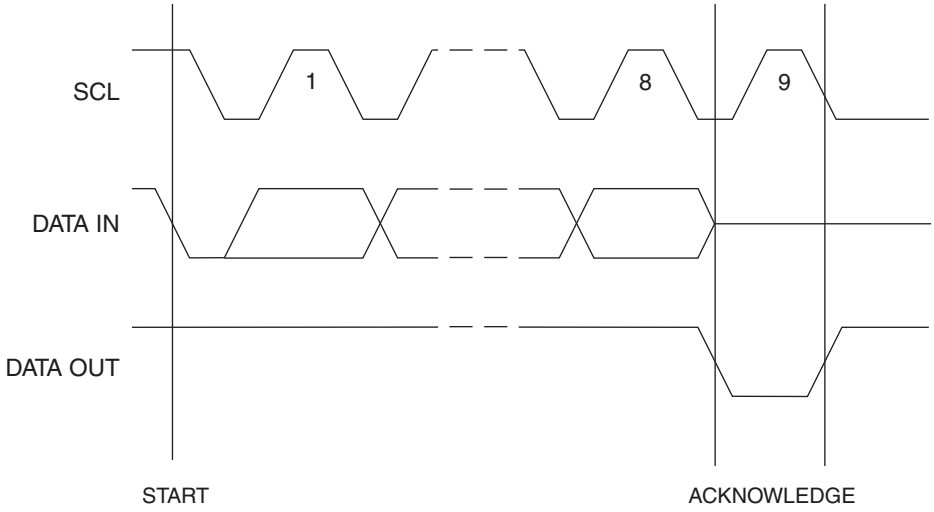


Figure 3-6. Output Acknowledge



4. Device Addressing

The 16K EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to <blue>Figure 6-1).

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the EEPROM devices.

The next three bits used for memory page addressing and are the most significant bits of the data word address which follows.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state.

5. Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see <blue>Figure 6-2 on page 10).

PAGE WRITE: The 16K EEPROM is capable of an 16-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see <blue>Figure 6-3 on page 11).

The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

6. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page to the first byte of the first page. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (see <blue>Figure 6-4 on page 11).

RANDOM READ: A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see <blue>Figure 6-5 on page 11).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see <blue>Figure 6-6 on page 11).

Figure 6-1. Device Address

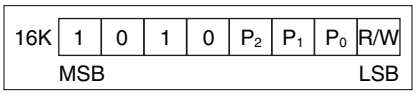
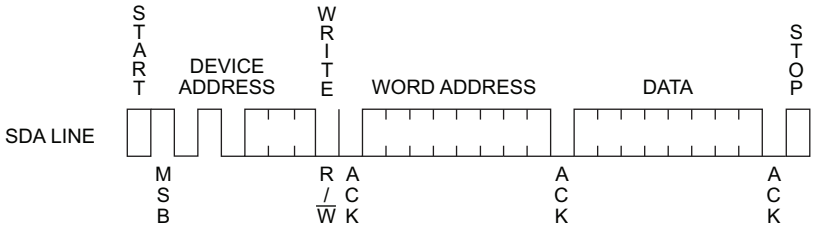


Figure 6-2. Byte Write



分销商库存信息:		
ATMEL		
AT24C16C-SSHM-T	AT24C16C-SSHM-B	AT24C16C-PUM
AT24C16C-XHM-T	AT24C16C-XHM-B	AT24C16C-STUM-T
AT24C16C-MAHM-T		