



16-/32- Channel, 3.5 Ω 1.8 V to 5.5 V, ± 2.5 V, Analog Multiplexers

Preliminary Technical Data

ADG726/ADG732

FEATURES

1.8 V to 5.5 V Single Supply
 ± 2.5 V Dual Supply Operation
3.5 Ω On Resistance
0.5 Ω On Resistance Flatness
Rail to Rail Operation
30ns Switching Times
Single 32 to 1 Channel Multiplexer
Dual/Differential 16 to 1 Channel Multiplexer
TTL/CMOS Compatible Inputs
For Functionally Equivalent devices with Serial Interface
See ADG725/ADG731

APPLICATIONS

Optical Applications
Data Acquisition Systems
Communication Systems
Relay replacement
Audio and Video Switching
Battery Powered Systems
Medical Instrumentation
Automatic Test Equipment

GENERAL DESCRIPTION

The ADG726/ADG732 are monolithic CMOS 32 channel/dual 16 channel analog multiplexers. The ADG732 switches one of thirty-two inputs (S1-S32) to a common output, D, as determined by the 5-bit binary address lines A0, A1, A2, A3 and A4. The ADG726 switches one of sixteen inputs as determined by the four bit binary address lines, A0, A1, A2 and A3.

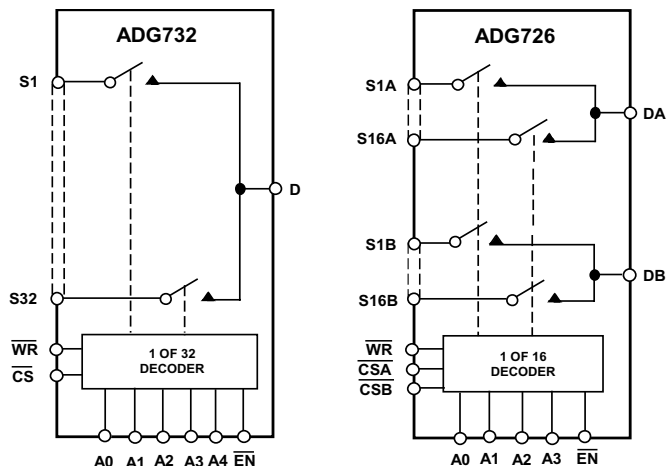
On chip latches facilitate microprocessor interfacing. The ADG726 device may also be configured for differential operation by tying CSA and CSB together. An $\overline{\text{EN}}$ input is used to enable or disable the devices. When disabled, all channels are switched OFF.

These multiplexers are designed on an enhanced submicron process that provides low power dissipation yet gives high switching speed, very low on resistance and leakage currents. They operate from single supply of 1.8V to 5.5V and ± 2.5 V dual supply, making them ideally suited to a variety of applications. On resistance is in the region of a few Ohms and is closely matched between switches and very flat over the full signal range. These parts can operate equally well as either Multiplexers or De-Multiplexers

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FUNCTIONAL BLOCK DIAGRAMS



and have an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All channels exhibit break before make switching action preventing momentary shorting when switching channels.

They are available in either 48 lead LFCSP or TQFP package.

PRODUCT HIGHLIGHTS

1. +1.8 V to +5.5 V Single or ± 2.5 V Dual Supply operation. These parts are specified and guaranteed with +5 V $\pm 10\%$, +3 V $\pm 10\%$ single supply and ± 2.5 V $\pm 10\%$ dual supply rails.
2. On Resistance of 3.5 Ω .
3. Guaranteed Break-Before-Make Switching Action.
4. 7mm x 7mm 48 lead LF Chip Scale Package (CSP) or 48 lead TQFP package.

PRELIMINARY TECHNICAL DATA

ADG726/ADG732—SPECIFICATIONS¹ ($V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $GND = 0V$, unless otherwise noted)

Parameter	B Version		Units	Test Conditions/Comments
	+25°C	-40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On-Resistance (R_{ON})	3.5	6	Ω typ Ω max	$V_S = 0V$ to V_{DD} , $I_{DS} = 10\text{ mA}$; Test Circuit 1
On-Resistance Match Between Channels (ΔR_{ON})		0.3	Ω typ	$V_S = 0V$ to V_{DD} , $I_{DS} = 10\text{ mA}$
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.5	0.8	Ω max Ω typ Ω max	$V_S = 0V$ to V_{DD} , $I_{DS} = 10\text{ mA}$
		1.2		
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	± 0.01		nA typ	$V_{DD} = 5.5V$ $V_D = 4.5V/1V$, $V_S = 1V/4.5V$; Test Circuit 2
	± 0.5	± 5	nA max	
Drain OFF Leakage I_D (OFF)	± 0.01		nA typ	$V_D = 4.5V/1V$, $V_S = 1V/4.5V$; Test Circuit 3
	± 0.5	± 5	nA max	
Channel ON Leakage I_D , I_S (ON)	± 0.01		nA typ	$V_D = V_S = 1V$, or $4.5V$; Test Circuit 4
	± 1	± 10	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current I_{INL} or I_{INH}	0.005		μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.1		
C_{IN} , Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS²				
$t_{TRANSITION}$	40	60	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, Test Circuit 5; $V_{S1} = 3V/0V$, $V_{S32} = 0V/3V$
Break-Before-Make Time Delay, t_D	30	1	ns typ ns min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 3V$, Test Circuit 6
$t_{ON}(EN, \overline{WR})$	32	50	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 3V$, Test Circuit 7
$t_{OFF}(EN)$	10	14	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 3V$, Test Circuit 8
Charge Injection	± 5		pC typ	$V_S = 0V$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; Test Circuit 9
Off Isolation	-60		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; Test Circuit 10
Channel to Channel Crosstalk	-60		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; Test Circuit 11
-3 dB Bandwidth	10		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 10
C_S (OFF)	13		pF typ	$f = 1\text{ MHz}$
C_D (OFF)				
ADG726	180		pF typ	$f = 1\text{ MHz}$
ADG732	360		pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)				
ADG726	200		pF typ	$f = 1\text{ MHz}$
ADG732	400		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS				
I_{DD}	10	20	μA typ μA max	$V_{DD} = +5.5V$ Digital Inputs = $0V$ or $+5.5V$

NOTES

¹Temperature range is as follows: B Version: -40°C to $+85^\circ\text{C}$.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS¹ ($V_{DD} = 3V \pm 10\%$, $V_{SS} = 0V$, $GND = 0V$, unless otherwise noted)

Parameter	B Version		Units	Test Conditions/Comments
	+25°C	-40°C to +85°C		
ANALOG SWITCH				
Analogue Signal Range		0 V to V_{DD}	V	
On-Resistance (R_{ON})	6		Ω typ	$V_S = 0V$ to V_{DD} , $I_{DS} = 10$ mA;
	11	12	Ω max	Test Circuit 1
On-Resistance Match Between Channels (ΔR_{ON})		0.4	Ω typ	$V_S = 0V$ to V_{DD} , $I_{DS} = 10$ mA
On-Resistance Flatness ($R_{FLAT(ON)}$)		1.2	Ω max	
		3	Ω max	$V_S = 0V$ to V_{DD} , $I_{DS} = 10$ mA
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	± 0.01		nA typ	$V_{DD} = 3.3V$
	± 1	± 5	nA max	$V_S = 3V/1V$, $V_D = 1V/3V$;
Drain OFF Leakage I_D (OFF)	± 0.01		nA typ	Test Circuit 2
	± 1	± 5	nA max	$V_S = 1V/3V$, $V_D = 3V/1V$;
Channel ON Leakage I_D , I_S (ON)	± 0.01		nA typ	Test Circuit 3
	± 1	± 10	nA max	$V_S = V_D = +1V$ or $+3V$;
				Test Circuit 4
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.1	μA max	
C_{IN} , Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS²				
$t_{TRANSITION}$	45		ns typ	$R_L = 300\Omega$, $C_L = 35$ pF Test Circuit 5
		75	ns max	$V_{S1} = 2V/0V$, $V_{S32} = 0V/2V$
Break-Before-Make Time Delay, t_D	30		ns typ	$R_L = 300\Omega$, $C_L = 35$ pF;
		1	ns min	$V_S = 2V$, Test Circuit 6
$t_{ON}(EN, \overline{WR})$	40		ns typ	$R_L = 300\Omega$, $C_L = 35$ pF;
		70	ns max	$V_S = 2V$, Test Circuit 7
$t_{OFF}(EN)$	20		ns typ	$R_L = 300\Omega$, $C_L = 35$ pF;
		28	ns max	$V_S = 2V$, Test Circuit 8
Charge Injection	± 5		pC typ	$V_S = 0V$, $R_S = 0\Omega$, $C_L = 1$ nF;
				Test Circuit 9
Off Isolation	-60		dB typ	$R_L = 50\Omega$, $C_L = 5$ pF, $f = 1$ MHz;
				Test Circuit 10
Channel to Channel Crosstalk	-60		dB typ	$R_L = 50\Omega$, $C_L = 5$ pF, $f = 1$ MHz;
				Test Circuit 11
-3 dB Bandwidth	10		MHz typ	$R_L = 50\Omega$, $C_L = 5$ pF, Test Circuit 10
C_S (OFF)	13		pF typ	$f = 1$ MHz
C_D (OFF)				
ADG726	180		pF typ	$f = 1$ MHz
ADG732	360		pF typ	$f = 1$ MHz
C_D , C_S (ON)				
ADG726	200		pF typ	$f = 1$ MHz
ADG732	400		pF typ	$f = 1$ MHz
POWER REQUIREMENTS				
I_{DD}	10		μA typ	$V_{DD} = +3.3V$
		20	μA max	Digital Inputs = 0 V or +3.3 V

NOTES

¹Temperature ranges are as follows: B Version: -40°C to +85°C.²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ADG726/ADG732—SPECIFICATIONS¹ Dual Supply

($V_{DD} = +2.5\text{ V} \pm 10\%$, $V_{SS} = -2.5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted)

Parameter	B Version		Units	Test Conditions/Comments
	+25°C	-40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On-Resistance (R_{ON})	3.5		Ω typ	$V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10\text{ mA}$; Test Circuit 1
	5.5	6	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})		0.3	Ω typ	$V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10\text{ mA}$
		0.8	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.5		Ω typ	$V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10\text{ mA}$
		1.2	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	± 0.01		nA typ	$V_{DD} = +2.75\text{ V}$, $V_{SS} = -2.75\text{ V}$ $V_S = +2.25\text{ V}/-1.25\text{ V}$, $V_D = -1.25\text{ V}/+2.25\text{ V}$; Test Circuit 2
	± 1	± 5	nA max	
Drain OFF Leakage I_D (OFF)	± 0.01		nA typ	$V_S = +2.25\text{ V}/-1.25\text{ V}$, $V_D = -1.25\text{ V}/+2.25\text{ V}$; Test Circuit 3
	± 1	± 5	nA max	
Channel ON Leakage I_D , I_S (ON)	± 0.01		nA typ	$V_S = V_D = +2.25\text{ V}/-1.25\text{ V}$, Test Circuit 4
	± 1	± 10	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		1.7	V min	
Input Low Voltage, V_{INL}		0.7	V max	
Input Current I_{INL} or I_{INH}	0.005		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.1	μA max	
C_{IN} , Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS²				
$t_{TRANSITION}$	40		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ Test Circuit 5
		60	ns max	$V_{S1} = 1.5\text{ V}/0\text{ V}$, $V_{S32} = 0\text{ V}/1.5\text{ V}$
Break-Before-Make Time Delay, t_D	15		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$;
		1	ns min	$V_S = 1.5\text{ V}$, Test Circuit 6
$t_{ON}(EN, \overline{WR})$	32		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$;
		50	ns max	$V_S = 1.5\text{ V}$, Test Circuit 7
$t_{OFF}(EN)$	16		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$;
		26	ns max	$V_S = 1.5\text{ V}$, Test Circuit 8
Charge Injection	± 8		pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; Test 9
Off Isolation	-60		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 10
Channel to Channel Crosstalk	-60		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 11
-3 dB Bandwidth	10		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 10
C_S (OFF)	13		pF typ	
C_D (OFF)				
ADG726	180		pF typ	$f = 1\text{ MHz}$
ADG732	360		pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)				
ADG726	200		pF typ	$f = 1\text{ MHz}$
ADG732	400		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS				
I_{DD}	10		μA typ	$V_{DD} = +2.75\text{ V}$ Digital Inputs = 0 V or +2.75 V
		20	μA max	
I_{SS}	10		μA typ	$V_{SS} = -2.75\text{ V}$ Digital Inputs = 0 V or +2.75 V
		20	μA max	

NOTES

¹Temperature range is as follows: B Version: -40°C to +85°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

TIMING CHARACTERISTICS^{1,2,3}

Parameter	Limit at T _{MIN} , T _{MAX}	Units	Conditions/Comments
t ₁	0	ns min	\overline{CS} to \overline{WR} Setup Time
t ₂	0	ns min	\overline{CS} to \overline{WR} Hold Time
t ₃	20	ns min	\overline{WR} pulse width
t ₄	10	ns min	Time between \overline{WR} cycles
t ₅	5	ns min	Address, Enable Setup Time
t ₆	2	ns min	Address, Enable Hold Time

NOTES

¹See Figure 1.²All input signals are specified with t_r = t_f = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.³Guaranteed by design and characterisation, not production tested.

Specifications subject to change without notice.

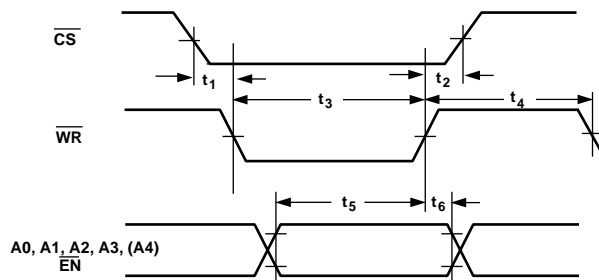


Figure 1. Timing Diagram

Figure 1 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while \overline{WR} is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of \overline{WR} . The ADG726 has two \overline{CS} inputs. This enables the part to be used either as a dual 16-1 channel multiplexer or a differential 16 channel multiplexer. If a differential output is required, tie \overline{CSA} and \overline{CSB} together.

PRELIMINARY TECHNICAL DATA

ADG726/ADG732

ABSOLUTE MAXIMUM RATINGS¹

(T_A = +25°C unless otherwise noted)

V _{DD} to V _{SS}	+7 V
V _{DD} to GND	-0.3 V to +7 V
V _{SS} to GND	+0.3 V to -7 V
Analog Inputs ²	V _{SS} - 0.3 V to V _{DD} +0.3 V or 30 mA, Whichever Occurs First
Digital Inputs ²	-0.3V to V _{DD} +0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	60mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D	30mA
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C

Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
48 lead CSP θ _{JA} Thermal Impedance	TBD°C/W
48 lead TQFP θ _{JA} Thermal Impedance	TBD°C/W
Lead Temperature, Soldering (10seconds)	300°C
IR Reflow, Peak Temperature	+220°C

NOTES

¹Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at A, \overline{WR} , \overline{RS} , S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

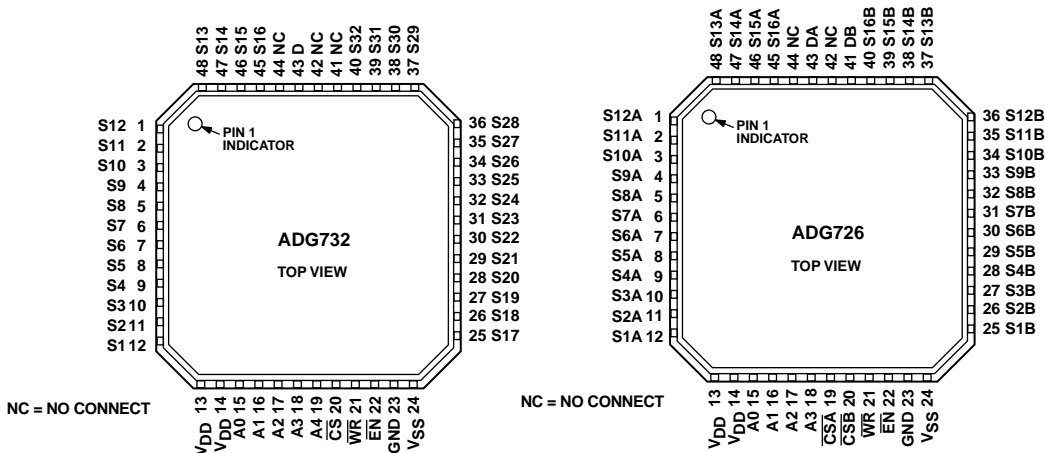
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG726/ADG732 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG726BCP	-40 °C to +85 °C	Chip Scale Package (CSP)	CP-48
ADG726BSU	-40 °C to +85 °C	Thin Quad Flatpack	SU-48
ADG732BCP	-40 °C to +85 °C	Chip Scale Package (CSP)	CP-48
ADG732BSU	-40 °C to +85 °C	Thin Quad Flatpack	SU-48

PIN CONFIGURATIONS CSP & TQFP



PRELIMINARY TECHNICAL DATA

ADG726/ADG732

Table 1. ADG726 Truth Table

A3	A2	A1	A0	$\overline{E}\overline{N}$	$\overline{C}\overline{S}\overline{A}$	$\overline{C}\overline{S}\overline{B}$	$\overline{W}\overline{R}$	ON Switch
X	X	X	X	X	1	1	L->H	Retains previous switch condition
X	X	X	X	X	1	1	X	No Change in Switch condition
X	X	X	X	1	0	0	0	NONE
0	0	0	0	0	0	0	0	S1A - DA, S1B - DB
0	0	0	1	0	0	0	0	S2A - DA, S2B - DB
0	0	1	0	0	0	0	0	S3A - DA, S3B - DB
0	0	1	1	0	0	0	0	S4A - DA, S4B - DB
0	1	0	0	0	0	0	0	S5A - DA, S5B - DB
0	1	0	1	0	0	0	0	S6A - DA, S6B - DB
0	1	1	0	0	0	0	0	S7A - DA, S7B - DB
0	1	1	1	0	0	0	0	S8A - DA, S8B - DB
1	0	0	0	0	0	0	0	S9A - DA, S9B - DB
1	0	0	1	0	0	0	0	S10A - DA, S10B - DB
1	0	1	0	0	0	0	0	S11A - DA, S11B - DB
1	0	1	1	0	0	0	0	S12A - DA, S12B - DB
1	1	0	0	0	0	0	0	S13A - DA, S13B - DB
1	1	0	1	0	0	0	0	S14A - DA, S14B - DB
1	1	1	0	0	0	0	0	S15A - DA, S15B - DB
1	1	1	1	0	0	0	0	S16A - DA, S16B - DB

Table 2. ADG732 Truth Table

A4	A3	A2	A1	A0	$\overline{E}\overline{N}$	$\overline{C}\overline{S}$	$\overline{W}\overline{R}$	Switch Condition
X	X	X	X	X	X	1	L->H	Retains previous switch condition
X	X	X	X	X	X	1	X	No Change in Switch Condition
X	X	X	X	X	1	0	0	NONE
0	0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	0	2
0	0	0	1	0	0	0	0	3
0	0	0	1	1	0	0	0	4
0	0	1	0	0	0	0	0	5
0	0	1	0	1	0	0	0	6
0	0	1	1	0	0	0	0	7
0	0	1	1	1	0	0	0	8
0	1	0	0	0	0	0	0	9
0	1	0	0	1	0	0	0	10
0	1	0	1	0	0	0	0	11
0	1	0	1	1	0	0	0	12
0	1	1	0	0	0	0	0	13
0	1	1	0	1	0	0	0	14
0	1	1	1	0	0	0	0	15
0	1	1	1	1	0	0	0	16
1	0	0	0	0	0	0	0	17
1	0	0	0	1	0	0	0	18
1	0	0	1	0	0	0	0	19
1	0	0	1	1	0	0	0	20
1	0	1	0	0	0	0	0	21
1	0	1	0	1	0	0	0	22
1	0	1	1	0	0	0	0	23
1	0	1	1	1	0	0	0	24
1	1	0	0	0	0	0	0	25
1	1	0	0	1	0	0	0	26
1	1	0	1	0	0	0	0	27
1	1	0	1	1	0	0	0	28
1	1	1	0	0	0	0	0	29
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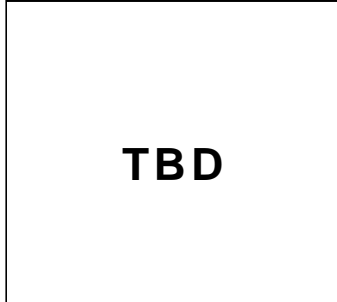
X = Don't Care
REV. PrD

ADG726/ADG732

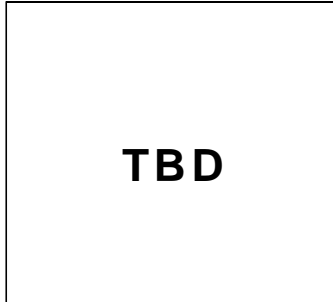
TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most Negative power supply in a dual supply application. In single supply applications, connect to GND.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
$V_D (V_S)$	Analog voltage on terminals D, S
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	On resistance match between any two channels, i.e. $R_{ONmax} - R_{ONmin}$
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_{INL}	Maximum input voltage for logic "0".
V_{INH}	Minimum input voltage for logic "1".
$I_{INL}(I_{INH})$	Input current of the digital input.
C_S (OFF)	"OFF" switch source capacitance. Measured with reference to ground.
C_D (OFF)	"OFF" switch drain capacitance. Measured with reference to ground.
C_D, C_S (ON)	"ON" switch capacitance. Measured with reference to ground.
C_{IN}	Digital input capacitance.
$t_{TRANSITION}$	Delay time measured between the 50% and 90% points of the digital inputs and the switch "ON" condition when switching from one address state to another.
$t_{ON}(\overline{EN})$	Delay time between the 50% and 90% points of the \overline{EN} digital input and the switch "ON" condition.
$t_{OFF}(\overline{EN})$	Delay time between the 50% and 90% points of the \overline{EN} digital input and the switch "OFF" condition.
t_{OPEN}	"OFF" time measured between the 80% points of both switches when switching from one address state to another.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Crosstalk	A measure of unwanted signal is coupled through from one channel to another as a result of parasitic capacitance.
On Response	The Frequency response of the "ON" switch.
Insertion Loss	The loss due to the ON resistance of the switch.

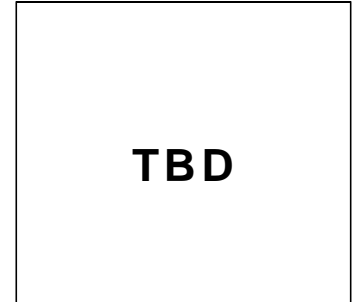
TYPICAL PERFORMANCE CHARACTERISTICS



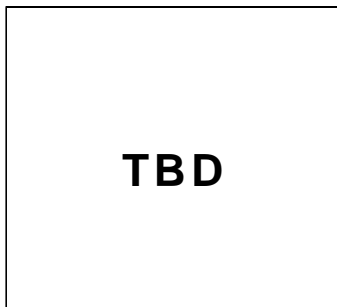
TPC 1. On Resistance as a Function of $V_D(V_S)$ for Single Supply



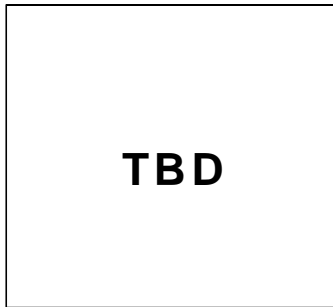
TPC 4. On Resistance as a Function of $V_D(V_S)$ for Different Temperatures, Single Supply



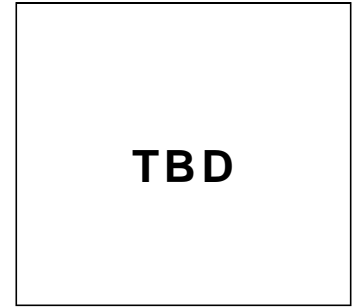
TPC 7. Leakage Currents as a function of $V_D(V_S)$



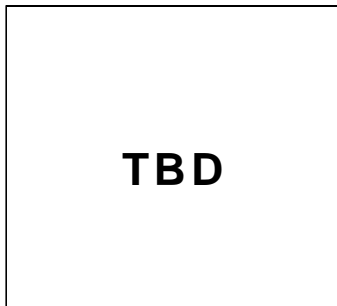
TPC 2. On Resistance as a Function of $V_D(V_S)$ for Dual Supply



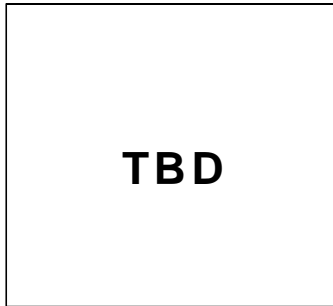
TPC 5. On Resistance as a Function of $V_D(V_S)$ for Different Temperatures, Dual Supply



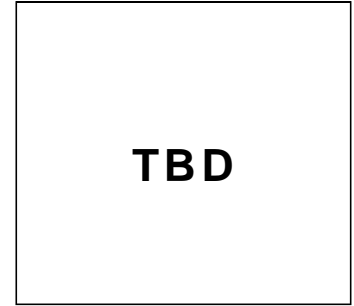
TPC 8. Leakage Currents as a function of $V_D(V_S)$



TPC 3. On Resistance as a Function of $V_D(V_S)$ for Different Temperatures, Single Supply



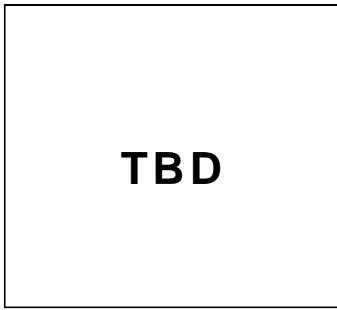
TPC 6. Leakage Currents as a function of $V_D(V_S)$



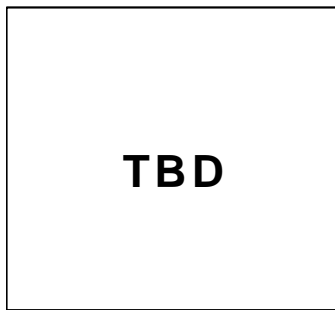
TPC 9. Leakage Currents as a function of Temperature

PRELIMINARY TECHNICAL DATA

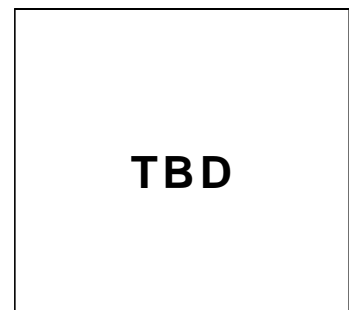
ADG726/ADG732



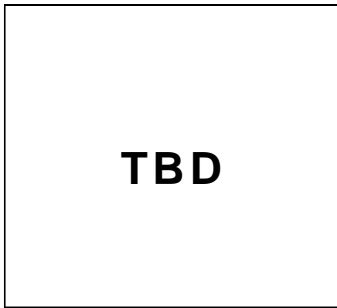
TPC 10. Leakage Currents as a Function of Temperature



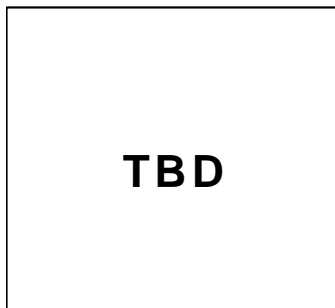
TPC 13. T_{ON}/T_{OFF} Times vs. Temperature



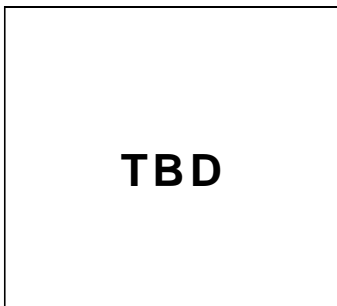
TPC 16. On Response vs. Frequency



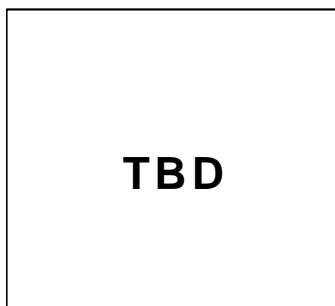
TPC 11. Supply Currents vs. Input Switching Frequency



TPC 14. Off Isolation vs. Frequency

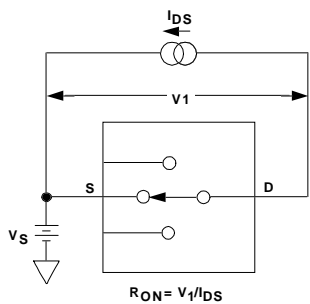


TPC 12. Charge Injection vs. Source Voltage

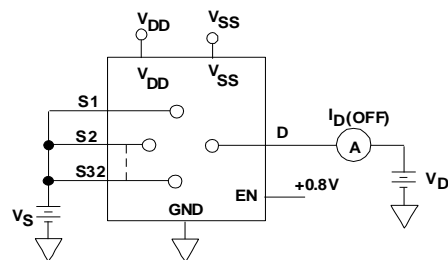


TPC 15. Crosstalk vs. Frequency

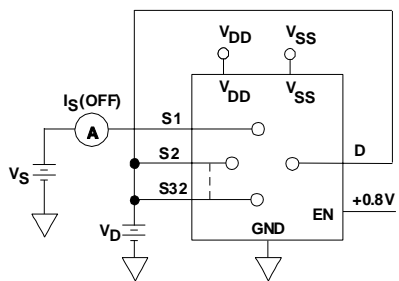
Test Circuits



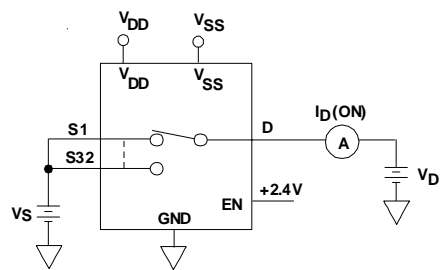
Test Circuit 1. On Resistance.



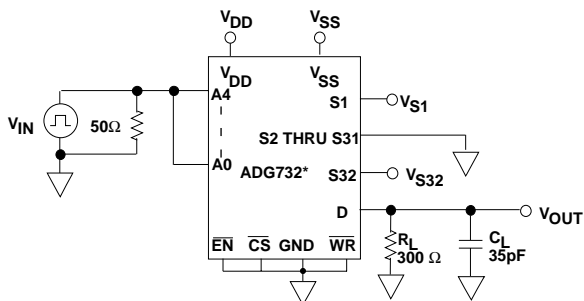
Test Circuit 3. I_D (OFF)



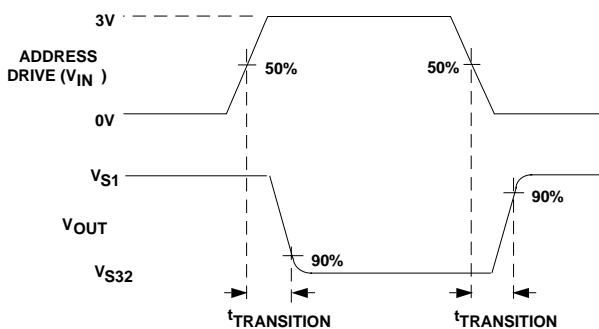
Test Circuit 2. I_S (OFF).



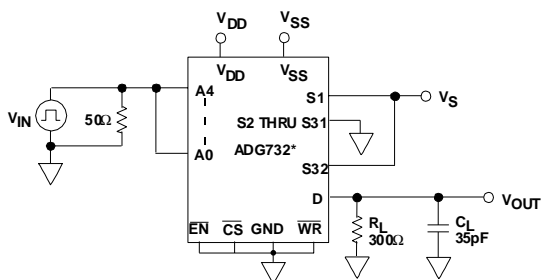
Test Circuit 4. I_D (ON)



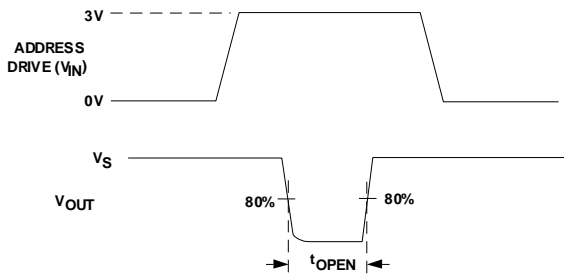
* SIMILAR CONNECTION FOR ADG726



Test Circuit 5. Switching Time of Multiplexer, $t_{TRANSITION}$.



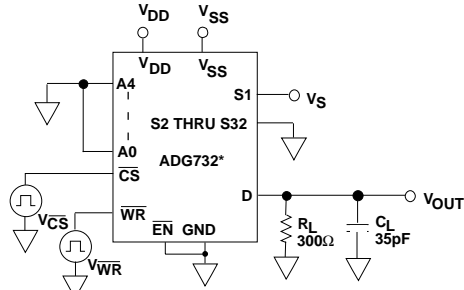
*SIMILAR CONNECTION FOR ADG726



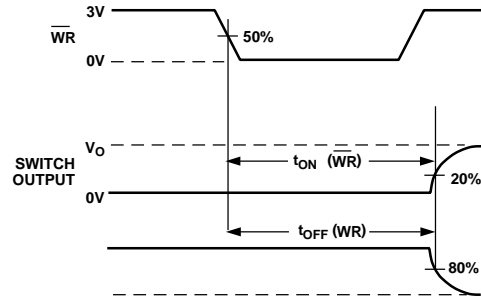
Test Circuit 6. Break Before Make Delay, t_{OPEN} .

PRELIMINARY TECHNICAL DATA

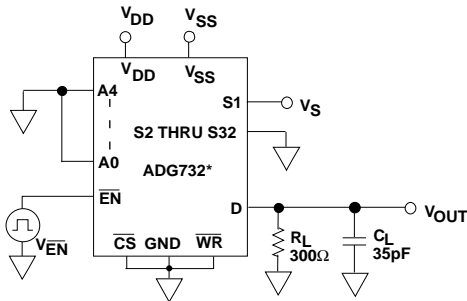
ADG726/ADG732



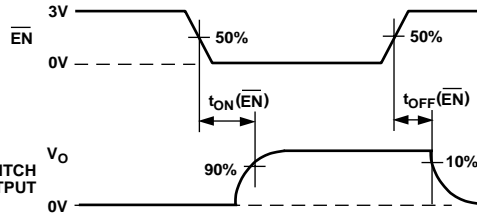
*SIMILAR CONNECTION FOR ADG726



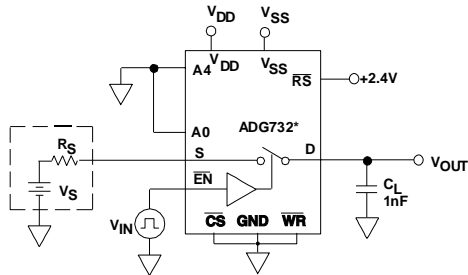
Test Circuit 7. Write Turn-On and Turn Off Time, t_{ON} , t_{OFF} (WR).



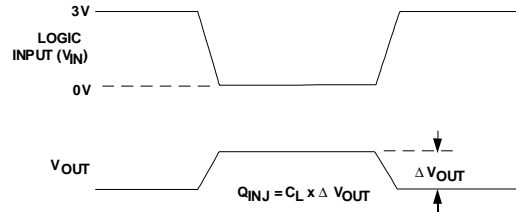
*SIMILAR CONNECTION FOR ADG726



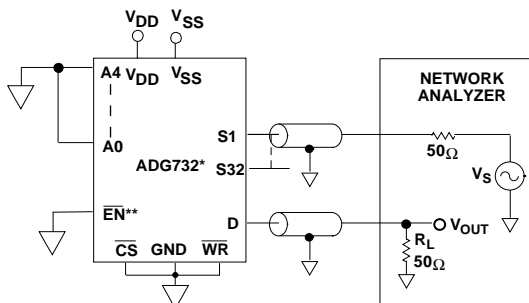
Test Circuit 8. Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$



*SIMILAR CONNECTION FOR ADG726



Test Circuit 9. Charge Injection.



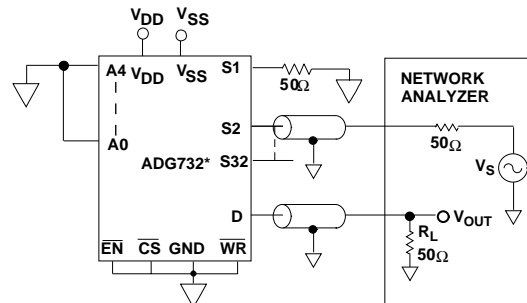
*SIMILAR CONNECTION FOR ADG726

** CONNECT TO 2.4V FOR CROSSTALK MEASUREMENTS

OFF ISOLATION = $20\text{LOG}_{10}(V_{OUT}/V_S)$

INSERTION LOSS = $20\text{LOG}_{10}\left(\frac{V_{OUT} \text{ WITH SWITCH}}{V_{OUT} \text{ WITHOUT SWITCH}}\right)$

Test Circuit 10. OFF Isolation and Bandwidth.



*SIMILAR CONNECTION FOR ADG726

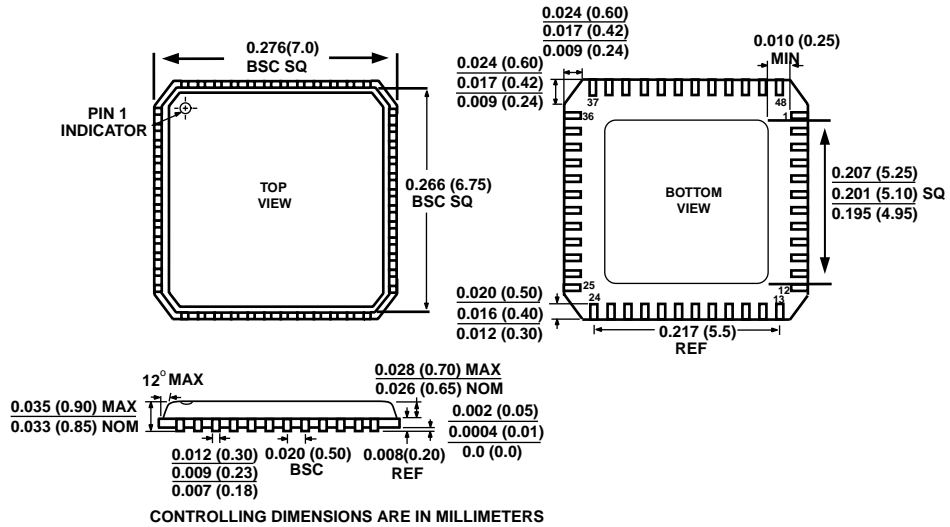
CHANNEL TO CHANNEL CROSSTALK=

$20\text{LOG}_{10}(V_{OUT}/V_S)$

Test Circuit 11. Channel-to-Channel Crosstalk.

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

**48-Lead CSP
(CP-48)**



**48-Lead TQFP
(SU-48)**

