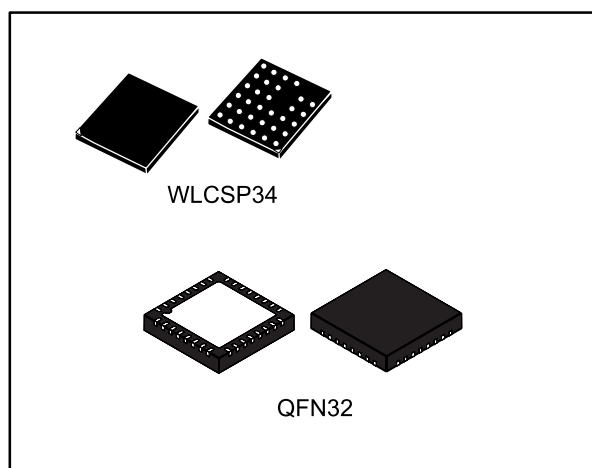


Upgradable Bluetooth® Low Energy network processor

Datasheet - production data



- High performance, ultra-low power Cortex-M0 32-bit based architecture core
- Upgradable BLE stack (stored in embedded Flash memory, via SPI)
- AES security co-processor
- Low power modes
- 16 or 32 MHz crystal oscillator
- 12 MHz ring oscillator
- 32 kHz crystal oscillator
- 32 kHz ring oscillator
- Compliant with the following radio frequency regulations: ETSI EN 300 328, EN 300 440, FCC CFR47 Part 15, ARIB STD-T66
- Available in QFN32 (5 x 5 mm) and WLCSP34 (2.66 x 2.56 mm) packages
- Operating temperature range: -40 °C to 85 °C

Features

- Bluetooth specification v4.0 compliant, slave single-mode Bluetooth low energy network processor
- Embedded Bluetooth low energy protocol stack: GAP, GATT, SM, L2CAP, LL, RF-PHY
- Bluetooth low energy profiles provided separately
- Operating supply voltage: from 2.0 to 3.6 V
- 8.2 mA maximum TX current (@0 dBm, 3.0 V)
- Down to 1.7 µA current consumption with active BLE stack
- Integrated linear regulator and DC-DC step-down converter
- Up to +8 dBm available output power (at antenna connector)
- Excellent RF link budget (up to 96 dB)
- Accurate RSSI to allow power control
- Proprietary application controller interface (ACI), SPI based, allows interfacing with an external host application microcontroller
- Full link controller and host security

Applications

- Watches
- Fitness, wellness and sports
- Consumer medical
- Security/proximity
- Remote control
- Home and industrial automation
- Assisted living
- Mobile phone peripherals
- PC peripherals

Table 1: Device summary

| Order code | Package | Packing |
|------------|-----------------------------|---------------|
| BLUENRGQTR | QFN32 (5 x 5 mm) | Tape and reel |
| BLUENRGCSP | WLCSP34 (2.66 x 2.56 mm) | Tape and reel |

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1 Description

The BlueNRG is a very low power Bluetooth Low Energy (BLE) single-mode network processor, compliant with Bluetooth specification v4.0. The BlueNRG can act as slave. The Bluetooth Low Energy stack runs on the embedded ARM Cortex-M0 core. The stack is stored on the on-chip non-volatile Flash memory and can be easily upgraded via SPI. The device comes pre-programmed with a production-ready stack image (whose version could change at any time without notice). A different or more up-to-date stack image can be downloaded from the ST web site and programmed on the device through the ST provided software tools. The BlueNRG allows applications to meet the tight advisable peak current requirements imposed by the use of standard coin cell batteries. The maximum peak current is only 10 mA at 1 dBm of output power. Ultra low-power sleep modes and very short transition times between operating modes allow very low average current consumption, resulting in longer battery life. The BlueNRG offers the option of interfacing with external microcontrollers using SPI transport layer.

2 General description

The BlueNRG is a single-mode Bluetooth low energy slave network processor, compliant with the Bluetooth specification v4.0.

It integrates a 2.4 GHz RF transceiver and a powerful Cortex-M0 microcontroller, on which a complete power-optimized stack for Bluetooth single mode protocol runs, providing:

- Slave role support
- GAP: peripheral, broadcaster roles
- ATT/GATT: client and server
- SM: privacy, authentication and authorization
- L2CAP
- Link Layer: AES-128 encryption and decryption

An on-chip non-volatile Flash memory allows on-field Bluetooth low energy stack upgrade.

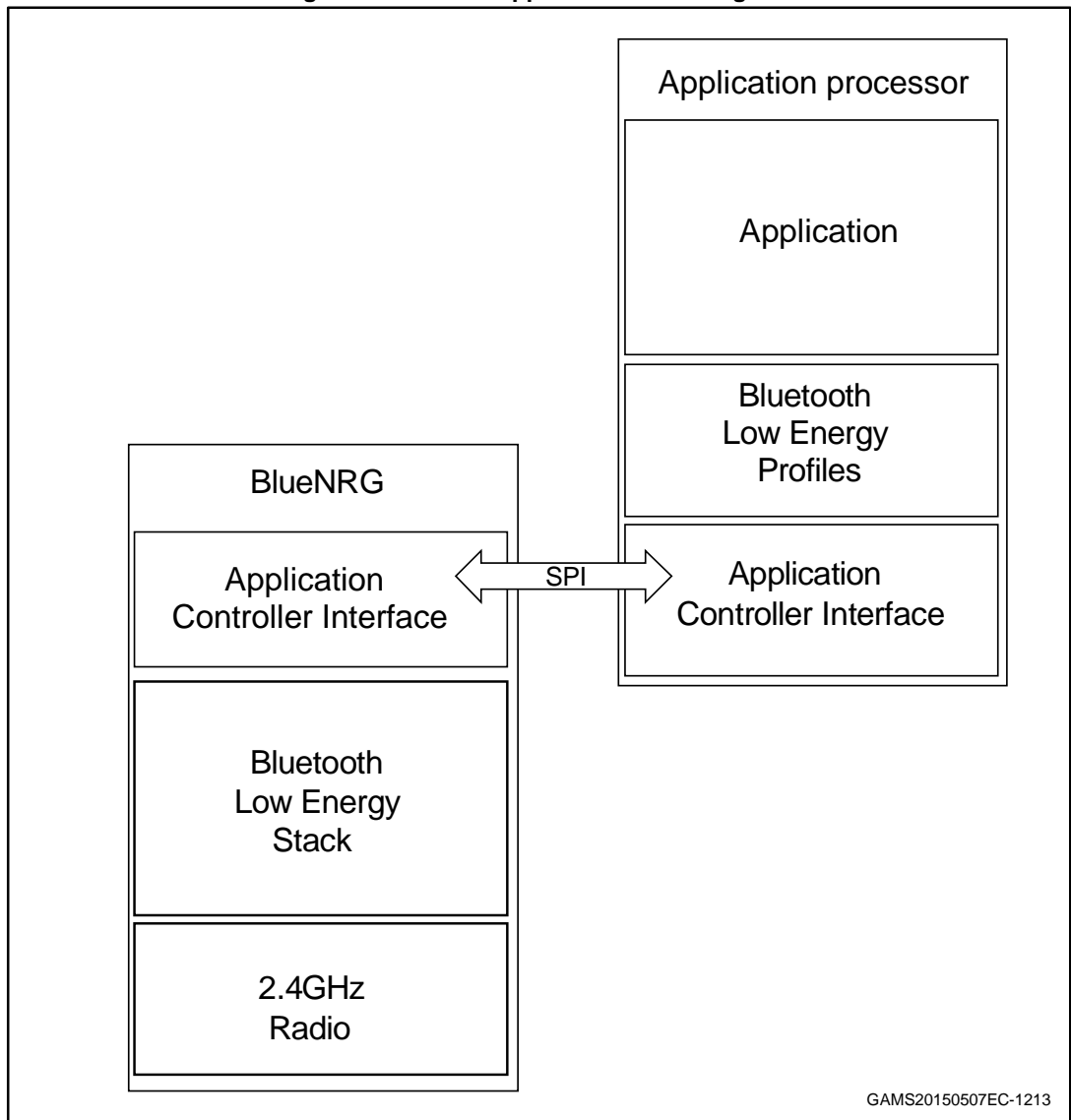
The device allows applications to meet the tight advisable peak current requirements imposed by the use of standard coin cell batteries. If the high efficiency embedded DC-DC step-down converter is used, the maximum input current is only 15 mA at the highest output power (+8 dBm). Even if the DC-DC converter is not used, the maximum input current is only 29 mA at the highest output power, still preserving battery life.

Ultra low-power sleep modes and very short transition time between operating modes result in very low average current consumption during real operating conditions, providing very long battery life.

Two different external matching networks are suggested: standard mode (TX output power up to +5 dBm) and high power mode (TX output power up to +8 dBm).

The external host application processor, where the application resides, is interfaced with the BlueNRG through an application controller interface protocol based on a standard SPI interface.

Figure 1: BlueNRG application block diagram



GAMS20150507EC-1213

3 Pin description

The device pinout is shown in *Figure 2: "Pinout top view (QFN32)"*, *Figure 3: "Pinout top view (WLCSP34)"* and *Figure 4: "Pinout bottom view (WLCSP34)"*. In *Table 2: "Pinout description"* a short description of the pins is provided.

Figure 2: Pinout top view (QFN32)

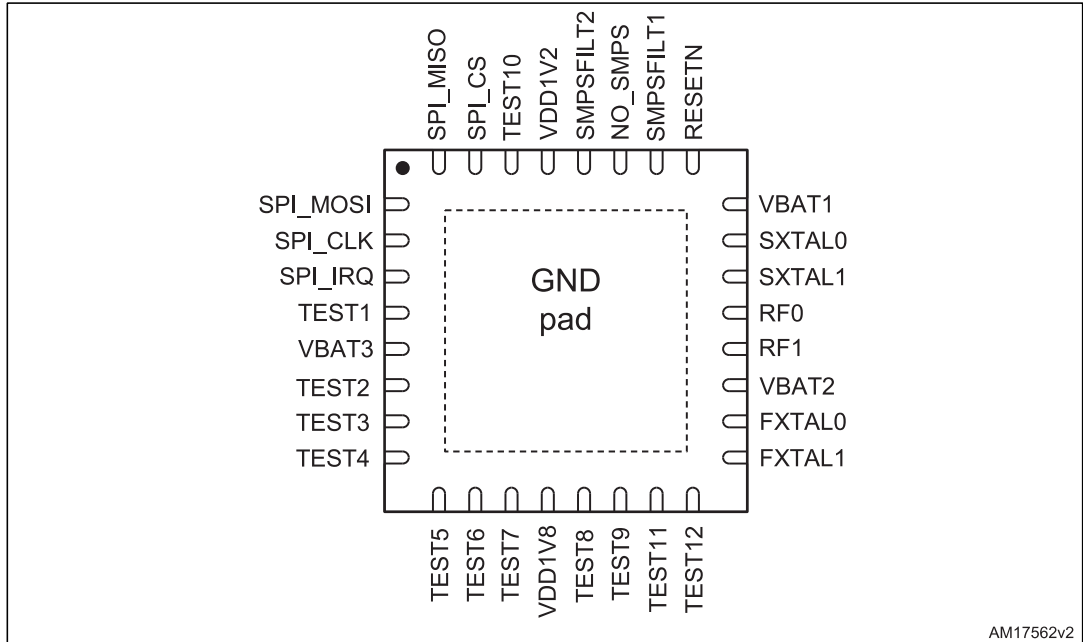
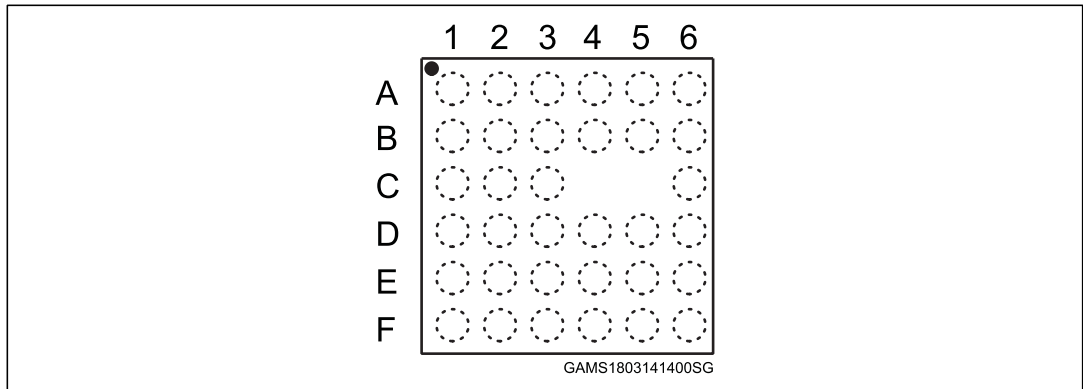


Figure 3: Pinout top view (WLCSP34)



Note: Top view (balls are underneath).

Figure 4: Pinout bottom view (WLCSP34)

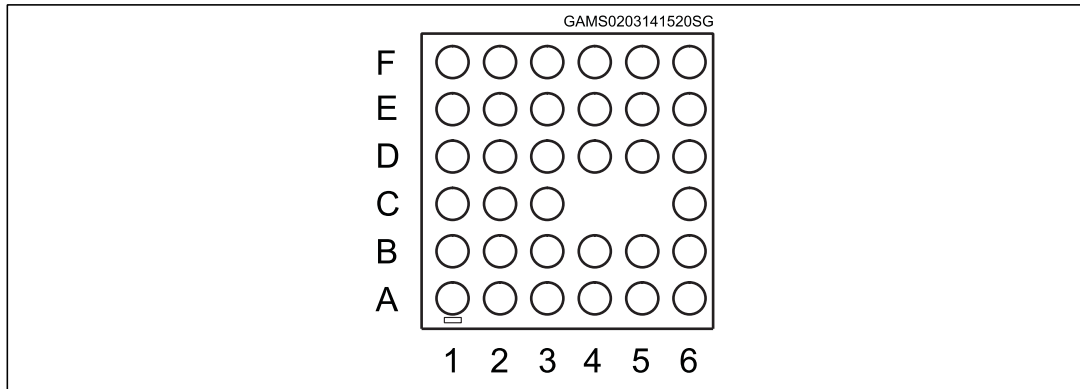


Table 2: Pinout description

| Pins | | Name | I/O | Description |
|-------|-------|----------|-----|---|
| QFN32 | WLCSP | | | |
| 1 | E2 | SPI_MOSI | I | SPI_MOSI |
| 2 | E1 | SPI_CLK | I | SPI_CLK |
| 3 | D2 | SPI_IRQ | O | SPI_IRQ |
| 4 | D1 | TEST1 | I/O | Test pin |
| 5 | C1 | VBAT3 | VDD | 2.0-3.6 battery voltage input |
| 6 | C2 | TEST2 | I/O | Test pin connected to GND |
| 7 | B1 | TEST3 | I/O | Test pin connected to GND |
| 8 | B2 | TEST4 | I/O | Test pin connected to GND |
| 9 | A1 | TEST5 | I/O | Test pin connected to GND |
| 10 | B3 | TEST6 | I/O | Test pin connected to GND |
| 11 | A2 | TEST7 | I/O | Test pin connected to GND |
| 12 | A3 | VDD1V8 | O | 1.8 V digital core |
| 13 | A4 | TEST8 | I/O | Test pin not connected |
| 14 | A5 | TEST9 | I/O | Test pin not connected |
| 15 | B4 | TEST11 | I/O | Test pin not connected (QFN32) Test pin connected to GND (WLCSP) |
| 16 | B5 | TEST12 | I/O | Test pin not connected (QFN32) Test pin connected to GND (WLCSP) |
| 17 | A6 | FXTAL1 | I | 16/32 MHz crystal |
| 18 | B6 | FXTAL0 | I | 16/32 MHz crystal |
| 19 | - | VBAT2 | VDD | 2.0-3.6 battery voltage input |
| 20 | C6 | RF1 | I/O | Antenna + matching circuit |
| 21 | D6 | RF0 | I/O | Antenna + matching circuit |
| 22 | E6 | SXTAL1 | I | 32 kHz crystal |
| 23 | E5 | SXTAL0 | I | 32 kHz crystal |
| 24 | D5 | VBAT1 | VDD | 2.0-3.6 battery voltage input |
| 25 | E4 | RESETN | I | Reset |

| Pins | | Name | I/O | Description |
|-------|-------|-----------|-----|-------------------------------------|
| QFN32 | WLCSP | | | |
| 26 | F6 | SMPSFILT1 | O | SMPS output |
| 27 | - | NO_SMPS | I | Power management strategy selection |
| 28 | F5 | SMPSFILT2 | I/O | SMPS input/output |
| 29 | F3 | VDD1V2 | O | 1.2 V digital core |
| 30 | E3 | TEST10 | I/O | TEST pin connected to GND |
| 31 | F2 | SPI_CS | I | SPI_CS |
| 32 | F1 | SPI_MISO | O | SPI_MISO |
| - | C3 | GND | GND | Ground |
| - | D3 | GND | GND | Ground |
| - | D4 | GND | GND | Ground |
| - | F4 | SMPS-GND | GND | SMPS ground |

4 Application circuits

The schematics below are purely indicative. For more detailed schematics, please refer to the "Reference design" and "Layout guidelines" which are provided as separate documents.

Figure 5: BlueNRG application circuit: active DC-DC converter QFN32 package

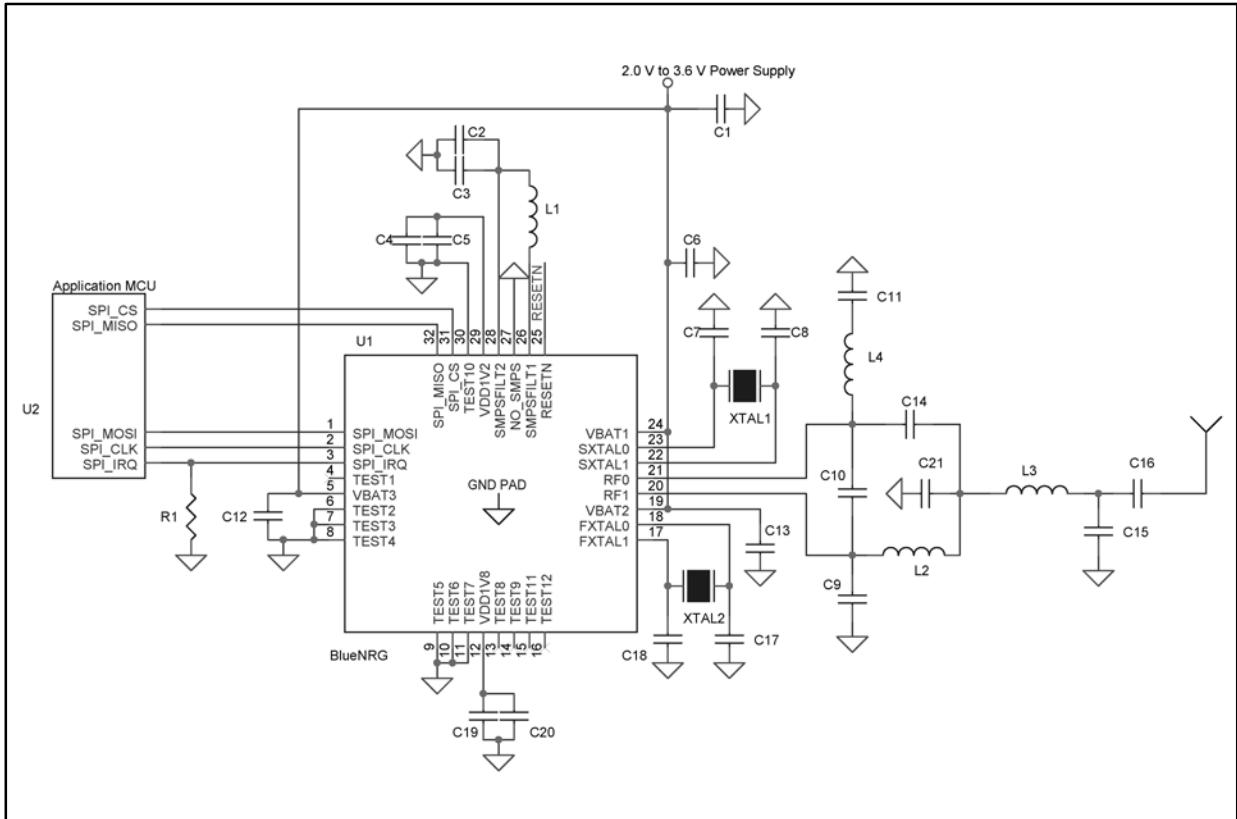


Figure 6: BlueNRG application circuit: non active DC-DC converter QFN32 package

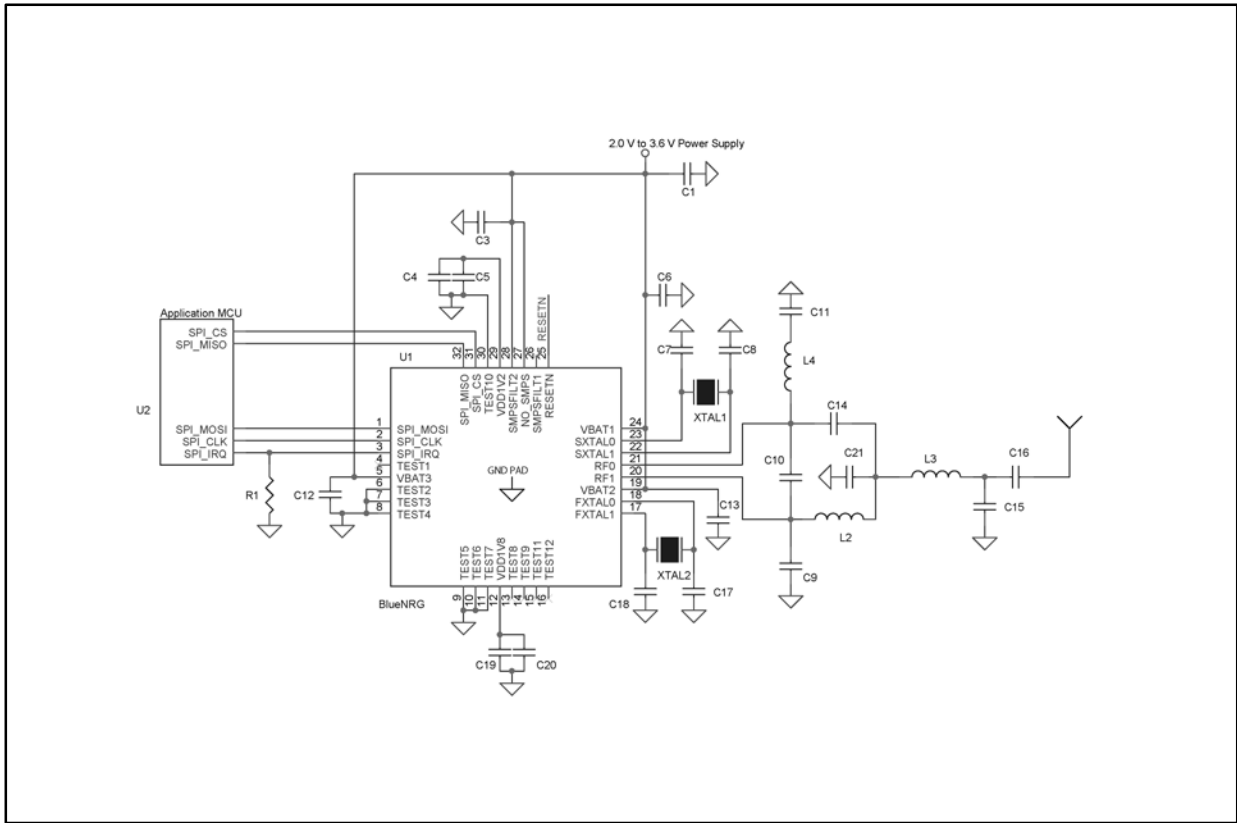


Figure 7: BlueNRG application circuit: active DC-DC converter WLCSP package

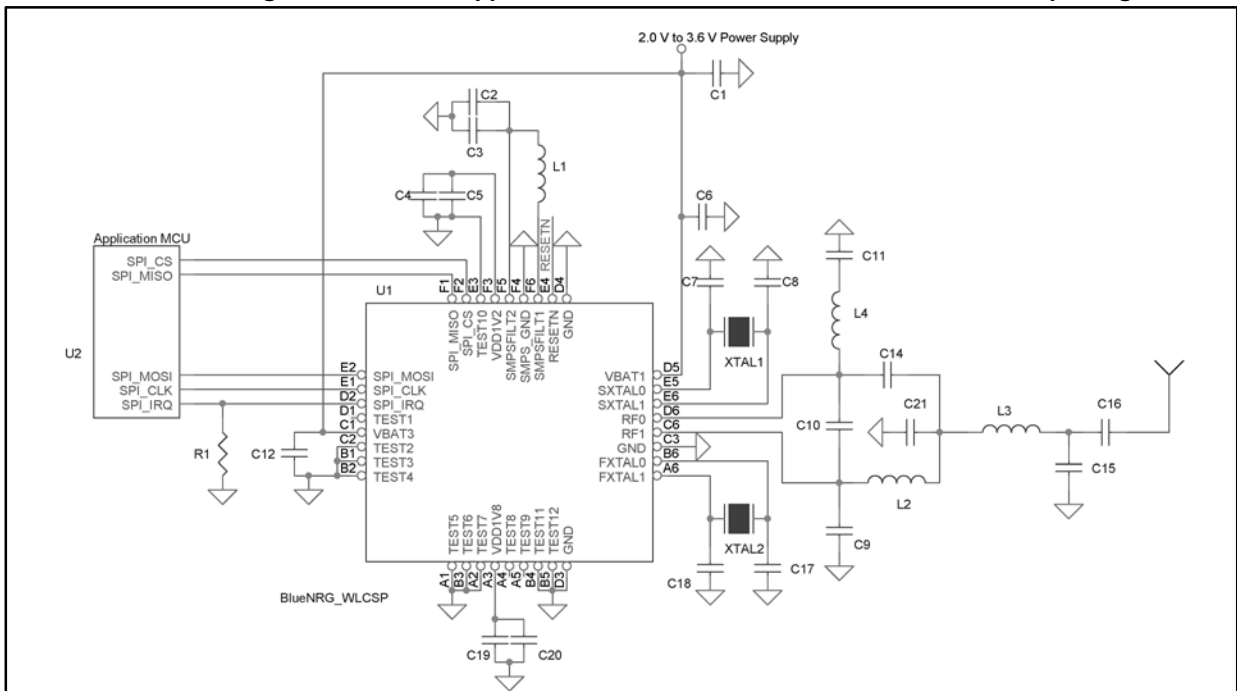


Figure 8: BlueNRG application circuit: non active DC-DC converter WLCSP package

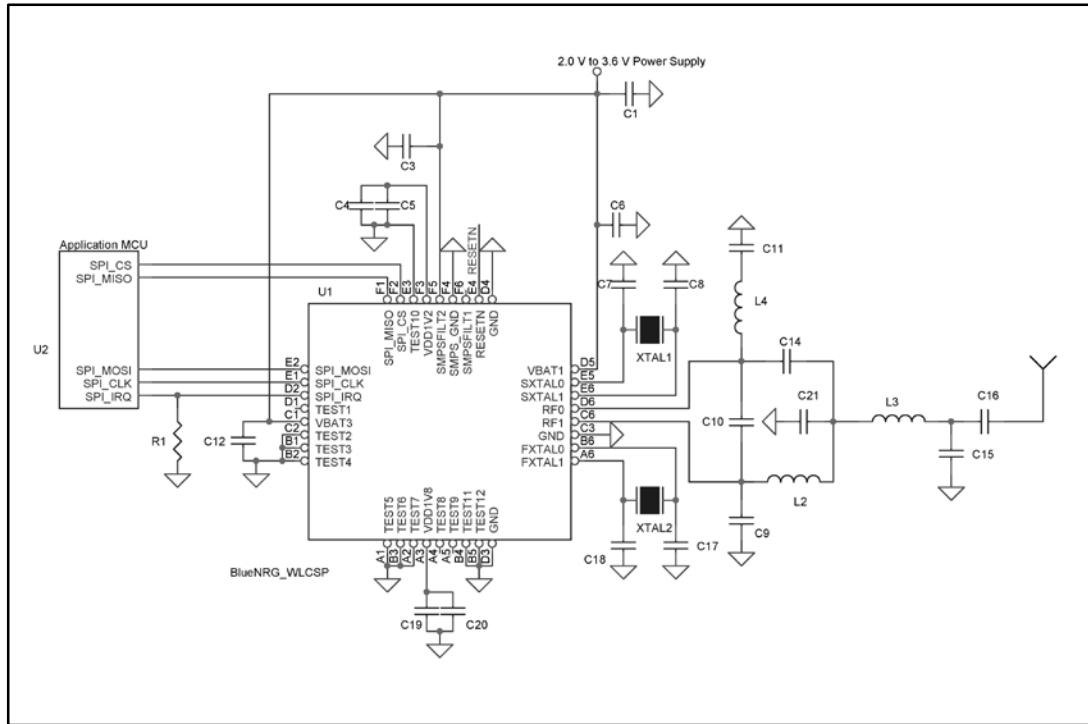


Table 3: External component list

| Component | Description |
|-----------|---|
| C1 | Decoupling capacitor |
| C2 | DC-DC converter output capacitor |
| C3 | DC-DC converter output capacitor |
| C4 | Decoupling capacitor for 1.2 V digital regulator |
| C5 | Decoupling capacitor for 1.2 V digital regulator |
| C6 | Decoupling capacitor |
| C7 | 32 kHz crystal loading capacitor ⁽¹⁾ |
| C8 | 32 kHz crystal loading capacitor ⁽¹⁾ |
| C9 | RF balun/matching network capacitor High Performance RF balun/matching network capacitor Standard mode |
| C10 | RF balun/matching network capacitor High Performance RF balun/matching network capacitor Standard mode |
| C11 | RF balun/matching network capacitor High Performance RF balun/matching network capacitor Standard mode |
| C12 | Decoupling capacitor |
| C13 | Decoupling capacitor |
| C14 | RF balun/matching network capacitor High Performance RF balun/matching network capacitor Standard mode |
| C15 | RF balun/matching network capacitor High Performance RF balun/matching network capacitor Standard mode |
| C16 | RF balun/matching network capacitor High Performance RF balun/matching network capacitor Standard mode |

| Component | Description |
|-----------|--|
| C17 | 16/32 MHz crystal loading capacitor |
| C18 | 16/32 MHz crystal loading capacitor |
| C19 | Decoupling capacitor for 1.8 V digital regulator |
| C20 | Decoupling capacitor for 1.8 V digital regulator |
| C21 | RF balun/matching network capacitor High Performance, RF balun/matching network capacitor Standard mode |
| L1 | DC-DC converter input inductor, Isat > 100 mA, Q > 25 |
| L2 | RF balun/matching network inductor High Performance RF balun/matching network inductor Standard mode |
| L3 | RF balun/matching network inductor High Performance RF balun/matching network inductor Standard mode |
| L4 | RF balun/matching network inductor High Performance RF balun/matching network inductor Standard mode |
| R1 | Pull-down resistor on the SPI_IRQ line (can be replaced by the internal pull-down of the Application MCU) |
| XTAL1 | 32 kHz crystal (optional) |
| XTAL2 | 16/32 MHz crystal |

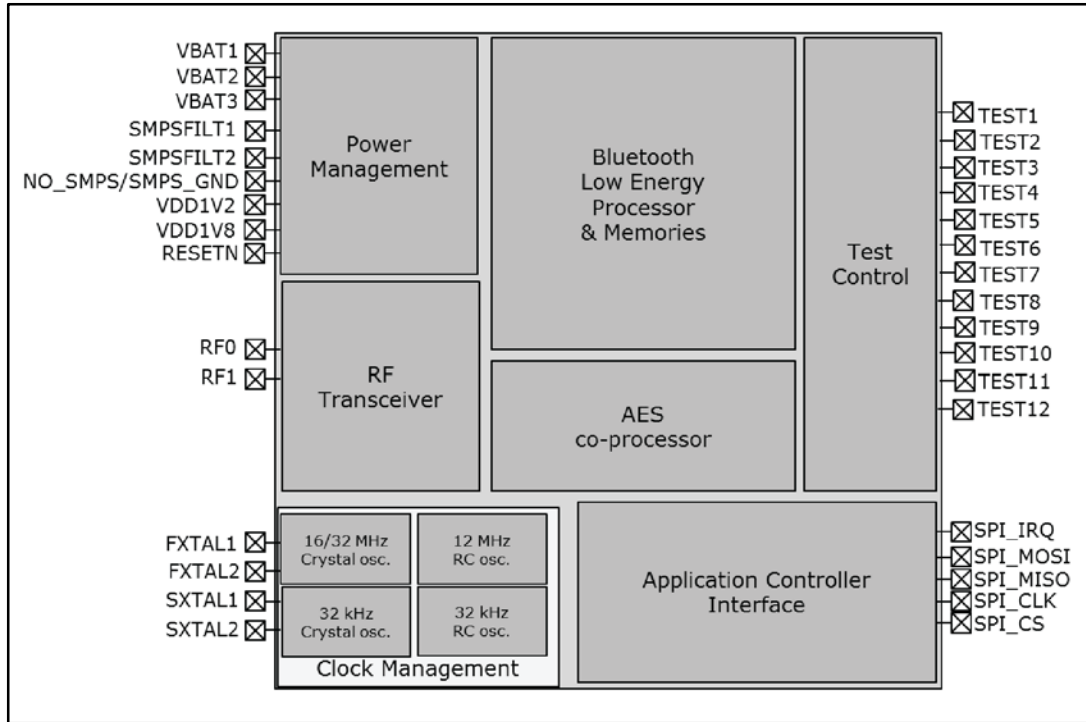
Notes:

⁽¹⁾Values valid only for the crystal NDK NX3215SA-32.768 kHz-EXS00A-MU00003. For other crystals refer to what specified in their datasheet.

5 Block diagram and descriptions

A block diagram of the device is shown in *Figure 9: "Block diagram"*. In the following subsections a short description of each module is given.

Figure 9: Block diagram



5.1 Core, memory and peripherals

The device contains an ARM Cortex-M0 microcontroller core that supports ultra-low leakage state retention mode and almost instantaneously returning to fully active mode on critical events.

The memory subsystem consists of 64 KB Flash, and 12 KB RAM , divided in two blocks of 6 KB (RAM1 and RAM2). Flash is used for the M0 program. No RAM or FLASH resources are available to the external microcontroller driving the BlueNRG.

The application controller interface (ACI) uses a standard SPI slave interface as transport layer, basing in five physical wires:

- 2 control wires (clock and slave select)
- 2 data wires with serial shift-out (MOSI and MISO) in full duplex
- 1 wire to indicate data availability from the slave

Table 4: SPI interface

| Name | Direction | Width | Description |
|----------|-----------|-------|--------------------------------|
| SPI_CS | In | 1 | SPI slave select = SPI enable. |
| SPI_CLK | In | 1 | SPI clock (max 8 MHz). |
| SPI_MOSI | In | 1 | Master output, slave input. |
| SPI_MISO | Out | 1 | Master input, slave output. |

| Name | Direction | Width | Description |
|---------|-----------|-------|----------------------------|
| SPI_IRQ | Out | 1 | Slave has data for master. |

All the SPI pins have an internal pull-down except for the CSN that has a pull-up. All the SPI pins, except the CSN, are in high impedance state during the low-power states. The IRQ pin needs a pull-down external resistor.

5.2 Power management

The device integrates both a low dropout voltage regulator (LDO) and a step-down DC-DC converter, and one of them can be used to power the internal circuitry. However even when the LDO is used, the stringent maximum current requirements, which are advisable when coin cell batteries are used, can be met and further improvements can be obtained with the DC-DC converter at the sole additional cost of an inductor and a capacitor.

The internal LDOs supplying both the 1.8 V digital blocks and 1.2 V digital blocks require decoupling capacitors for stable operation.

Figure 10: "Power management strategy using LDO" and *Figure 11: "Power management strategy using step-down DC-DC converter"*, show the simplified power management schemes using LDO and DC-DC converter.

Figure 10: Power management strategy using LDO

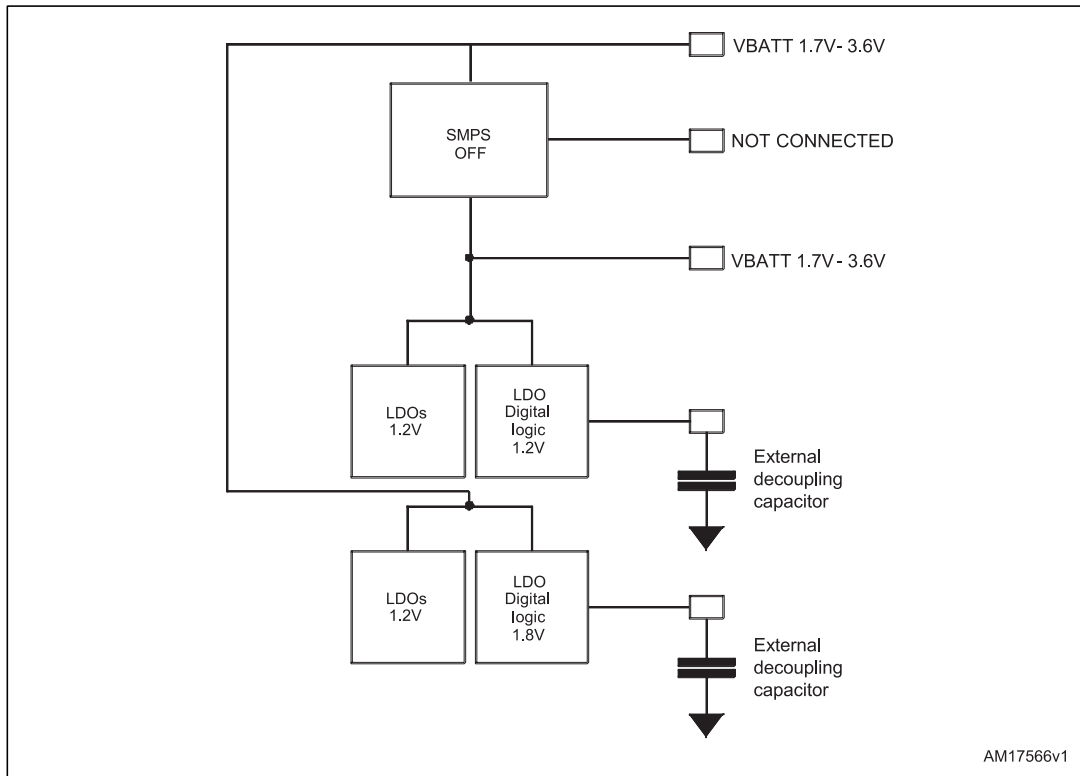
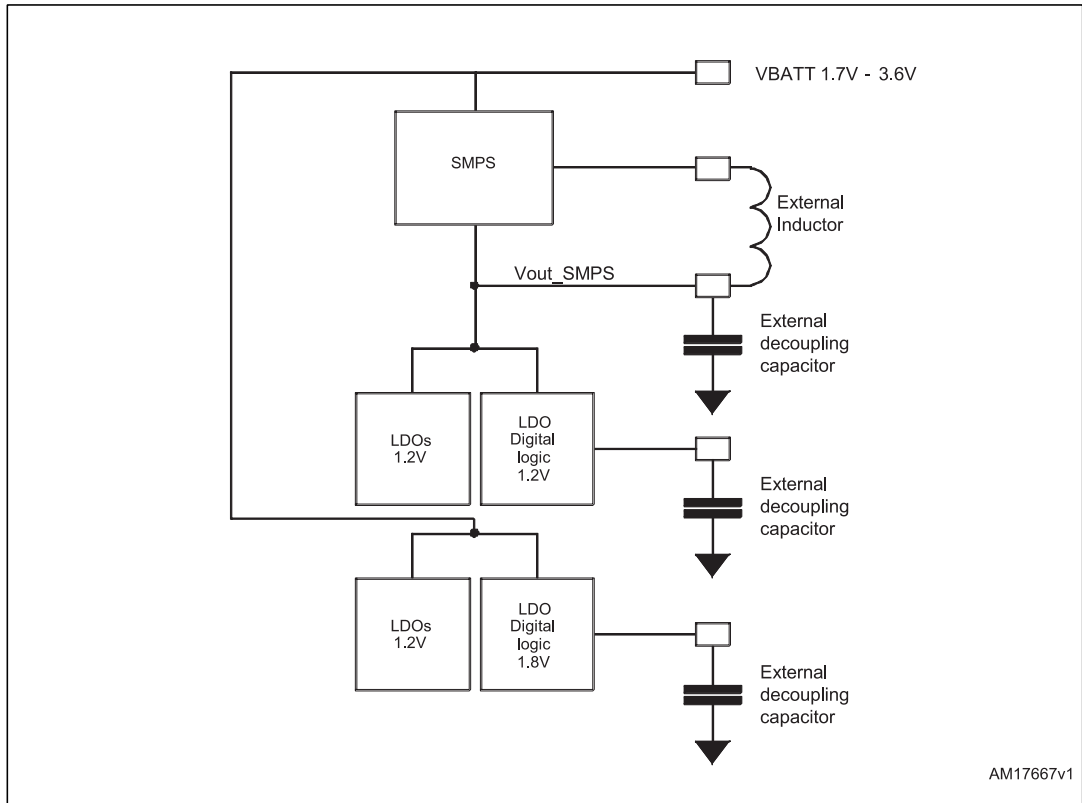


Figure 11: Power management strategy using step-down DC-DC converter



5.3 Clock management

The device integrates two low-speed frequency oscillators (LSOSC) and two High speed (16 MHz or 32 MHz) frequency oscillators (HSOSC).

The low frequency clock is used in Low Power mode and can be supplied either by a 32.7 kHz oscillator that uses an external crystal and guarantee up to ± 50 ppm frequency tolerance, or by a ring oscillator with maximum ± 500 ppm frequency tolerance, which does not require any external components.

The primary high frequency clock is a 16 MHz or 32 MHz crystal oscillator. There is also a fast-starting 12 MHz ring oscillator that provides the clock while the crystal oscillator is starting up. Frequency tolerance of high speed crystal oscillator is ± 50 ppm.

The usage of the 16 MHz (or 32 MHz) crystal is strictly necessary.

5.4 Bluetooth low energy radio

The device integrates an RF transceiver compliant with the Bluetooth specification and the standard national regulations in the unlicensed 2.4 GHz ISM band.

The RF transceiver requires very few external discrete components. It provides 96 dB link budgets with excellent link reliability, keeping the maximum peak current below 15 mA.

In Transmit mode, the power amplifier (PA) drives the signal generated by the frequency synthesizer out to the antenna terminal through a very simple external network. The power delivered as well as the harmonic content depends on the external impedance seen by the PA.

The output power is programmable from -18 dBm to +8 dBm, to allow a user-defined power control system and to guarantee optimum power consumption for each scenario.

6 Operating modes

Several operating modes are defined for the BlueNRG:

- Reset mode
- Sleep mode
- Standby mode
- Active mode
- Radio mode
 - Receive Radio mode
 - Transmit Radio mode

In Reset mode, the device is in ultra-low power consumption: all voltage regulators, clocks and the RF interface are not powered. The device enters Reset mode by asserting the external reset signal. As soon as it is de-asserted, the device follows the normal activation sequence to transit to Active mode.

In Sleep mode either the low speed crystal oscillator or the low speed ring oscillator are running, whereas the high speed oscillators are powered down as well as the RF interface. The state of the device is retained and the content of the RAM is preserved. Depending on the application, part of the RAM (RAM2 block) can be switched off during sleep to save more power (refer to stack mode 1, described in UM1868).

While in Sleep mode, the device waits until an internal timer expires and then it goes into Active mode. The transition from Sleep mode to Active mode can also be activated through the SPI interface.

Standby mode and Sleep mode are equivalent but the low speed frequency oscillators are powered down. In Standby mode the device can be activated through the SPI interface.

In Active mode the device is fully operational: all interfaces, including SPI and RF, are active as well as all internal power supplies together with the high speed frequency oscillator. The MCU core is also running.

Radio mode differs from Active mode as also the RF transceiver is active and it is capable of either transmitting or receiving.

Figure 12: "Simplified state machine" reports the simplified state machine:

Figure 12: Simplified state machine

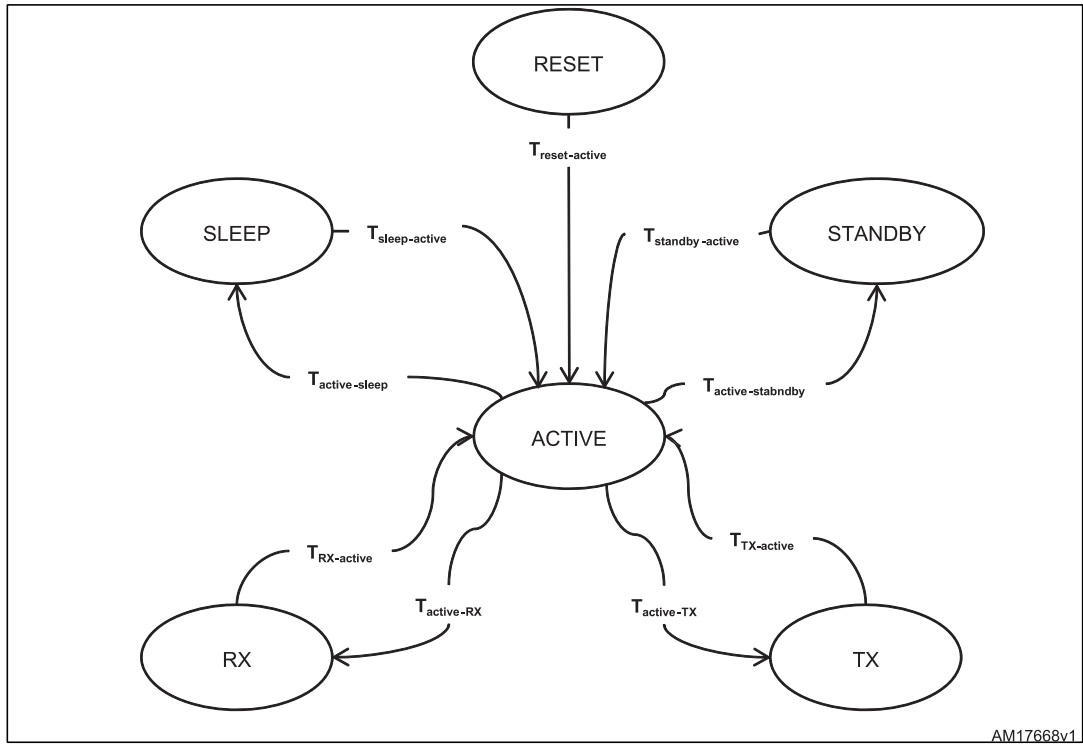


Table 5: Operating modes

| State | Digital LDO | SPI | LSOSC | HSOSC | Core | RF synt. | RX chain | TX chain |
|---------|----------------------------------|-----|-------|-------|------|----------|----------|----------|
| Reset | OFF Register contents lost | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| Standby | ON Register contents retained | ON | OFF | OFF | OFF | OFF | OFF | OFF |
| Sleep | ON Register contents retained | ON | ON | OFF | OFF | OFF | OFF | OFF |
| Active | ON Register contents retained | ON | - | ON | ON | OFF | OFF | OFF |
| RX | ON Register contents retained | ON | - | ON | ON | ON | ON | OFF |
| TX | ON Register contents retained | ON | - | ON | ON | ON | OFF | ON |

Table 6: Transition times

| Transition | Maximum time | Condition |
|-------------------------------|--------------|----------------------|
| Reset-active ⁽¹⁾ | 1.5 ms | 32 kHz not available |
| | 7 ms | 32 kHz RO |
| | 94 ms | 32 kHz XO |
| Standby-active ⁽¹⁾ | 0.42 ms | 32 kHz not available |
| | 6.2 ms | 32 kHz RO |
| | 93 ms | 32 kHz XO |
| Sleep-active ⁽¹⁾ | 0.42 ms | |
| Active-RX | 125 μ s | Channel change |
| | 61 μ s | No channel change |
| Active-TX | 131 μ s | Channel change |
| | 67 μ s | No channel change |
| RX-TX or TX-RX | 150 μ s | |

Notes:

⁽¹⁾These measurements are taken using NX3225SA-16.000 MHz-EXS00A-CS05997.

7 Application controller interface

The application controller interface (ACI) is based on a standard SPI module with speeds up to 8 MHz. The ACI defines a protocol providing access to all the services offered by the layers of the embedded Bluetooth stack. The ACI commands are described in the associated document on ACI command interface (UM1755). In addition, the ACI provides a set of commands that allow to program BlueNRG firmware from an external device connected to SPI. The complete description of updater commands and procedures is provided in a separate application note (AN4491).

8 Absolute maximum ratings and thermal data

Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referred to GND.

Table 7: Absolute maximum ratings

| Pin | Parameter | Value | Unit |
|--|---|--------------|------|
| 5, 19, 24, 26, 28 | DC-DC converter supply voltage input and output | -0.3 to +3.9 | V |
| 12, 29 | DC voltage on linear voltage regulator | -0.3 to +3.9 | V |
| 1, 2, 3, 4, 6, 7, 8, 9, 10, 11, 25, 27, 30, 31, 32 | DC voltage on digital input/output pins | -0.3 to +3.9 | V |
| 13, 14, 15, 16 | DC voltage on analog pins | -0.3 to +3.9 | V |
| 17, 18, 22, 23 | DC voltage on XTAL pins | -0.3 to +1.4 | V |
| 20, 21 ⁽¹⁾ | DC voltage on RF pins | -0.3 to +1.4 | V |
| T _{STG} | Storage temperature range | -40 to +125 | °C |
| V _{ESD-HBM} | Electrostatic discharge voltage | ±2.0 | kV |

Notes:

⁽¹⁾+8 dBm input power at antenna connector in Standard mode, +11 dBm in High Power mode, with given reference design.

Table 8: Thermal data

| Symbol | Parameter | Value | Unit |
|----------------------|-------------------------------------|-----------------------------|------|
| R _{thj-amb} | Thermal resistance junction-ambient | 34 (QFN32) 50 (WLCSP36) | °C/W |
| R _{thj-c} | Thermal resistance junction-case | 2.5 (QFN32) 25 (WLCSP36) | °C/W |

9 General characteristics

Table 9: Recommended operating conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------|-------------------------------------|------|------|------|------|
| V _{BAT} | Operating Battery supply voltage | 2.0 | | 3.6 | V |
| T _A | Operating Ambient temperature range | -40 | | +85 | °C |

10 Electrical specification

10.1 Electrical characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to $T_A = 25\text{ }^\circ\text{C}$, $V_{BAT} = 3.0\text{ V}$. All performance data are referred to a 50 W antenna connector, via reference design, QFN32 package version.

Table 10: Electrical characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit | |
|--|----------------|--------------------|-------------------------|------|------|------|---------------|
| Power consumption when DC-DC converter active | | | | | | | |
| I_{BAT} | Supply current | Reset | | 5 | | nA | |
| | | Standby | RAM2 OFF | | 1.3 | | μA |
| | | | RAM2 ON | | 2 | | |
| | | Sleep | 32 kHz XO ON (RAM2 OFF) | | 1.7 | | μA |
| | | | 32 kHz XO ON (RAM2 ON) | | 2.4 | | |
| | | | 32 kHz RO ON (RAM2 OFF) | | 2.8 | | |
| | | | 32 kHz RO ON (RAM2 ON) | | 3.5 | | |
| | | Active | CPU, Flash and RAM off | | 2 | | mA |
| | | | CPU, Flash and RAM on | | 3.3 | | |
| | | RX | High Power mode | | 7.7 | | mA |
| | | | Standard mode | | 7.3 | | |
| | | TX Standard mode | +5 dBm | | 11 | | mA |
| | | | 0 dBm | | 8.2 | | |
| | | | -2 dBm | | 7.2 | | |
| | | | -6 dBm | | 6.7 | | |
| | | | -9 dBm | | 6.3 | | |
| | | | -12 dBm | | 6.1 | | |
| | | | -15 dBm | | 5.9 | | |
| | | TX High Power mode | +8 dBm | | 15.1 | | mA |
| | | | +4 dBm | | 10.9 | | |
| +2 dBm | | | 9 | | | | |
| -2 dBm | | | 8.3 | | | | |
| -5 dBm | | | 7.7 | | | | |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit | |
|--|----------------------|-------------------------------|-------------------------|------|------|------|---------|
| | | -8 dBm | | 7.1 | | | |
| | | -11 dBm | | 6.8 | | | |
| | | -14 dBm | | 6.6 | | | |
| Power consumption when DC-DC converter not active | | | | | | | |
| I_{BAT} | Supply current | Reset | | 5 | | nA | |
| | | Standby | RAM2 OFF | | 1.4 | | μ A |
| | | | RAM2 ON | | 2 | | |
| | | Sleep | 32 kHz XO ON (RAM2 OFF) | | 1.7 | | μ A |
| | | | 32kHz XO ON (RAM2 ON) | | 2.4 | | |
| | | | 32 kHz RO ON (RAM2 OFF) | | 2.8 | | |
| | | | 32 kHz RO ON (RAM2 ON) | | 3.5 | | |
| | | Active CPU, Flash and RAM off | | 2.3 | | mA | |
| | | RX | High Power mode | | 14.5 | | mA |
| | | | Standard mode | | 14.3 | | |
| | | TX Standard mode | +5 dBm | | 21 | | mA |
| | | | 0 dBm | | 15.4 | | |
| | | | -2 dBm | | 13.3 | | |
| | | | -6 dBm | | 12.2 | | |
| | | | -9 dB | | 11.5 | | |
| | | | -12 dBm | | 11 | | |
| | | | -15 dBm | | 10.6 | | |
| | | -18 dBm | | 10.4 | | | |
| | | TX High Power mode | +8 dBm | | 28.8 | | mA |
| | | | +4 dBm | | 20.5 | | |
| +2 dBm | | | 17.2 | | | | |
| -2 dBm | | | 15.3 | | | | |
| -5 dBm | | | 14 | | | | |
| -8 dBm | | | 13 | | | | |
| -11 dBm | | | 12.3 | | | | |
| -14 dBm | | 12 | | | | | |
| Digital I/O | | | | | | | |
| C_{IN} | Port I/O capacitance | | 1.29 | 1.38 | 1.67 | pF | |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------|---------------------------------------|--------------------------------|------|------|------|------|
| T _{RISE} | Rise time | 0.1*VDD to 0.9*VDD, CL = 50 pF | 5 | | 19 | ns |
| T _{FALL} | Fall time | 0.9*VDD to 0.1*VDD, CL = 50 pF | 6 | | 22 | ns |
| T(RST) | Hold time for reset | | 1.5 | | | ms |
| TC | V _{BAT} range | | 3.0 | 3.3 | 3.6 | V |
| TC1 | V _{BAT} range | | 2.25 | 2.5 | 2.75 | V |
| VIL | Input low voltage | V _{BAT} range: TC | -0.3 | | 0.8 | V |
| | | V _{BAT} range: TC1 | -0.3 | | 0.7 | |
| VIH | Input high voltage | V _{BAT} range: TC | 2.0 | | 3.6 | V |
| | | V _{BAT} range: TC1 | 1.7 | | 3.6 | |
| VOL | Output low voltage | V _{BAT} range: TC | | | 0.4 | V |
| | | V _{BAT} range: TC1 | | | 0.7 | |
| VOH | Output high voltage | V _{BAT} range: TC | 2.4 | | | V |
| | | V _{BAT} range: TC1 | 1.7 | | | |
| IOL | Low level output current @ VOL (max.) | V _{BAT} range: TC | 3.4 | 5.6 | 7.9 | mA |
| | | V _{BAT} range: TC1 | 3.8 | 6.6 | 10.1 | |
| IOH | High level output current @ VOH (min) | V _{BAT} range: TC | 5.5 | 10.6 | 17.6 | mA |
| | | V _{BAT} range: TC1 | 3.7 | 7.2 | 12.0 | |

10.2 RF general characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to T_A = 25 °C, V_{BAT} = 3.0 V. All performance data are referred to a 50 W antenna connector, via reference design, QFN32 package version.

Table 11: RF general characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------|-----------------------------|-----------------|------|------|--------|------|
| FREQ | Frequency range | | 2400 | | 2483.5 | MHz |
| F _{CH} | Channel spacing | | | 2 | | MHz |
| RF _{ch} | RF channel center frequency | | 2402 | | 2480 | MHz |

10.3 RF transmitter characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to $T_A = 25\text{ }^\circ\text{C}$, $V_{BAT} = 3.0\text{ V}$. All performance data are referred to a 50 W antenna connector, via reference design, QFN32 package version.

Table 12: RF Transmitter characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------------------|--|--|------|--------------|-----------|-------------|
| MOD | Modulation scheme | | GFSK | | | |
| BT | Bandwidth-bit period product | | | 0.5 | | |
| M_{index} | Modulation index | | 0.45 | 0.5 | 0.55 | |
| DR | Air data rate | | | 1 | | Mbps |
| ST_{acc} | Symbol time accuracy | | | | 50 | ppm |
| P_{MAX} | Maximum output power at antenna connector | High power | | +8 | +10 | dBm |
| | | Standard mode | | +5 | +7 | dBm |
| P_{RFC} | Minimum output power | High power | | -15 | | dB |
| | | Standard mode | | -18 | | dB |
| P_{RFC} | RF power accuracy | | | | ± 2 | dB |
| P_{BW1M} | 6 dB bandwidth for modulated carrier (1 Mbps) | Using resolution bandwidth of 100 kHz | 500 | | | kHz |
| P_{RF1} | 1 st adjacent channel transmit power 2 MHz | Using resolution bandwidth of 100 kHz and average detector | | | -20 | dBm |
| P_{RF2} | 2 nd adjacent channel transmit power >3 MHz | Using resolution bandwidth of 100 kHz and average detector | | | -30 | dBm |
| P_{SPUR} | Spurious emission | Harmonics included. Using resolution bandwidth of 1 MHz and average detector | | | -41 | dBm |
| CF_{dev} | Center frequency deviation | During the packet and including both initial frequency offset and drift | | | ± 150 | kHz |
| Freq _{drift} | Frequency drift | During the packet | | | ± 50 | kHz |
| IFreq _{drift} | Initial carrier frequency drift | | | | ± 20 | kHz |
| DriftRate _{max} | Maximum drift rate | | | | 400 | Hz/ μ s |
| Z_{LOAD} | Optimum differential load | Standard mode @ 2440 MHz | | 25.9 + j44.4 | | Ω |
| | | High power mode @ 2440 MHz | | 25.4 + j20.8 | | |

10.4 RF receiver characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to $T_A = 25\text{ }^\circ\text{C}$, $V_{BAT} = 3.0\text{ V}$. All performance data are referred to a 50 W antenna connector, via reference design, QFN32 package version.

Table 13: RF receiver characteristics

| Symbol | Parameter | Test conditions | | Min. | Typ. | Max. | Unit |
|--|---|---|-----------------|--------------------|--------------------|------|----------|
| RXSENS | Sensitivity | BER <0.1% | | - | -88 | | dBm |
| P _{SAT} | Saturation | BER <0.1% | Standard mode | | 8 | | dBm |
| | | | High power mode | | 11 | | |
| Z _{IN} | Input differential impedance | Standard mode @ 2440 MHz | | | 31.4 - j26.6 | | Ω |
| | | High power mode @ 2440 MHz | | 28.8 - j18.5 | | | |
| RF selectivity with BLE equal modulation on interfering signal | | | | | | | |
| C/I _{co-channel} | Co-channel interference | Wanted signal=-67dBm, BER ≤ 0.1% | | - | 9 | | dBc |
| C/I _{1 MHz} | Adjacent (+1 MHz) interference | Wanted signal = -67dBm, BER ≤ 0.1% | | | 2 | | dBc |
| C/I _{2 MHz} | Adjacent (+2 MHz) interference | Wanted signal = -67 dBm, BER ≤ 0.1% | | | -34 | | dBc |
| C/I _{3 MHz} | Adjacent (+3 MHz) interference | Wanted signal=-67dBm, BER ≤ 0.1% | | | -40 | | dBc |
| C/I _{≥4 MHz} | Adjacent (≥ ±4 MHz) interference | Wanted signal = -67dBm, BER ≤ 0.1% | | | -34 | | dBc |
| C/I _{≥6 MHz} | Adjacent (≥ ±6 MHz) interference | Wanted signal = -67dBm BER ≤ 0.1% | | | -45 | | dBc |
| C/I _{≥25 MHz} | Adjacent (≥ ±25 MHz) interference | Wanted signal=-67 dBm, BER ≤ 0.1% | | | -64 | | dBc |
| C/I _{Image} | Image frequency Interference -2 MHz | Wanted signal=-67 dBm, BER ≤ 0.1% | | | -20 | | dBc |
| C/I _{Image±1 MHz} | Adjacent (±1 MHz) Interference to in-band image frequency | Wanted signal=-67dBm, BER ≤ 0.1% | -1MHz | | 5 | | dBc |
| | | | -3MHz | -25 | | | |
| Out of Band blocking (interfering signal CW) | | | | | | | |
| C/I _{Block} | Interfering signal frequency 30 MHz – 2000 MHz | Wanted signal=-67dBm, BER ≤ 0.1%, measurement resolution 10 MHz | | - | | -30 | dBm |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|--|---|------|------|------|------|
| C/I _{Block} | Interfering signal frequency 2003 MHz – 2399 MHz | Wanted signal = -67 dBm, BER ≤ 0.1%, measurement resolution 3 MHz | | | -35 | dBm |
| C/I _{Block} | Interfering signal frequency 2484 MHz – 2997 MHz | Wanted signal = -67 dBm, BER ≤ 0.1%, measurement resolution 3 MHz | | | -35 | dBm |
| C/I _{Block} | Interfering signal frequency 3000 MHz – 12.75 GHz | Wanted signal=-67dBm, BER ≤ 0.1%, measurement resolution 25 MHz | | | -30 | dBm |
| Intermodulation characteristics (CW signal at f ₁ , BLE interfering signal at f ₂) | | | | | | |
| P _{IM(3)} | Input power of IM interferes at 3 and 6 MHz distance from wanted signal | Wanted signal = -64 dBm, BER ≤ 0.1% | | | -33 | dBm |
| P _{IM(-3)} | Input power of IM interferes at -3 and -6 MHz distance from wanted signal | Wanted signal = -64 dBm, BER ≤ 0.1% | | | -43 | dBm |
| P _{IM(4)} | Input power of IM interferes at ±4 and ±8 MHz distance from wanted signal | Wanted signal=-64dBm, BER ≤ 0.1% | | | -33 | dBm |
| P _{IM(5)} | Input power of IM interferes at ±5 and ±10 MHz distance from wanted signal | Wanted signal = -64 dBm, BER ≤ 0.1% | | | -33 | dBm |

10.5 High speed crystal oscillator (HSXOSC) characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to T_A = 25 °C, V_{BAT} = 3.0 V.

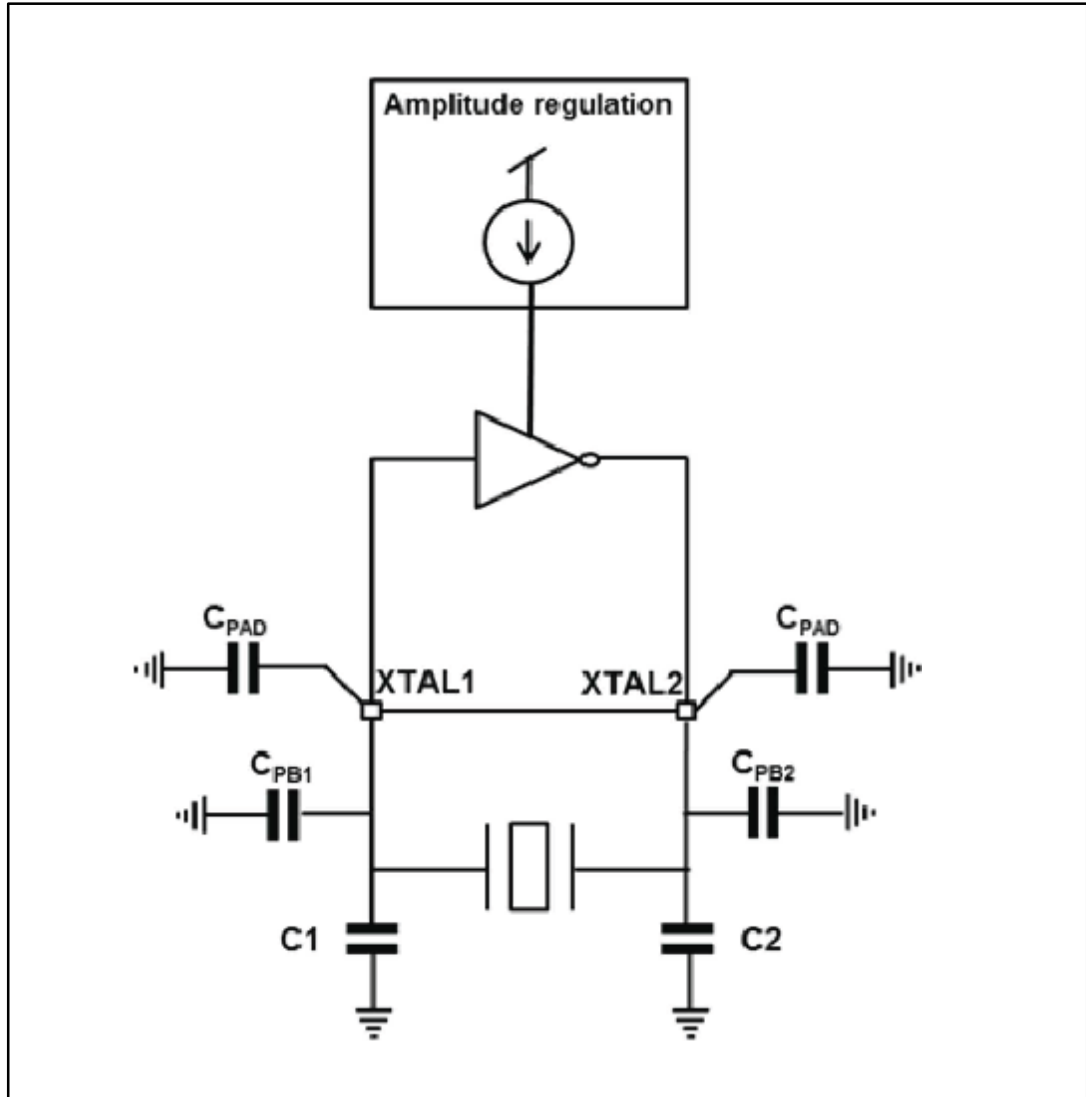
Table 14: High speed crystal oscillator characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------|------------------------------|---|------|-------|------|------|
| f _{NOM} | Nominal frequency | | | 16/32 | | MHz |
| f _{TOL} | Frequency tolerance | Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance. | | | ±50 | ppm |
| ESR | Equivalent series resistance | | | | 100 | Ω |
| P _d | Drive level | | | | 100 | μW |

10.5.1 High speed crystal oscillator (HSXOSC)

The device includes a fully integrated, low power 16/32 MHz Xtal oscillator with an embedded amplitude regulation loop. In order to achieve low power operation and good frequency stability of the Xtal oscillator, certain considerations with respect to the quartz load capacitance C_0 need to be taken into account. [Figure 13: "Simplified block diagram of the amplitude regulated oscillator"](#) shows a simplified block diagram of the amplitude regulated oscillator used on the device.

Figure 13: Simplified block diagram of the amplitude regulated oscillator



Low power consumption and fast startup time is achieved by choosing a quartz crystal with a low load capacitance C_0 . To achieve good frequency stability, the following equation needs to be satisfied:

Equation 1

$$C_0 = \frac{C'_1 * C'_2}{C'_1 + C'_2}$$

Where $C1' = C1 + CPCB1 + CPAD$, $C2' = C2 + CPCB2 + CPAD$, where $C1$ and $C2$ are external (SMD) components, $CPCB1$ and $CPCB2$ are PCB routing parasites and $CPAD$ is the equivalent small-signal pad-capacitance. The value of $CPAD$ is around 0.5 pF for each pad. The routing parasites should be minimized by placing quartz and $C1/C2$ capacitors close to the chip, not only for an easier matching of the load capacitance $C0$, but also to ensure robustness against noise injection. Connect each capacitor of the Xtal oscillator to ground by a separate via.

10.6 Low speed crystal oscillator (LSXOSC) characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to $T_A = 25\text{ }^\circ\text{C}$, $V_{BAT} = 3.0\text{ V}$.

Table 15: Low speed crystal oscillator characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|---|------|--------|------|------|
| f_{NOM} | Nominal frequency | | | 32.768 | | kHz |
| f_{TOL} | Frequency tolerance | Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance. | | | ±50 | ppm |
| ESR | Equivalent series resistance | | | | 90 | kΩ |
| P_D | Drive level | | | | 0.1 | μW |

Note: These values are the correct ones for NX3215SA-32.768 kHz-EXS00A-MU00003.

10.7 High speed ring oscillator (HSROSC) characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to $T_A = 25\text{ }^\circ\text{C}$, $V_{BAT} = 3.0\text{ V}$, QFN32 package version.

Table 16: High speed ring oscillator characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------|-------------------|-----------------|------|------|------|------|
| f_{NOM} | Nominal frequency | | | 12 | 16 | MHz |

10.8 Low speed ring oscillator (LSROSC) characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to $T_A = 25\text{ }^\circ\text{C}$, $V_{BAT} = 3.0\text{ V}$, QFN32 package version.

Table 17: Low speed ring oscillator characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------------------|---------------------|-----------------|------|------|------|------|
| 32 kHz ring oscillator (LSROSC) | | | | | | |
| f_{NOM} | Nominal frequency | | | 37.4 | | kHz |
| f_{TOL} | Frequency tolerance | | | | ±500 | ppm |

10.9 N-fractional frequency synthesizer characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to $T_A = 25\text{ }^\circ\text{C}$, $V_{BAT} = 3.0\text{ V}$, $f_c = 2440\text{ MHz}$.

Table 18: N-fractional frequency synthesizer characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------|------------------------|---|------|------|---------------|---------------|
| PN _{SYNTH} | RF carrier phase noise | At $\pm 1\text{MHz}$ offset from carrier | | -113 | | dBc/Hz |
| | | At $\pm 3\text{MHz}$ offset from carrier | | -119 | | dBc/Hz |
| | | At $\pm 6\text{MHz}$ offset from carrier | | TBD | | dBc/Hz |
| | | At $\pm 25\text{MHz}$ offset from carrier | | TBD | | dBc/Hz |
| LOCK _{TIME} | PLL lock time | | | 40 | μs | |
| TO _{TIME} | PLL turn on / hop time | Including calibration | | | 150 | μs |

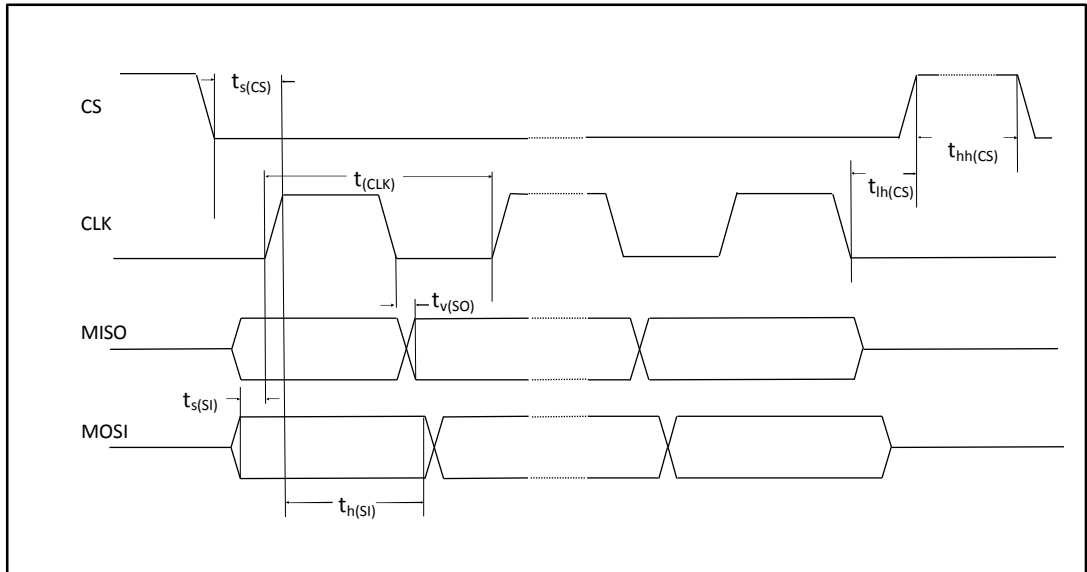
10.10 SPI characteristics

Table 19: SPI characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------------|----------------------|---------------|------|------|------|
| $f_{CLK1}/t_{(CLK)}$ | SPI clock frequency | | | 8 | MHz |
| DuCy _(CLK) | SPI clock duty cycle | | 50 | | % |
| $t_{s(CS)}$ | CS setup time | 40 | | | ns |
| $t_{lh(CS)}$ | CS low hold time | 40 | | | |
| $t_{hh(CS)}$ | CS high hold time | $10t_{(CLK)}$ | | | |
| $t_{s(SI)}$ | MOSI setup time | 20 | | | |
| $t_{h(SI)}$ | MOSI hold time | 10 | | | |
| $t_{v(SO)}$ | MISO valid time | | | 40 | |

The values for the parameters given in this table are based on characterization, not tested in production.

Figure 14: SPI timings



11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

11.1 QFN32 package information

Figure 15: QFN32 (5 x 5 x 1 pitch 0.5 mm) package outline

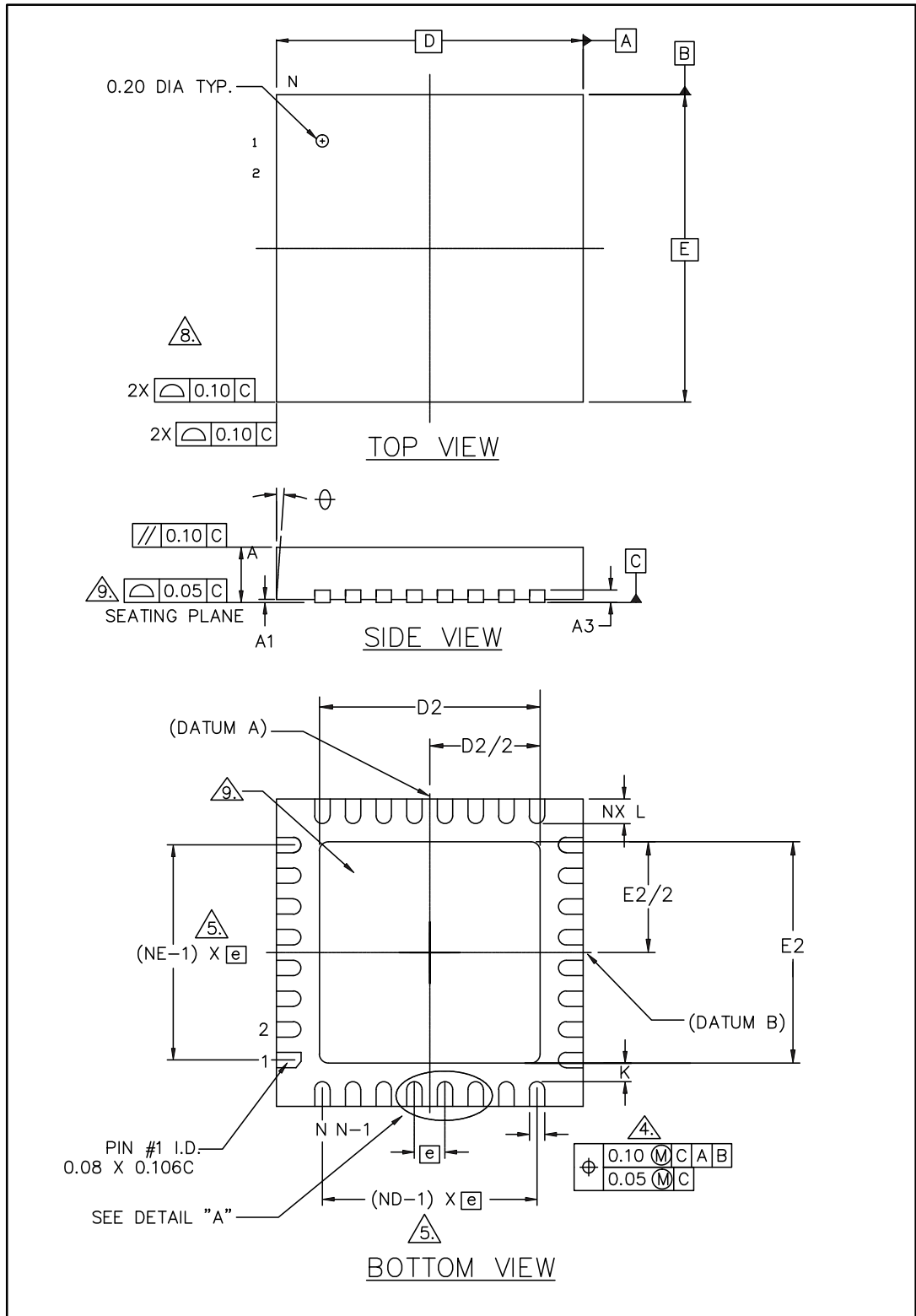
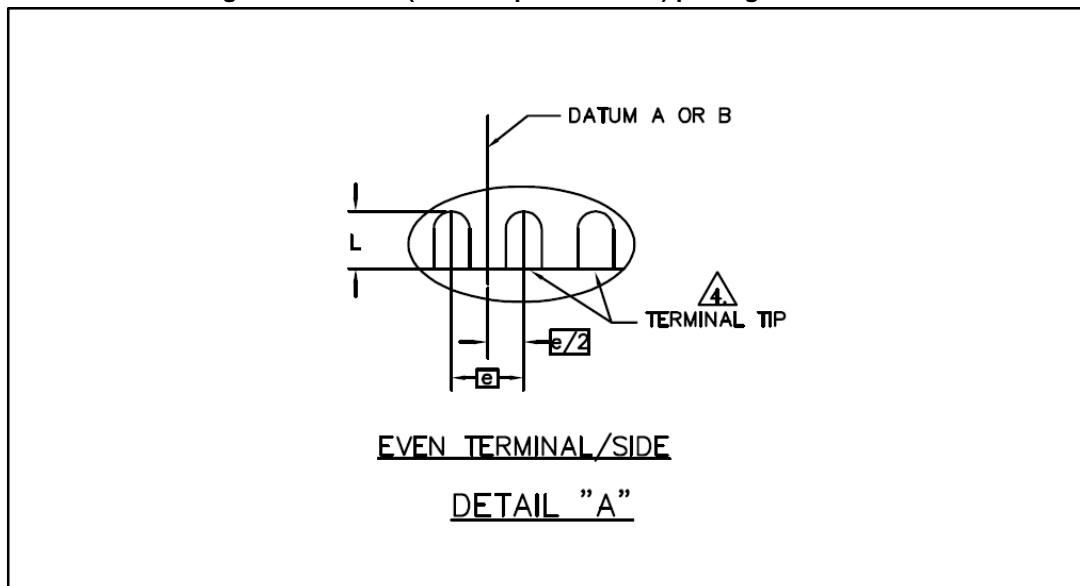


Table 20: QFN32 (5 x 5 x 1 pitch 0.5 mm) mechanical data

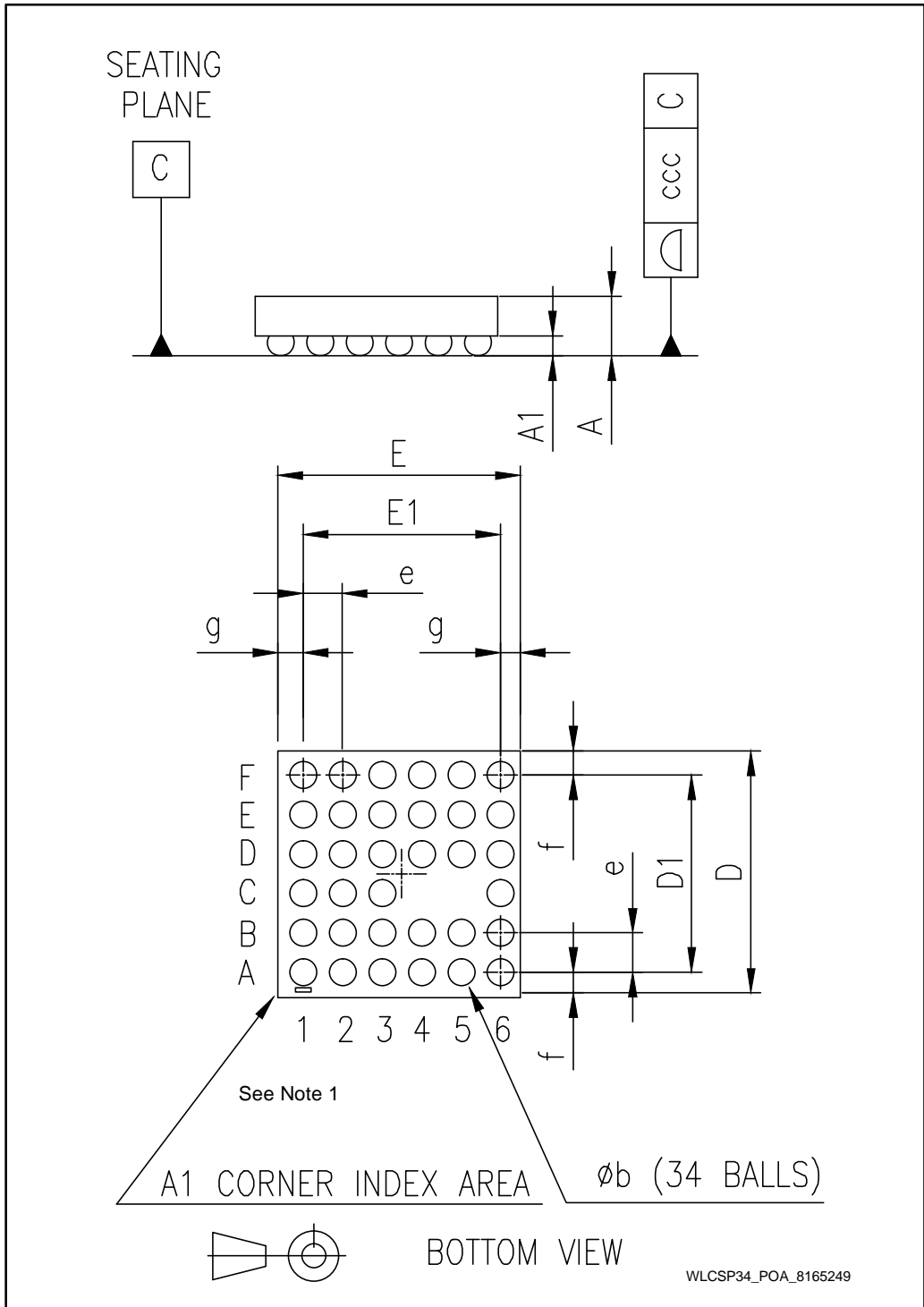
| Dim. | mm | | |
|--------|----------|------|------|
| | Min. | Typ. | Max. |
| A | 0.80 | 0.85 | 1.00 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.25 | 0.25 | 0.30 |
| D | 5.00 BSC | | |
| E | 5.00 BSC | | |
| D2 | 3.2 | | 3.70 |
| E2 | 3.2 | | 3.70 |
| e | 0.5 BSC | | |
| L | 0.30 | 0.40 | 0.50 |
| Φ | 0° | | 14° |
| K | 0.20 | | |

Figure 16: QFN32 (5 x 5 x 1 pitch 0.5 mm) package detail "A"



11.2 WLCSP34 package information

Figure 17: WLCSP34 (2.66 x 2.56 x 0.5 pitch 0.4 mm) package outline



1. The corner of terminal A1 must be identified on the top surface by using a laser marking dot.

Table 21: WLCSP34 (2.66 x 2.56 x 0.5 pitch 0.4 mm) mechanical data

| Dim. | mm. | | | Notes |
|------|------|------|------|-------|
| | Min. | Typ. | Max. | |
| A | | | 0.50 | |
| A1 | | 0.20 | | |
| b | | 0.27 | | (1) |
| D | 2.50 | 2.56 | 2.58 | (2) |
| D1 | | 2.00 | | |
| E | 2.60 | 2.66 | 2.68 | (3) |
| E1 | | 2.00 | | |
| e | | 0.40 | | |
| f | | 0.28 | | |
| g | | 0.33 | | |
| ccc | | | 0.05 | |

Notes:

(1)The typical ball diameter before mounting is 0.25 mm.

(2) $D = f + D1 + f$.

(3) $E = g + E1 + g$.

12 PCB assembly guidelines

For Flip Chip mounting on the PCB, STMicroelectronics recommends the use of a solder stencil aperture of 330 x 330 μm maximum and a typical stencil thickness of 125 μm. Flip Chips are fully compatible with the use of near eutectic 95.8% Sn, 3.5% Ag, 0.7% Cu solder paste with no-clean flux. ST's recommendations for Flip Chip board mounting are illustrated on the soldering reflow profile shown in [Figure 18: "Flip Chip CSP \(2.66 x 2.56 x 0.5 pitch 0.4 mm\) package reflow profile recommendation"](#)

Figure 18: Flip Chip CSP (2.66 x 2.56 x 0.5 pitch 0.4 mm) package reflow profile recommendation

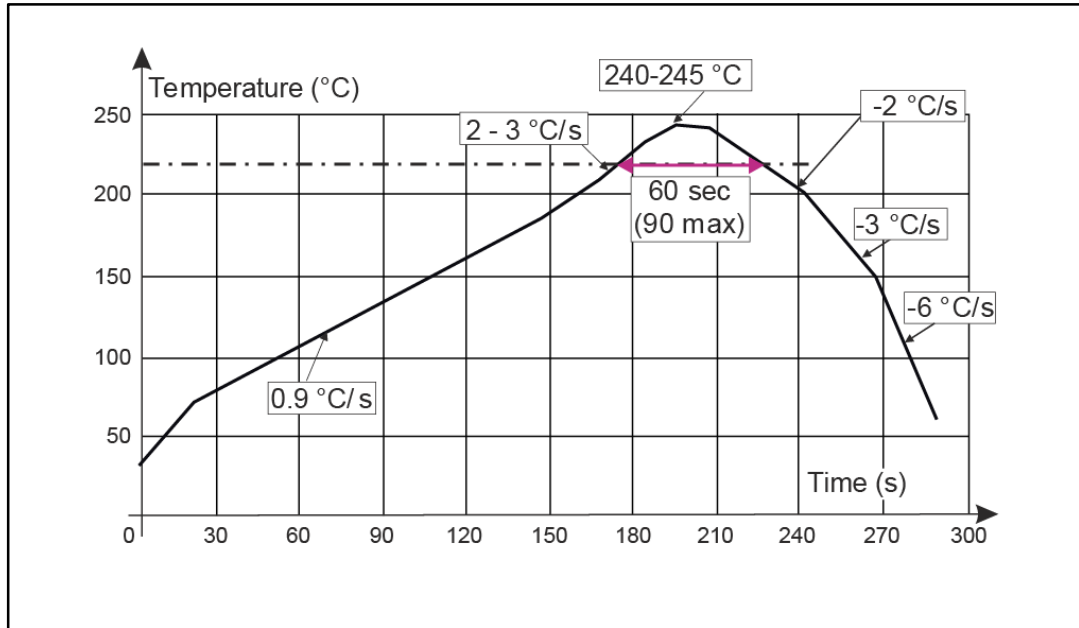


Table 22: Flip Chip CSP (2.66 x 2.56 x 0.5 pitch 0.4 mm) package reflow profile recommendation

| Profile | Value | |
|---|---------------|---------|
| | Typ. | Max. |
| Temp. gradient in preheat (T = 70 – 180 °C) | 0.9 °C/s | 3 °C/s |
| Temp. gradient (T = 200 – 225 °C) | 2 °C/s | 3 °C/s |
| Peak temp. in reflow | 240 - 245 °C | 260 °C |
| Time above 220 °C | 60 s | 90 s |
| Temp. gradient in cooling | -2 to -3 °C/s | -6 °C/s |
| Time from 50 to 220 °C | 160 to 220 s | |

Dwell time in the soldering zone (with temperature higher than 220 °C) has to be kept as short as possible to prevent component and substrate damage. Peak temperature must not exceed 260 °C. Controlled atmosphere (N₂ or N₂H₂) is recommended during the whole reflow, especially above 150 °C.

Flip Chips are able to withstand three times the previous recommended reflow profile to be compatible with a double reflow when SMDs are mounted on both sides of the PCB plus one additional repair.

A maximum of three soldering reflows are allowed for these lead-free packages (with repair step included).

The use of a no-clean paste is highly recommended to avoid any cleaning operation. To prevent any bump cracks, ultrasonic cleaning methods are not recommended.

13 Revision history

Table 23: Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 09-Aug-2013 | 1 | Initial release. |
| 07-Feb-2014 | 2 | <ul style="list-style-type: none"> • Datasheet promoted from preliminary data to production data • Added WLCSP34 package to <i>Table 1: Device summary</i> • Deleted references to "low power ADC" throughout the document. • Added pin information for the WLCSP package to <i>Figure 3: BlueNRG pinout top view (WLCSP34)</i>, <i>Table 2: Pinout description</i> • Updated <i>Figure 5: BlueNRG application circuit: active DC-DC converter QFN32 package</i> and <i>Figure 6: BlueNRG application circuit: non active DC-DC converter QFN32 package</i> • Added <i>Figure 7: BlueNRG application circuit: active DC-DC converter WLCSP package</i> and <i>Figure 8: BlueNRG application circuit: non active DC-DC converter WLCSP package</i> • Modified High Performance and Standard Mode values in <i>Table 3: External component list</i> • Changed all references the term "Slave" to "RAM2 OFF", and "Master" to "RAM2 ON" in <i>Figure 7: Electrical characteristics</i>. • Modified <i>High Performance and Standard Mode values</i> in <i>Table 3: External component list</i>. • Modified <i>Figure 9: BlueNRG block diagram</i> • Corrected error in typical BSC value for reference "e" in <i>Table 20</i>. • Added WLCSP package drawing and dimensions data (in <i>Figure 14</i> and <i>Table 21</i>). • Minor text corrections throughout the document. |
| 19-Mar-2014 | 3 | <p>Added: <i>Figure 3: Pinout top view (WLCSP34)</i></p> <p>Updated: <i>Figure 5: BlueNRG application circuit: active DC-DC converter QFN32 package</i> and <i>Figure 6: BlueNRG application circuit non active DC-DC onverter QFN32 package</i>, <i>Figure 7: BlueNRG application circuit: active DC-DC converter WLCSP package</i> and <i>Figure 8: BlueNRG application circuit: non active DC-DC converter WLCSP package</i> .</p> |
| 21-Mar-2014 | 4 | Added: <i>Section 12: PCB assembly guidelines</i> |

| Date | Revision | Changes |
|-------------|----------|---|
| 20-Nov-2014 | 5 | Updated:Bluetooth specification v4.1 compliancy, <i>Table 2: Pinout description</i> , <i>Table 3: External component list</i> , <i>Table 8: Thermal data</i> , <i>Table 14: High speed crystal oscillator characteristics</i> , <i>Table 15: Low speed crystal oscillator characteristics</i> , <i>Table 18: N-fractional frequency synthesizer characteristics</i> , <i>Section 10.7: High speed ring oscillator (HSROSC) characteristics</i> and <i>Section 5: Block diagram and descriptions</i> . Added: <i>Section 10.5.1: High speed crystal oscillator (HSXOSC)</i> |
| 13-May-2015 | 6 | Updated: <i>Features</i> section in cover page; <i>Table 2</i> , replaced reference to Bluetooth specification v4.1 with v4.0 throughout the document, <i>Figure 1: BlueNRG application block diagram</i> Minor changes throughout the document to improve readability. |
| 03-Nov-2015 | 7 | Added: <i>Section 10.10: SPI characteristics</i> |
| 16-Nov-2015 | 8 | Updated title, <i>Features</i> , <i>Description</i> and <i>General description</i> . |
| 20-Nov-2015 | 9 | Updated title, <i>Features</i> , <i>Description</i> and <i>General description</i> . |
| 28-Jan-2016 | 10 | Modified title, <i>Features</i> , <i>Description</i> , <i>General description</i> and <i>Application controller interface</i> . |

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