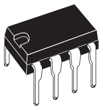
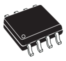
LM555 General-purpose single bipolar timers

Features

- Low turn-off time
- Maximum operating frequency greater than 500 kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- Output can source or sink up to 200 mA
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C



N
DIP8
(Plastic package)



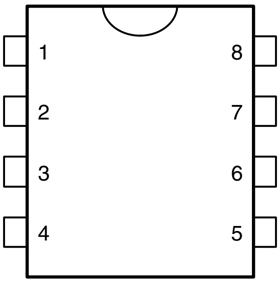
D
SO8
(Plastic micropackage)

Description

The LM555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor.

The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA.

Pin connections
(top view)



1 - GND
2 - Trigger
3 - Output
4 - Reset
5 - Control voltage
6 - Threshold
7 - Discharge
8 - V_{CC}

1 Schematic diagrams

Figure 1. Block diagram

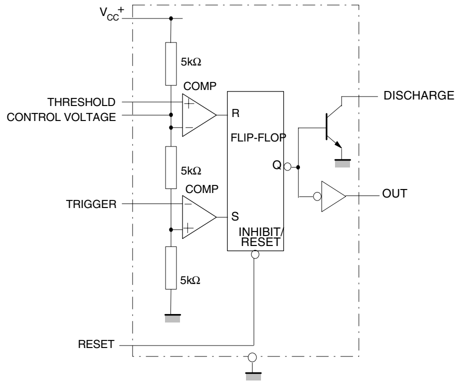
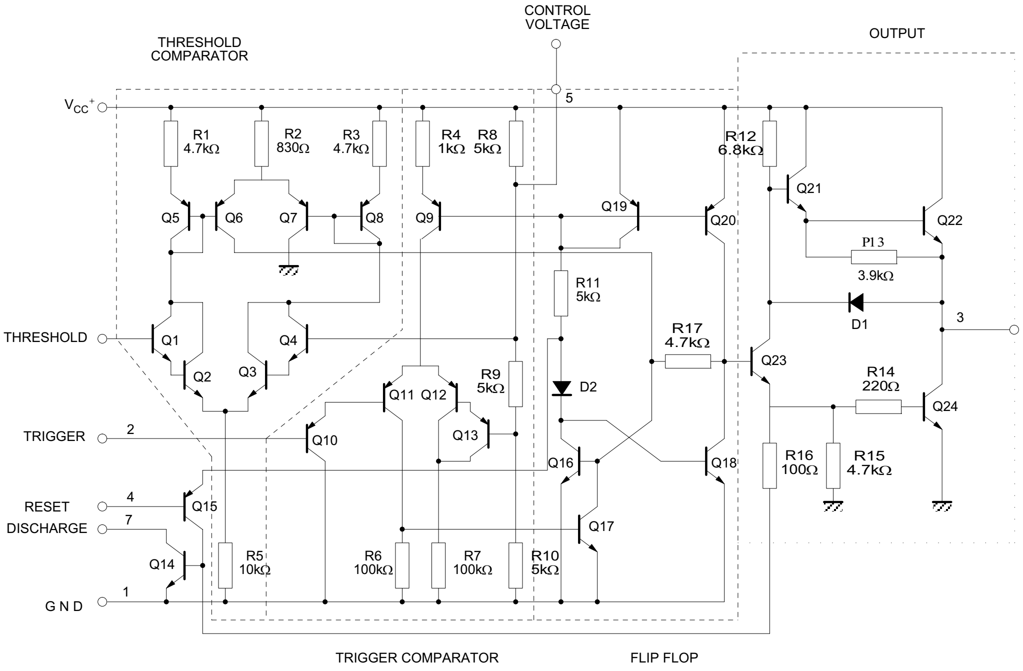


Figure 2. Schematic diagram



2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	18	V
I_{OUT}	Output current (sink & source)	±225	mA
R_{thja}	Thermal resistance junction to ambient(1) DIP8 SO-8	 85 125	°C/W
R_{thjc}	Thermal resistance junction to case (1) DIP8 SO-8	 41 40	°C/W
ESD	Human body model (HBM)(2)	1000	V
	Machine model (MM)(3)	100	
	Charged device model (CDM)(4)	1500	
	Latch-up immunity	200	mA
T_{LEAD}	Lead temperature (soldering 10 seconds)	260	°C
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature range	-65 to 150	°C

1. Short-circuits can cause excessive heating. These values are typical.
2. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
3. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
4. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage LM555	 4.5 to 16	V
V_{th}, V_{trig}, V_{cl}, V_{reset}	Maximum input voltage	V_{CC}	V
I_{OUT}	Output current (sink and source)	±200	mA
T_{oper}	Operating free air temperature range LM555	 0 to 70	°C

3 Electrical characteristics

Table 3. T_{amb} = +25° C, V_{CC} = +5 V to +15 V (unless otherwise specified)

Symbol	Parameter				LM555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CC}	Supply current ($R_L = \infty$)							mA
	Low state V_{CC} = +5V		3	5		3	6	
	V_{CC} = +15V		10	12		10	15	
	High state V_{CC} = +5V		2			2		
	Timing error (monostable)							
	(R_A = 2kΩ to 100kΩ, C = 0.1µF)							
	Initial accuracy (1)		0.5	2		1	3	%
	Drift with temperature		30	100		50		ppm/°C
	Drift with supply voltage		0.05	0.2		0.1	0.5	%/V
	Timing error (astable)							
	(R_A, R_B = 1kΩ to 100kΩ, C = 0.1µF, V_{CC} = +15V)							
	Initial accuracy (1)		1.5			2.25		%
	Drift with temperature		90			150		ppm/°C
	Drift with supply voltage		0.15			0.3		%/V
V_{CL}	Control voltage level							V
	V_{CC} = +15V	9.6	10	10.4	9	10	11	
	V_{CC} = +5V	2.9	3.33	3.8	2.6	3.33	4	
V_{th}	Threshold voltage							V
	V_{CC} = +15V	9.4	10	10.6	8.8	10	11.2	
	V_{CC} = +5V	2.7	3.33	4	2.4	3.33	4.2	
I_{th}	Threshold current (2)		0.1	0.25		0.1	0.25	µA
V_{trig}	Trigger voltage							V
	V_{CC} = +15V	4.8	5	5.2	4.5	5	5.6	
	V_{CC} = +5V	1.45	1.67	1.9	1.1	1.67	2.2	
I_{trig}	Trigger current (V_{trig} = 0V)		0.5	0.9		0.5	2.0	µA
V_{reset}	Reset voltage (3)	0.4	0.7	1	0.4	0.7	1	V
I_{reset}	Reset current							mA
	V_{reset} = +0.4V		0.1	0.4		0.1	0.4	
	V_{reset} = 0V		0.4	1		0.4	1.5	
V_{OL}	Low level output voltage							V
	V_{CC} = +15V $I_{O(sink)}$ = 10mA		0.1	0.15		0.1	0.25	
	$I_{O(sink)}$ = 50mA		0.4	0.5		0.4	0.75	
	$I_{O(sink)}$ = 100mA		2	2.2		2	2.5	
	$I_{O(sink)}$ = 200mA		2.5			2.5		
	V_{CC} = +5V $I_{O(sink)}$ = 8mA		0.1	0.25		0.3	0.4	
	$I_{O(sink)}$ = 5mA		0.05	0.2		0.25	0.35	
V_{OH}	High level output voltage							V
	V_{CC} = +15V $I_{O(sink)}$ = 200mA		12.5			12.5		
	$I_{O(sink)}$ = 100mA	13	13.3		12.75	13.3		
	V_{CC} = +5V $I_{O(sink)}$ = 100mA	3	3.3		2.75	3.3		

Table 3. T_{amb} = +25° C, V_{CC} = +5 V to +15 V (unless otherwise specified) (continued)

Symbol	Parameter				LM555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$I_{dis(off)}$	Discharge pin leakage current (output high) V_{dis} = 10V		20	100		20	100	nA
$V_{dis(sat)}$	Discharge pin saturation voltage (output low) (4) V_{CC} = +15V, I_{dis} = 15mA V_{CC} = +5V, I_{dis} = 4.5mA		180 80	480 200		180 80	480 200	mV
t_r t_f	Output rise time Output fall time		100 100	200 200		100 100	300 300	ns
t_{off}	Turn off time (5) (V_{reset} = V_{CC})		0.5			0.5		µs

1. Tested at V_{CC} = +5 V and V_{CC} = +15 V.
2. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total ($R_A + R_B$) is 20 MΩ for +15 V operation and 3.5 MΩ for +5 V operation.
3. Specified with trigger input high.
4. No protection against excessive pin 7 current is necessary, providing the package dissipation rating is not exceeded.
5. Time measured from a positive pulse (from 0 V to 0.8 x V_{CC}) on the Threshold pin to the transition from high to low on the output pin. Trigger is tied to threshold.

Figure 3. Minimum pulse width required for triggering

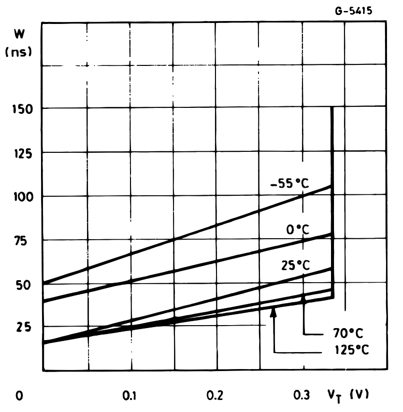


Figure 4. Supply current versus supply voltage

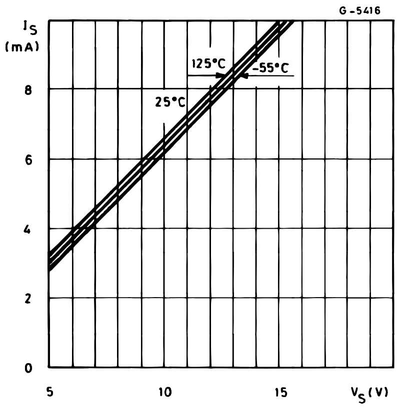


Figure 5. Delay time versus temperature

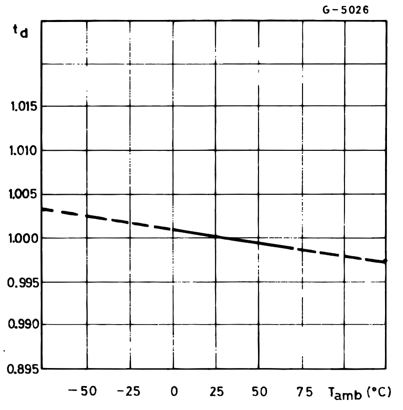


Figure 6. Low output voltage versus output sink current

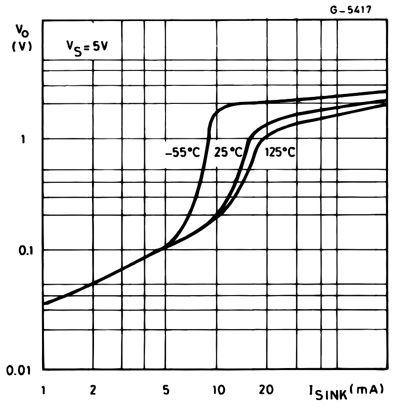


Figure 7. Low output voltage versus output sink current

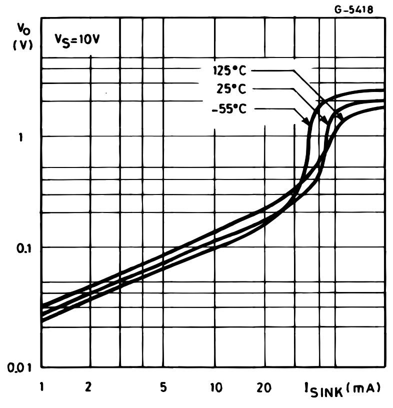


Figure 8. Low output voltage versus output sink current

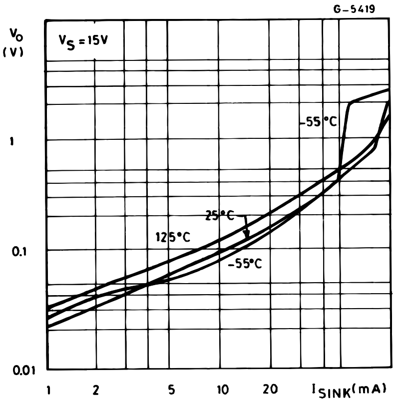


Figure 9. High output voltage drop versus output

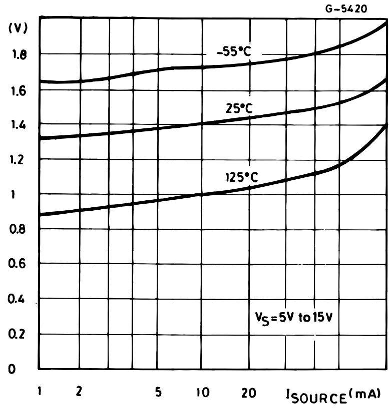


Figure 10. Delay time versus supply voltage

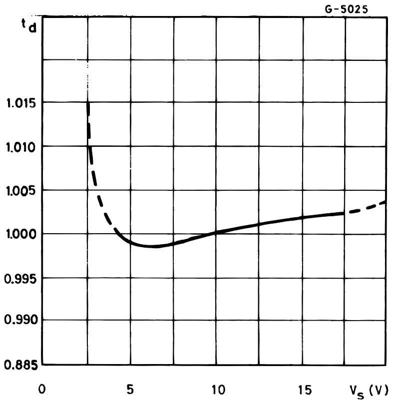
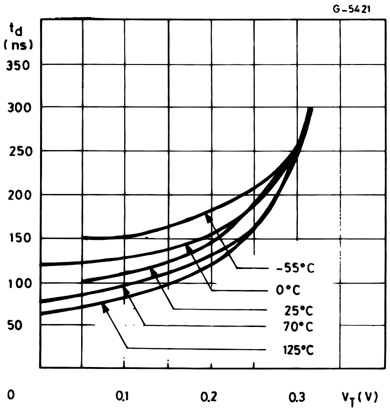


Figure 11. Propagation delay versus voltage level of trigger value

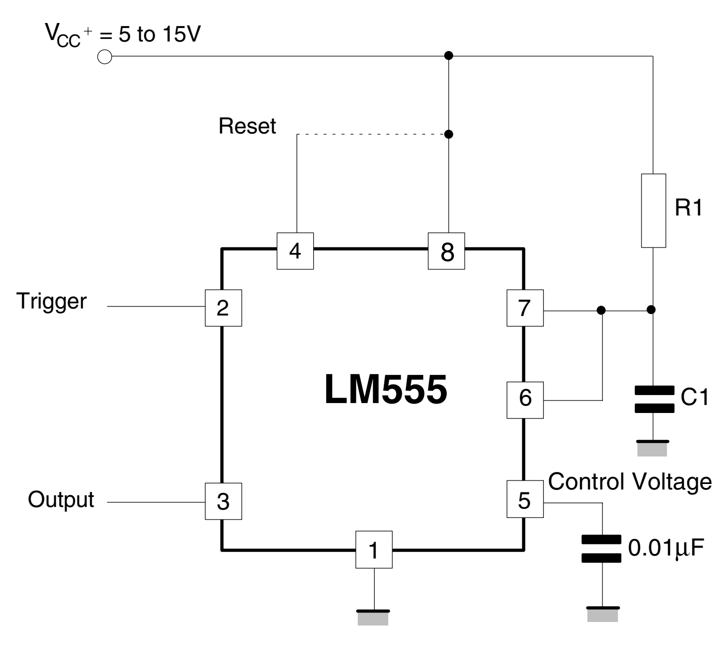


4 Application information

4.1 Monostable operation

In the monostable mode, the timer generates a single pulse. As shown in *Figure 12*, the external capacitor is initially held discharged by a transistor inside the timer.

Figure 12. Typical schematics in monostable operation



The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC}. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by $t = 1.1\ R_1C_1$ and is easily determined by *Figure 14*.

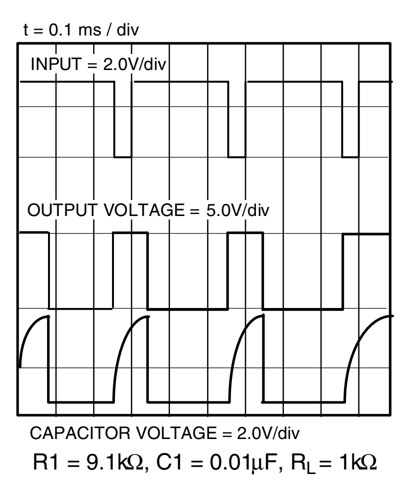
Note that because the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short-circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant $t = R_1C_1$. When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state.

Figure 13 shows the actual waveforms generated in this mode of operation.

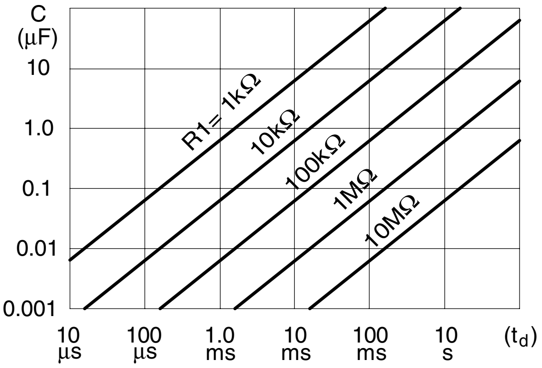
When Reset is not used, it should be tied high to avoid any possibility of unwanted triggering.

Figure 13. Waveforms in monostable operation



R1 = 9.1kΩ, C1 = 0.01µF, R_L = 1kΩ

Figure 14. Pulse duration versus R1C1



4.2 Astable operation

When the circuit is connected as shown in *Figure 15* (pins 2 and 6 connected) it triggers itself and free runs as a multi-vibrator. The external capacitor charges through R_1 and R_2 and discharges through R_2 only. Thus the duty cycle can be set accurately by adjusting the ratio of these two resistors.

In the astable mode of operation, C_1 charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times and, therefore, frequency are independent of the supply voltage.

Figure 15. Typical schematics in astable operation

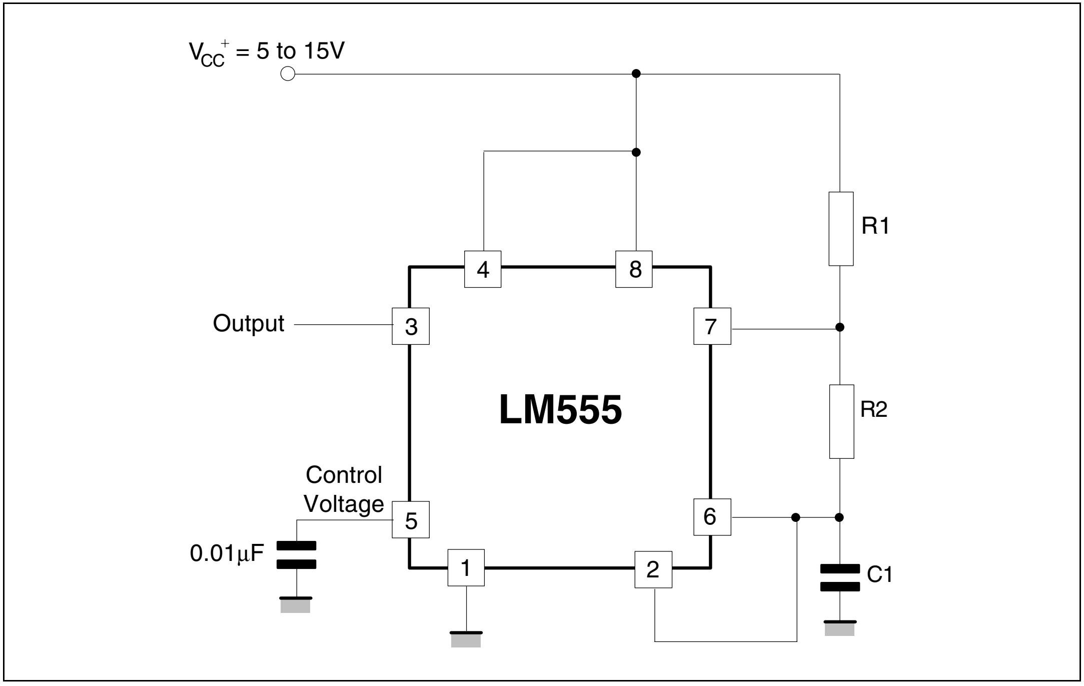


Figure 16 shows the actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by:

$t1 = 0.693\ (R_1 + R_2)\ C_1$

and the discharge time (output LOW) by:

$t2 = 0.693\ (R_2)\ C_1$

Thus the total period T is given by:

$T = t1 + t2 = 0.693\ (R1 + 2R2)\ C1$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R1 + 2R2)C1}$$

It can easily be found from *Figure 17*.

The duty cycle is given by:

$$D = \frac{R2}{R1 + 2R2}$$

Figure 16. Waveforms in astable operation

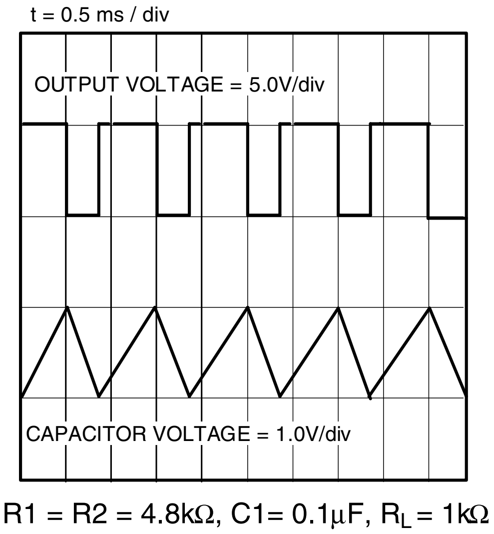
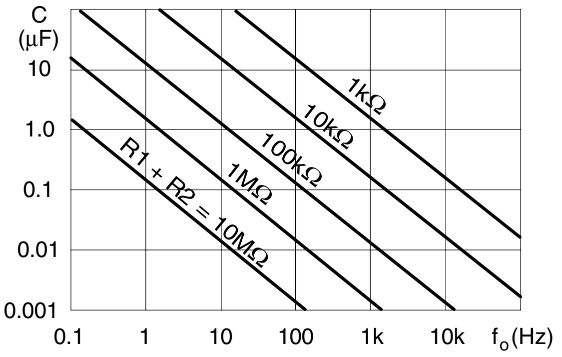


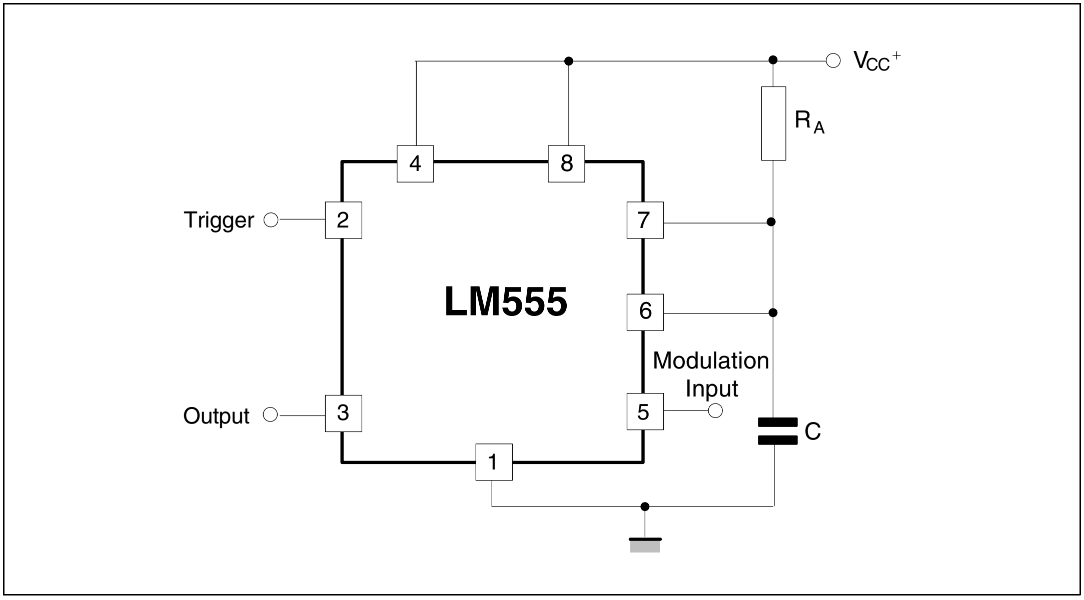
Figure 17. Free running frequency versus R_1, R_2 and C_1



4.3 Pulse width modulator

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 18* shows the circuit.

Figure 18. Pulse width modulator



4.4 Linear ramp

When the pull-up resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 19* shows a circuit configuration that will perform this function.

Figure 19. Linear ramp

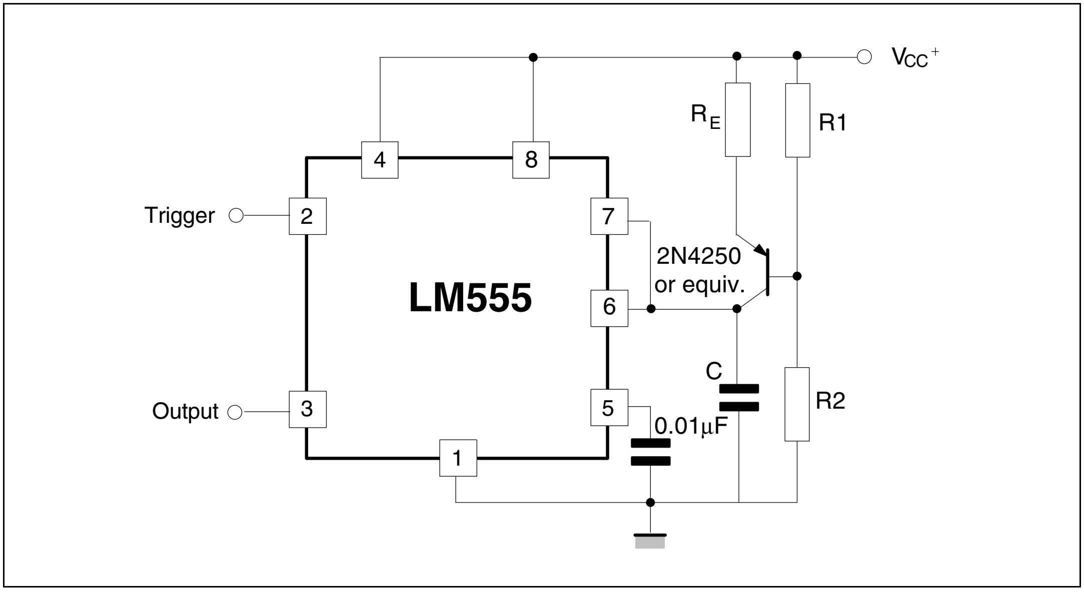
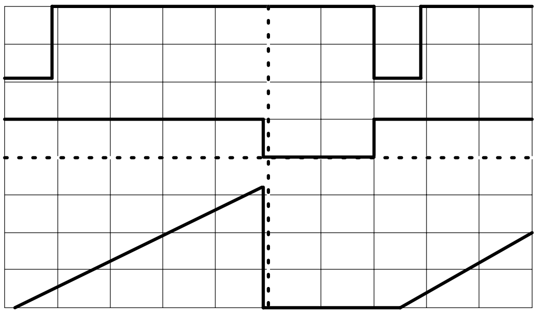


Figure 20 shows the waveforms generator by the linear ramp.

The time interval is given by:

$$T = \frac{(2/3\ Vcc\ RE\ (R1+R2)\ C}{R1\ Vcc\ -\ VBE\ (R1+R2)}\ VBE = 0.6V$$

Figure 20. Linear ramp



$V_{CC} = 5$ V
Time:
20 µs/DIV
$R_1 + 47$ kΩ
$R_2 = 100$ kΩ
$R_E = 2.7$ kΩ
C = 0.01 µF

Top trace: input 3 V/DIV
Middle trace: output 5 V/DIV
Bottom trace: output 5 V/DIV
Bottom trace: capacitor voltage 1 V/DIV

4.5 50% duty cycle oscillator

For a 50% duty cycle, the resistors R_A and R_B can be connected as in *Figure 21*. The time period for the output high is the same as for astable operation (see *Section 4.2 on page 9*):

$t1 = 0.693\ R_A\ C$

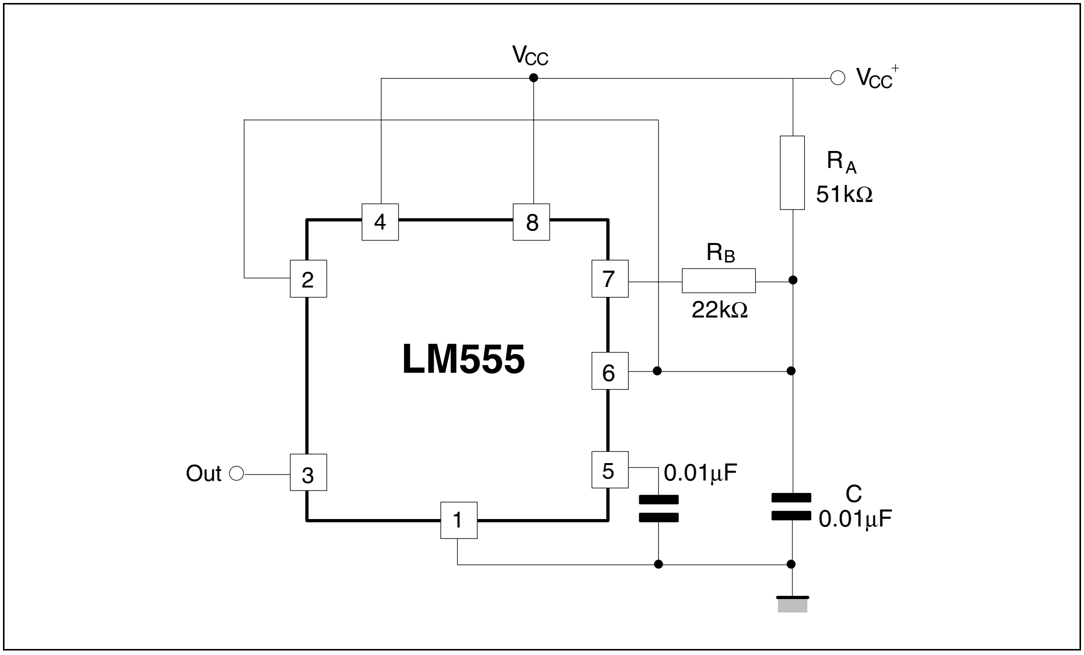
For the output low it is

$$t_2 = \ [(R.\ RB)/(RA+RB)].C.Ln\left[\frac{RB - 2RA}{2RB - RA}\right]$$

Thus the frequency of oscillation is:

$$f = \frac{1}{t1 + t2}$$

Figure 21. 50% duty cycle oscillator



Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

4.6 Additional information

Adequate power supply bypassing is necessary to protect associated circuitry. The minimum recommended is 0.1 µF in parallel with 1 µF electrolytic.