

## UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER

### GENERAL DESCRIPTION

The HG82C51 is a USART (Universal Synchronous Asynchronous Receiver Transmitter) for serial data communication.

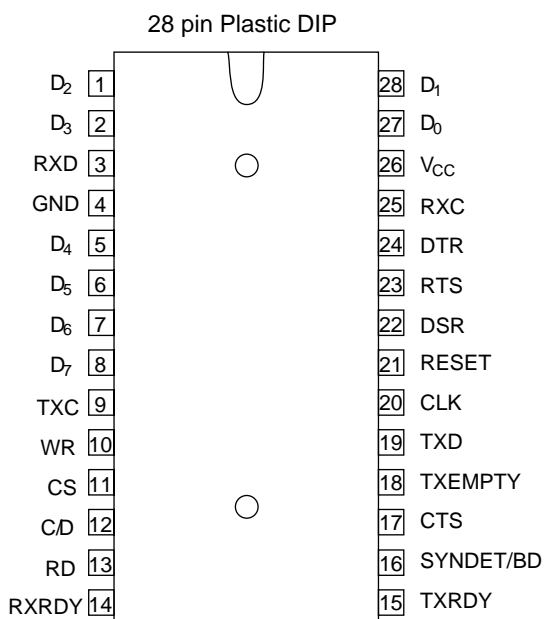
As a peripheral device of a microcomputer system, the HG82C51 receives parallel data from the CPU and transmits serial data after conversion. This device also receives serial data from the outside and transmits parallel data to the CPU after conversion.

The HG82C51 configures a fully static circuit using silicon gate CMOS technology. Therefore, it operates on extremely low power at 100  $\mu$ A (max) of standby current by suspending all operations.

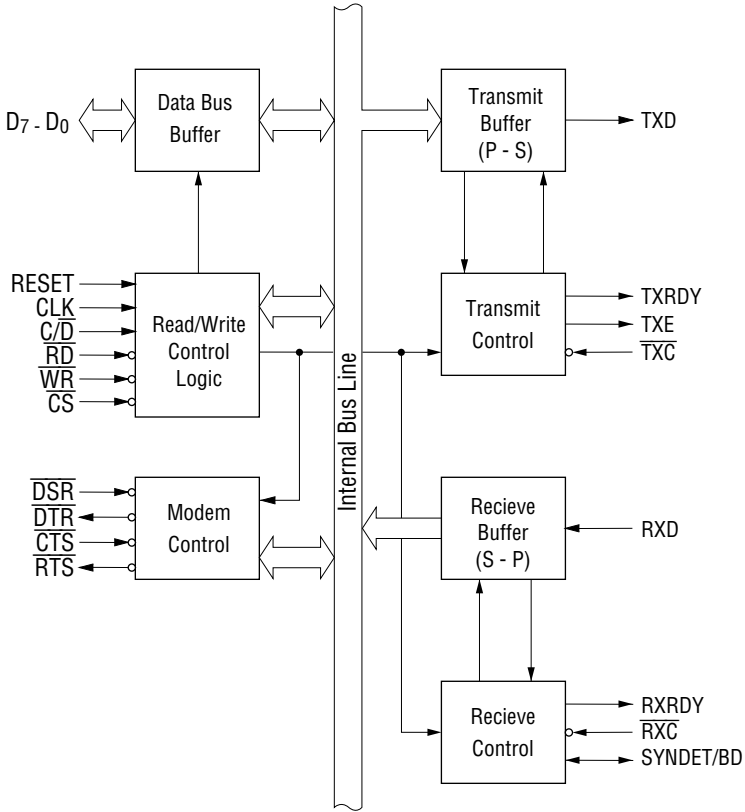
### FEATURES

- Wide power supply voltage range from 3 V to 6 V
- Wide temperature range from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- Synchronous communication upto 64 Kbaud
- Asynchronous communication upto 38.4 Kbaud
- Transmitting/receiving operations under double buffered configuration.
- Error detection (parity, overrun and framing)
- 28-pin Plastic DIP (DIP28-P-600-2.54)

### PIN CONFIGURATION (TOP VIEW)

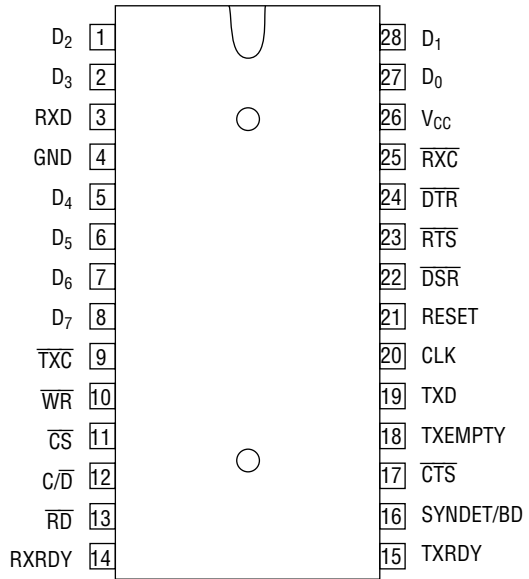


FUNCTIONAL BLOCK DIAGRAM

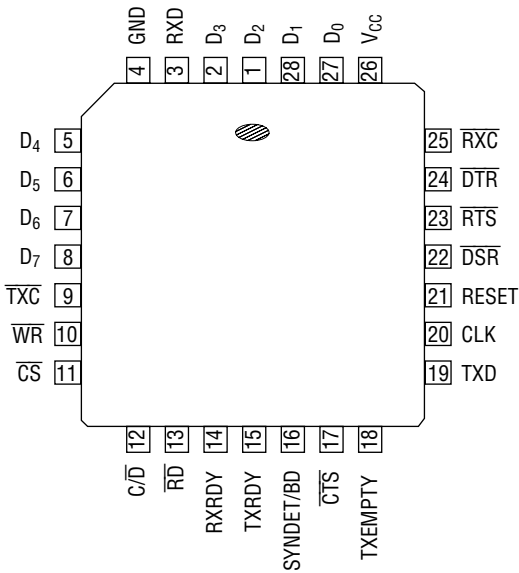


**PIN CONFIGURATION (TOP VIEW)**

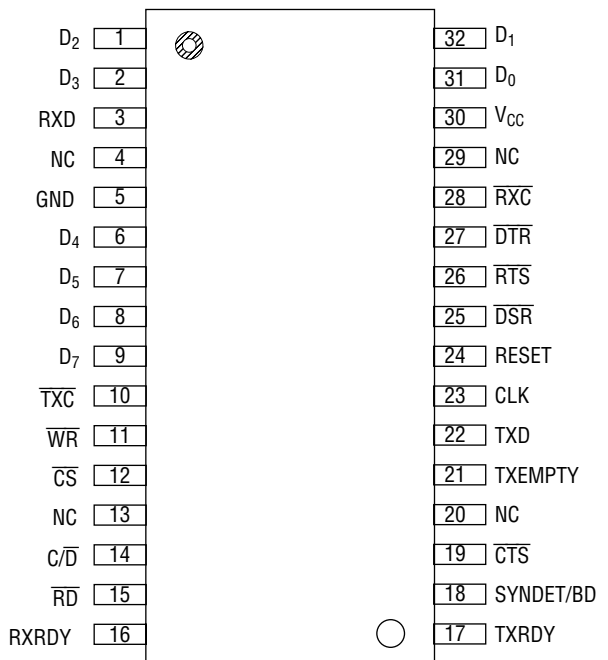
**28 pin Plastic DIP**



**28 pin Plastic QFJ**



**32 pin Plastic SSOP**



## FUNCTION

### Outline

The HG82C51's functional configuration is programmed by software. Operation between the HG82C51 and a CPU is executed by program control. Table 1 shows the operation between a CPU and the device.

Table 1 Operation between HG82C51 and CPU

| $\overline{CS}$ | C/D | $\overline{RD}$ | $\overline{WR}$ |                    |
|-----------------|-----|-----------------|-----------------|--------------------|
| 1               | ×   | ×               | ×               | Data Bus 3-State   |
| 0               | ×   | 1               | 1               | Data Bus 3-State   |
| 0               | 1   | 0               | 1               | Status → CPU       |
| 0               | 1   | 1               | 0               | Control Word ← CPU |
| 0               | 0   | 0               | 1               | Data → CPU         |
| 0               | 0   | 1               | 0               | Data ← CPU         |

It is necessary to execute a function-setting sequence after resetting the HG82C51. Fig. 1 shows the function-setting sequence.

If the function was set, the device is ready to receive a command, thus enabling the transfer of data by setting a necessary command, reading a status and reading/writing data.

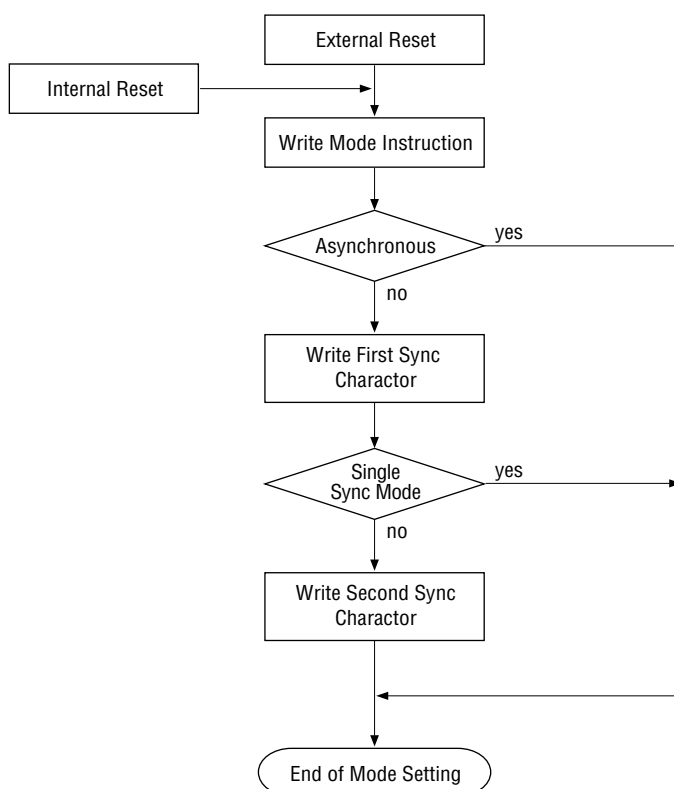


Fig. 1 Function-setting Sequence (Mode Instruction Sequence)

## Control Words

There are two types of control word.

1. Mode instruction (setting of function)
2. Command (setting of operation)

### 1) Mode Instruction

Mode instruction is used for setting the function of the HG82C51. Mode instruction will be in "wait for write" at either internal reset or external reset. That is, the writing of a control word after resetting will be recognized as a "mode instruction."

Items set by mode instruction are as follows:

- Synchronous/asynchronous mode
- Stop bit length (asynchronous mode)
- Character length
- Parity bit
- Baud rate factor (asynchronous mode)
- Internal/external synchronization (synchronous mode)
- Number of synchronous characters (Synchronous mode)

The bit configuration of mode instruction is shown in Figures 2 and 3. In the case of synchronous mode, it is necessary to write one-or two byte sync characters.

If sync characters were written, a function will be set because the writing of sync characters constitutes part of mode instruction.

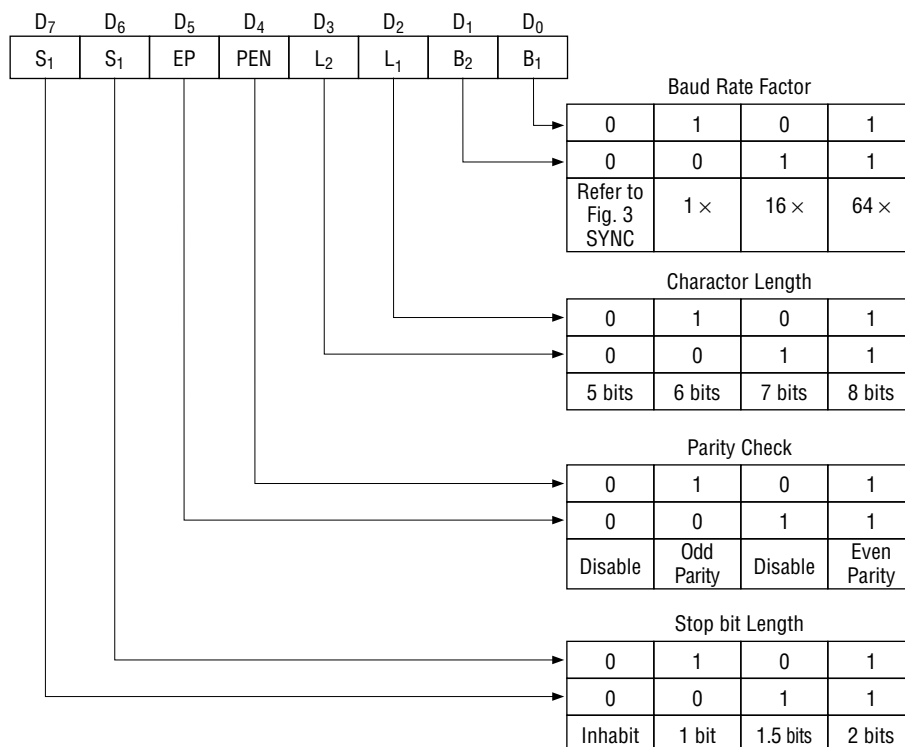
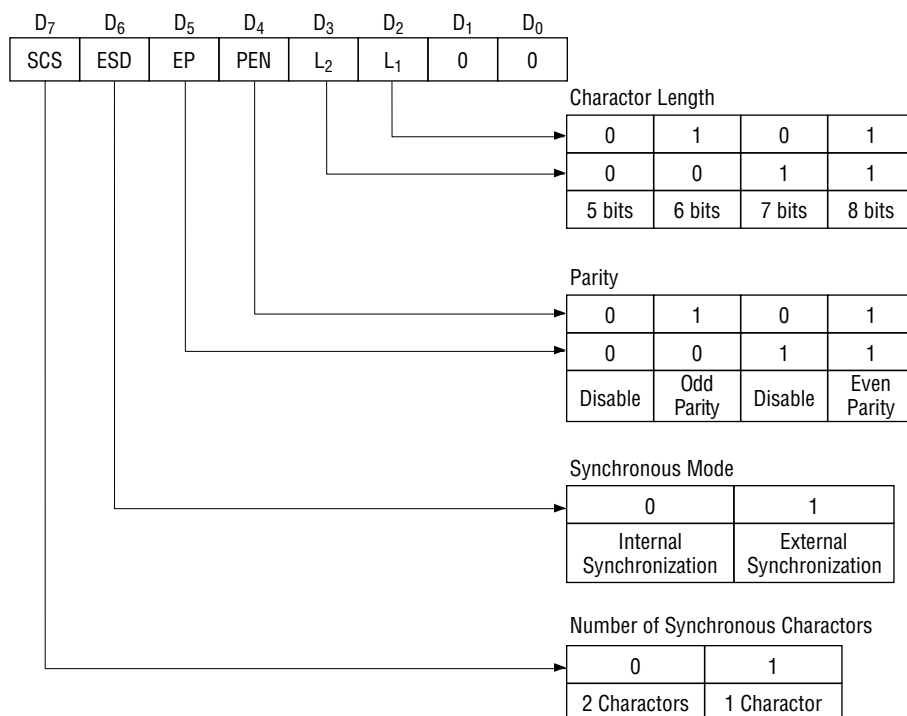


Fig. 2 Bit Configuration of Mode Instruction (Asynchronous)



**Fig. 3 Bit Configuration of Mode Instruction (Synchronous)**

## 2) Command

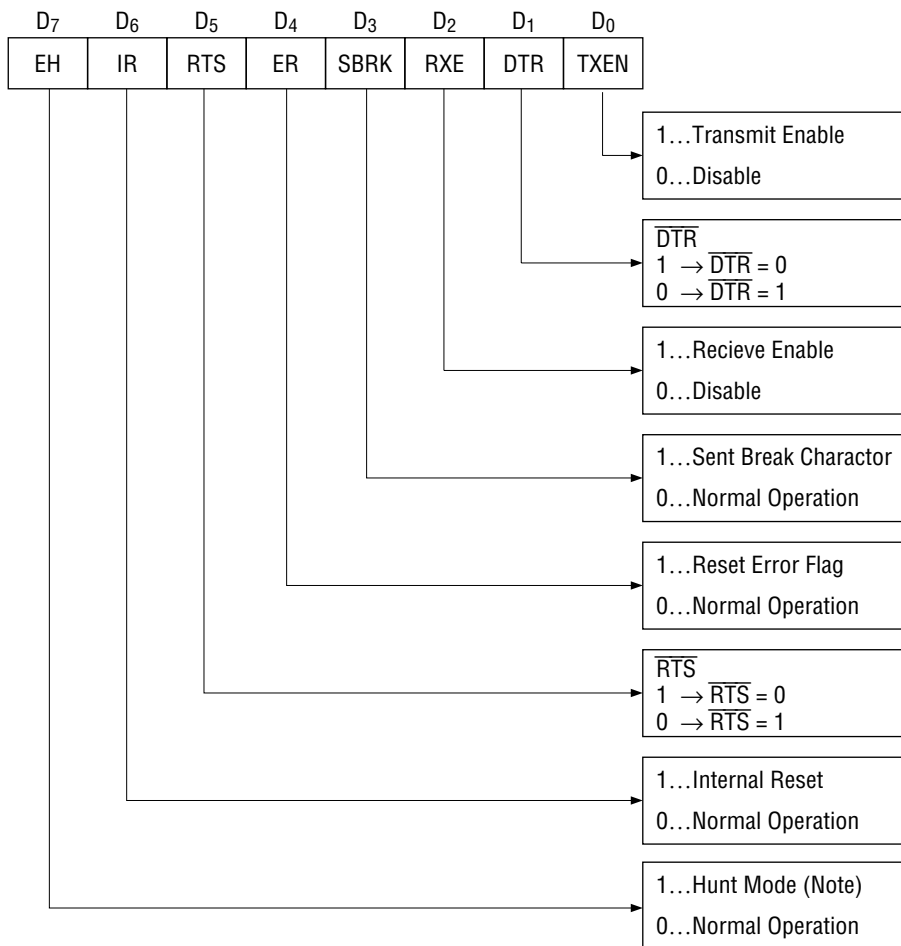
Command is used for setting the operation of the HG82C51.

It is possible to write a command whenever necessary after writing a mode instruction and sync characters.

Items to be set by command are as follows:

- Transmit Enable/Disable
- Receive Enable/Disable
- $\overline{\text{DTR}}$ ,  $\overline{\text{RTS}}$  Output of data.
- Resetting of error flag.
- Sending to break characters
- Internal resetting
- Hunt mode (synchronous mode)

The bit configuration of a command is shown in Fig. 4.

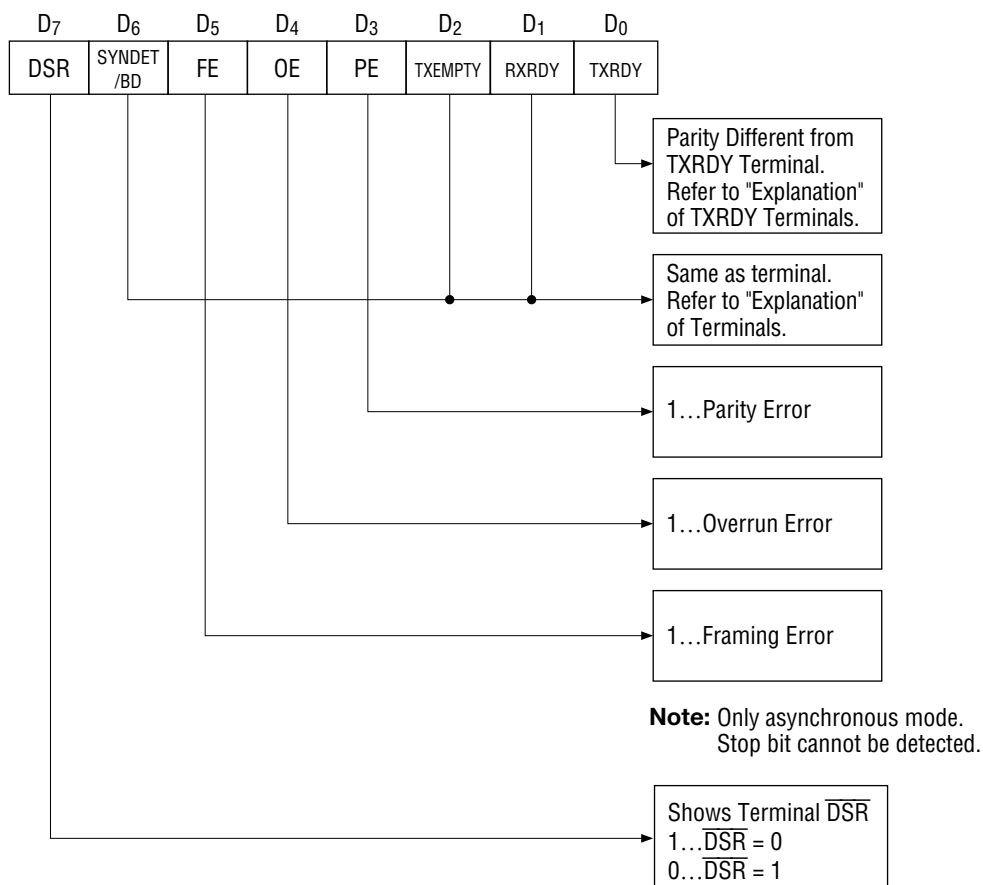


**Note:** Seach mode for synchronous characters in synchronous mode.

**Fig. 4 Bit Configuration of Command**

## Status Word

It is possible to see the internal status of HG82C51 by reading a status word. The bit configuration of status word is shown in Fig. 5.



**Fig. 5 Bit Configuration of Status Word**

## Standby Status

It is possible to put the HG82C51 in standby status. When the following conditions have been satisfied the HG82C51 is in standby status.

- (1)  $\overline{\text{CS}}$  terminal is fixed at  $V_{cc}$  level.
- (2) Input pins other  $\overline{\text{CS}}$ ,  $\text{D}_0$  to  $\text{D}_7$ ,  $\overline{\text{RD}}$ ,  $\overline{\text{WR}}$  and  $\text{C}/\overline{\text{D}}$  are fixed at  $V_{cc}$  or  $\text{GND}$  level (including SYNDET in external synchronous mode).

Note: When all output currents are 0, ICCS specification is applied.



## Pin Description

### **D<sub>0</sub> to D<sub>7</sub> (I/O terminal)**

This is bidirectional data bus which receive control words and transmits data from the CPU and sends status words and received data to CPU.

### **RESET (Input terminal)**

A High on this input forces the HG82C51 into reset status.

The device waits for the writing of "mode instruction."

The min. reset width is six clock inputs during the operating status of CLK.

### **CLK (Input terminal)**

CLK signal is used to generate internal device timing.

CLK signal is independent of  $\overline{RXC}$  or  $\overline{TXC}$ .

However, the frequency of CLK must be greater than 30 times the  $\overline{RXC}$  and  $\overline{TXC}$  at Synchronous mode and Asynchronous "x1" mode, and must be greater than 5 times at Asynchronous "x16" and "x64" mode.

### **$\overline{WR}$ (Input terminal)**

This is the "active low" input terminal which receives a signal for writing transmit data and control words from the CPU into the HG82C51.

### **$\overline{RD}$ (Input terminal)**

This is the "active low" input terminal which receives a signal for reading receive data and status words from the HG82C51.

### **C/ $\overline{D}$ (Input terminal)**

This is an input terminal which receives a signal for selecting data or command words and status words when the HG82C51 is accessed by the CPU.

If C/ $\overline{D}$  = low, data will be accessed.

If C/ $\overline{D}$  = high, command word or status word will be accessed.

### **$\overline{CS}$ (Input terminal)**

This is the active low input terminal which selects the HG82C51 at low level when the CPU accesses.

Note: The device won't be in "standby status"; only setting  $\overline{CS}$  = High.  
Refer to "Explanation of Standby Status."

### **TXD (output terminal)**

This is an output terminal for transmitting data from which serial-converted data is sent out. The device is in "mark status" (high level) after resetting or during a status when transmit is disabled. It is also possible to set the device in "break status" (low level) by a command.

**TXRDY (output terminal)**

This is an output terminal which indicates that the HG82C51 is ready to accept a transmitted data character. But the terminal is always at low level if  $\overline{\text{CTS}}$  = high or the device was set in "TX disable status" by a command.

Note: TXRDY status word indicates that transmit data character is receivable, regardless of  $\overline{\text{CTS}}$  or command.

If the CPU writes a data character, TXRDY will be reset by the leading edge or  $\overline{\text{WR}}$  signal.

**TXEMPTY (Output terminal)**

This is an output terminal which indicates that the HG82C51 has transmitted all the characters and had no data character.

In "synchronous mode," the terminal is at high level, if transmit data characters are no longer remaining and sync characters are automatically transmitted. If the CPU writes a data character, TXEMPTY will be reset by the leading edge of  $\overline{\text{WR}}$  signal.

Note : As the transmitter is disabled by setting  $\overline{\text{CTS}}$  "High" or command, data written before disable will be sent out. Then TXD and TXEMPTY will be "High".

Even if a data is written after disable, that data is not sent out and TXE will be "High". After the transmitter is enabled, it sent out. (Refer to Timing Chart of Transmitter Control and Flag Timing)

 **$\overline{\text{TXC}}$  (Input terminal)**

This is a clock input signal which determines the transfer speed of transmitted data.

In "synchronous mode," the baud rate will be the same as the frequency of  $\overline{\text{TXC}}$ .

In "asynchronous mode," it is possible to select the baud rate factor by mode instruction.

It can be 1, 1/16 or 1/64 the  $\overline{\text{TXC}}$ .

The falling edge of  $\overline{\text{TXC}}$  sifts the serial data out of the HG82C51.

**RXD (input terminal)**

This is a terminal which receives serial data.

**RXRDY (Output terminal)**

This is a terminal which indicates that the HG82C51 contains a character that is ready to READ.

If the CPU reads a data character, RXRDY will be reset by the leading edge of  $\overline{\text{RD}}$  signal.

Unless the CPU reads a data character before the next one is received completely, the preceding data will be lost. In such a case, an overrun error flag status word will be set.

 **$\overline{\text{RXC}}$  (Input terminal)**

This is a clock input signal which determines the transfer speed of received data.

In "synchronous mode," the baud rate is the same as the frequency of  $\overline{\text{RXC}}$ .

In "asynchronous mode," it is possible to select the baud rate factor by mode instruction.

It can be 1, 1/16, 1/64 the  $\overline{\text{RXC}}$ .

**SYNDET/BD (Input or output terminal)**

This is a terminal whose function changes according to mode.

In “internal synchronous mode,” this terminal is at high level, if sync characters are received and synchronized. If a status word is read, the terminal will be reset.

In “external synchronous mode,” this is an input terminal.

A High on this input forces the HG82C51 to start receiving data characters.

In “asynchronous mode,” this is an output terminal which generates “high level” output upon the detection of a “break” character if receiver data contains a “low-level” space between the stop bits of two continuous characters. The terminal will be reset, if RXD is at high level.

After Reset is active, the terminal will be output at low level.

 **$\overline{\text{DSR}}$  (Input terminal)**

This is an input port for MODEM interface. The input status of the terminal can be recognized by the CPU reading status words.

 **$\overline{\text{DTR}}$  (Output terminal)**

This is an output port for MODEM interface. It is possible to set the status of  $\overline{\text{DTR}}$  by a command.

 **$\overline{\text{CTS}}$  (Input terminal)**

This is an input terminal for MODEM interface which is used for controlling a transmit circuit. The terminal controls data transmission if the device is set in “TX Enable” status by a command. Data is transmittable if the terminal is at low level.

 **$\overline{\text{RTS}}$  (Output terminal)**

This is an output port for MODEM interface. It is possible to set the status  $\overline{\text{RTS}}$  by a command.

**ABSOLUTE MAXIMUM RATING**

| Parameter            | Symbol    | Rating                 | Unit | Conditions                 |
|----------------------|-----------|------------------------|------|----------------------------|
| Power Supply Voltage | $V_{CC}$  | -0.5 to +7             | V    | With respect to GND        |
| Input Voltage        | $V_{IN}$  | -0.5 to $V_{CC} + 0.5$ | V    |                            |
| Output Voltage       | $V_{OUT}$ | -0.5 to $V_{CC} + 0.5$ | V    |                            |
| Storage Temperature  | $T_{STG}$ | -55 to +150            | °C   | —                          |
| Power Dissipation    | $P_D$     | 0.9                    | W    | $T_a = 25^{\circ}\text{C}$ |

**OPERATING RANGE**

| Parameter             | Symbol   | Range     | Unit |
|-----------------------|----------|-----------|------|
| Power Supply Voltage  | $V_{CC}$ | 3 - 6     | V    |
| Operating Temperature | $T_{op}$ | -40 to 85 | °C   |

**RECOMMENDED OPERATING CONDITIONS**

| Parameter             | Symbol   | Min. | Typ. | Max.           | Unit |
|-----------------------|----------|------|------|----------------|------|
| Power Supply Voltage  | $V_{CC}$ | 4.5  | 5    | 5.5            | V    |
| Operating Temperature | $T_{op}$ | -40  | +25  | +85            | °C   |
| "L" Input Voltage     | $V_{IL}$ | -0.3 | —    | +0.8           | V    |
| "H" Input Voltage     | $V_{IH}$ | 2.2  | —    | $V_{CC} + 0.3$ | V    |

**DC CHARACTERISTICS**

( $V_{CC} = 4.5$  to  $5.5$  V  $T_a = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )

| Parameter                | Symbol    | Min. | Typ. | Max. | Unit          | Measurement Conditions                                     |
|--------------------------|-----------|------|------|------|---------------|--|
| "L" Output Voltage       | $V_{OL}$  | —    | —    | 0.45 | V             | $I_{OL} = 2.5$ mA  |
| "H" Output Voltage       | $V_{OH}$  | 3.7  | —    | —    | V             | $I_{OH} = -2.5$ mA   |
| Input Leak Current       | $I_{LI}$  | -10  | —    | 10   | $\mu\text{A}$ | $0 \leq V_{IN} \leq V_{CC}$                                |
| Output Leak Current      | $I_{LO}$  | -10  | —    | 10   | $\mu\text{A}$ | $0 \leq V_{OUT} \leq V_{CC}$                               |
| Operating Supply Current | $I_{CCO}$ | —    | —    | 5    | mA            | Asynchronous X64 during Transmitting/Receiving             |
| Standby Supply Current   | $I_{CCS}$ | —    | —    | 100  | $\mu\text{A}$ | All Input voltage shall be fixed at $V_{CC}$ or GND level. |

## AC CHARACTERISTICS

### CPU Bus Interface Part

( $V_{CC} = 4.5$  to  $5.5$  V,  $T_a = -40$  to  $85^\circ\text{C}$ )

| Parameter                             | Symbol     | Min. | Max. | Unit     | Remarks |
|---------------------------------------|------------|------|------|----------|---------|
| Address Stable before $\overline{RD}$ | $t_{AR}$   | 20   | —    | ns       | Note 2  |
| Address Hold Time for $\overline{RD}$ | $t_{RA}$   | 20   | —    | ns       | Note 2  |
| $\overline{RD}$ Pulse Width           | $t_{RR}$   | 130  | —    | ns       | —       |
| Data Delay from $\overline{RD}$       | $t_{RD}$   | —    | 100  | ns       | —       |
| $\overline{RD}$ to Data Float         | $t_{DF}$   | 10   | 75   | ns       | —       |
| Recovery Time between $\overline{RD}$ | $t_{RVR}$  | 6    | —    | $t_{CY}$ | Note 5  |
| Address Stable before $\overline{WR}$ | $t_{AW}$   | 20   | —    | ns       | Note 2  |
| Address Hold Time for $\overline{WR}$ | $t_{WA}$   | 20   | —    | ns       | Note 2  |
| $\overline{WR}$ Pulse Width           | $t_{WW}$   | 100  | —    | ns       | —       |
| Data Set-up Time for $\overline{WR}$  | $t_{DW}$   | 100  | —    | ns       | —       |
| Data Hold Time for $\overline{WR}$    | $t_{WD}$   | 0    | —    | ns       | —       |
| Recovery Time between $\overline{WR}$ | $t_{RVW}$  | 6    | —    | $t_{CY}$ | Note 4  |
| RESET Pulse Width                     | $t_{RESW}$ | 6    | —    | $t_{CY}$ | —       |

## Serial Interface Part

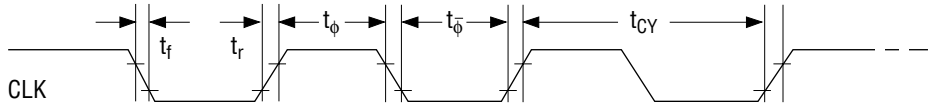
(V<sub>CC</sub> = 4.5 to 5.5 V, T<sub>a</sub> = -40 to 85°C)

| Parameter  | Symbol                          | Min.             | Max.                 | Unit            | Remarks              |
|--|---------------------------------|------------------|----------------------|-----------------|----------------------|
| Main Clock Period  | t <sub>CY</sub>                 | 160              | —                    | ns              | Note 3               |
| Clock Low Time   | t <sub>φ</sub>                  | 50               | —                    | ns              | —                    |
| Clock High Time  | t <sub>φ</sub>                  | 70               | t <sub>CY</sub> - 50 | ns              | —                    |
| Clock Rise/Fall Time   | t <sub>r</sub> , t <sub>f</sub> | —                | 20                   | ns              | —                    |
| TXD Delay from Falling Edge of $\overline{\text{TXC}}$                     | t <sub>DTX</sub>                | —                | 1                    | μS              | —                    |
| Transmitter Clock Frequency  | 1 × Baud                        | f <sub>TX</sub>  | DC                   | 64              | kHz<br>Note 3        |
|  | 16 × Baud                       | f <sub>TX</sub>  | DC                   | 615             |                      |
|  | 64 × Baud                       | f <sub>TX</sub>  | DC                   | 615             |                      |
| Transmitter Clock Low Time   | 1 × Baud                        | t <sub>TPW</sub> | 13                   | —               | t <sub>CY</sub><br>— |
|  | 16 ×, 64 × Baud                 | t <sub>TPW</sub> | 2                    | —               | t <sub>CY</sub><br>— |
| Transmitter Clock High Time  | 1 × Baud                        | t <sub>TPD</sub> | 15                   | —               | t <sub>CY</sub><br>— |
|  | 16 ×, 64 × Baud                 | t <sub>TPD</sub> | 3                    | —               | t <sub>CY</sub><br>— |
| Receiver Clock Frequency   | 1 × Baud                        | f <sub>RX</sub>  | DC                   | 64              | kHz<br>Note 3        |
|  | 16 × Baud                       | f <sub>RX</sub>  | DC                   | 615             |                      |
|  | 64 × Baud                       | f <sub>RX</sub>  | DC                   | 615             |                      |
| Receiver Clock Low Time  | 1 × Baud                        | t <sub>RPW</sub> | 13                   | —               | t <sub>CY</sub><br>— |
|  | 16 ×, 64 × Baud                 | t <sub>RPW</sub> | 2                    | —               | t <sub>CY</sub><br>— |
| Receiver Clock High Time   | 1 × Baud                        | t <sub>RPD</sub> | 15                   | —               | t <sub>CY</sub><br>— |
|  | 16 ×, 64 × Baud                 | t <sub>RPD</sub> | 3                    | —               | t <sub>CY</sub><br>— |
| Time from the Center of Last Bit to the Rise of TXRDY                      | t <sub>TXRDY</sub>              | —                | 8                    | t <sub>CY</sub> | —                    |
| Time from the Leading Edge of $\overline{\text{WR}}$ to the Fall of TXRDY  | t <sub>TXRDY CLEAR</sub>        | —                | 400                  | ns              | —                    |
| Time From the Center of Last Bit to the Rise of RXRDY                      | t <sub>RXRDY</sub>              | —                | 26                   | t <sub>CY</sub> | —                    |
| Time from the Leading Edge of $\overline{\text{RD}}$ to the Fall of RXRDY  | t <sub>RXRDY CLEAR</sub>        | —                | 400                  | ns              | —                    |
| Internal SYNDET Delay Time from Rising Edge of $\overline{\text{RXC}}$     | t <sub>IS</sub>                 | —                | 26                   | t <sub>CY</sub> | —                    |
| SYNDET Setup Time for $\overline{\text{RXC}}$                              | t <sub>ES</sub>                 | 18               | —                    | t <sub>CY</sub> | —                    |
| TXE Delay Time from the Center of Last Bit                                 | t <sub>TXEMPTY</sub>            | 20               | —                    | t <sub>CY</sub> | —                    |
| MODEM Control Signal Delay Time from Rising Edge of $\overline{\text{WR}}$ | t <sub>WC</sub>                 | 8                | —                    | t <sub>CY</sub> | —                    |
| MODEM Control Signal Setup Time for Falling Edge of $\overline{\text{RD}}$ | t <sub>CR</sub>                 | 20               | —                    | t <sub>CY</sub> | —                    |
| RXD Setup Time for Rising Edge of $\overline{\text{RXC}}$ (1X Baud)        | t <sub>RXDS</sub>               | 11               | —                    | t <sub>CY</sub> | —                    |
| RXD Hold Time for Falling Edge of $\overline{\text{RXC}}$ (1X Baud)        | t <sub>RXDH</sub>               | 17               | —                    | t <sub>CY</sub> | —                    |

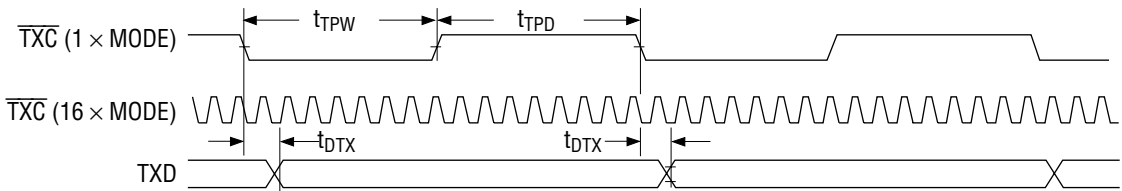
- Notes:
1. AC characteristics are measured at 150 pF capacity load as an output load based on 0.8 V at low level and 2.2 V at high level for output and 1.5 V for input.
  2. Addresses are CS and C/D.
  3. f<sub>TX</sub> or f<sub>RX</sub> ≤ 1/(30 T<sub>cy</sub>) 1× Baud  
f<sub>TX</sub> or f<sub>RX</sub> ≤ 1/(5 T<sub>cy</sub>) 16×, 64× Baud
  4. This recovery time is mode Initialization only. Recovery time between command writes for Asynchronous Mode is 8 t<sub>CY</sub> and for Synchronous Mode is 18 t<sub>CY</sub>. Write Data is allowed only when TXRDY = 1.
  5. This recovery time is Status read only. Read Data is allowed only when RXRDY = 1.
  6. Status update can have a maximum delay of 28 clock periods from event affecting the status.

**TIMING CHART**

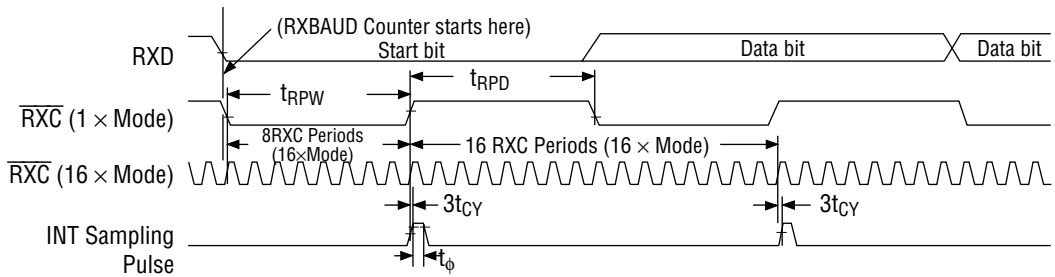
**System Clock Input**



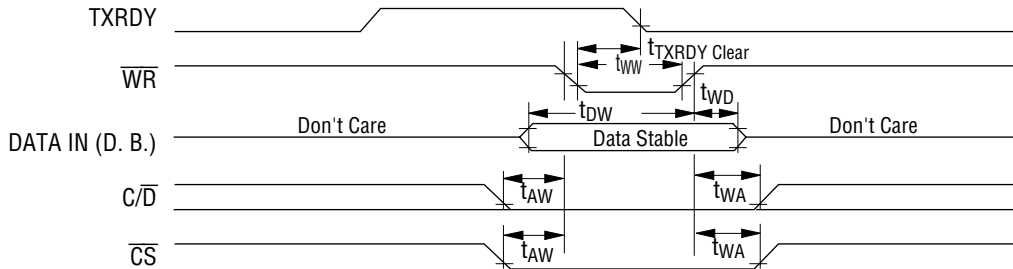
**Transmitter Clock and Data**



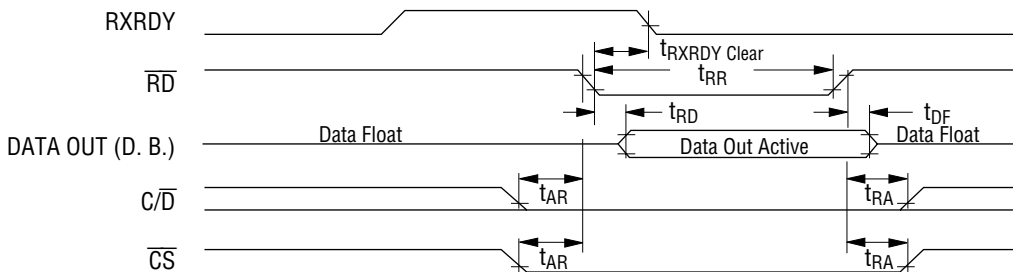
**Receiver Clock and Data**



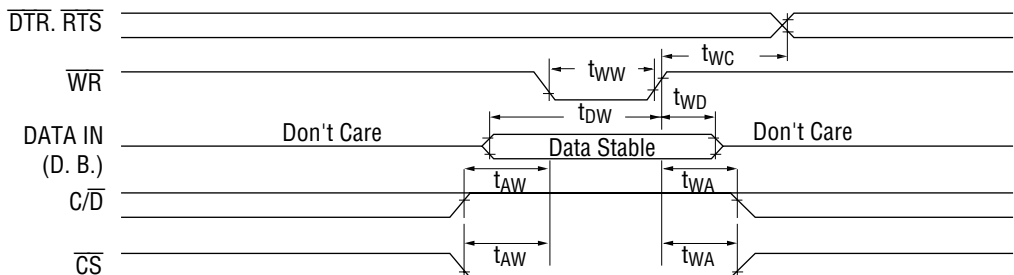
**Write Data Cycle (CPU → USART)**



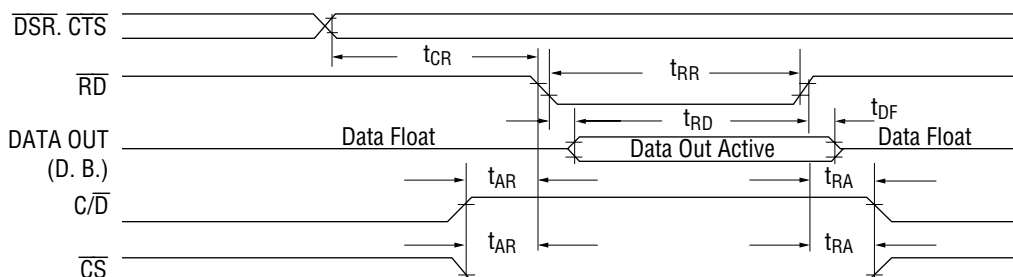
**Read Data Cycle (CPU ← USART)**



**Write Control or Output Port Cycle (CPU → USART)**

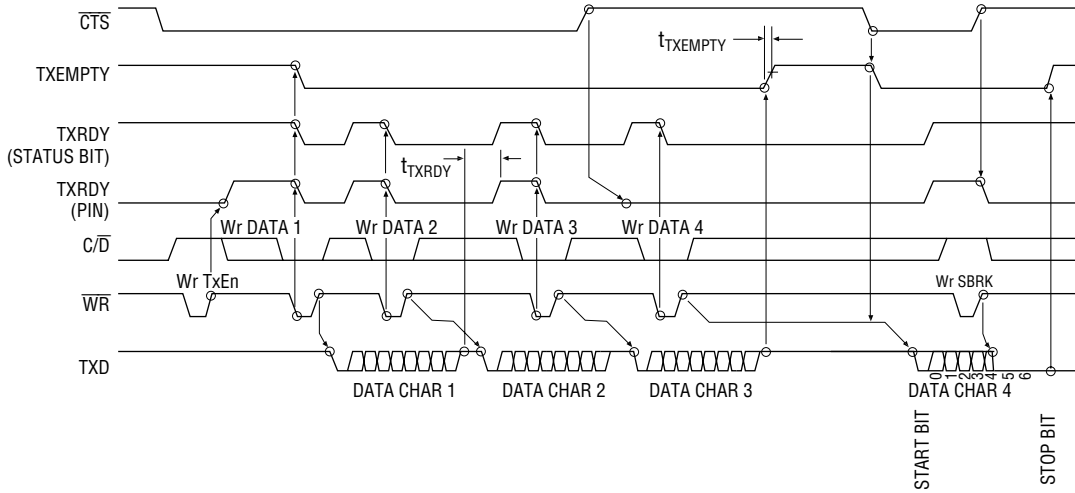


**Read Control or Input Port Cycle (CPU ← USART)**



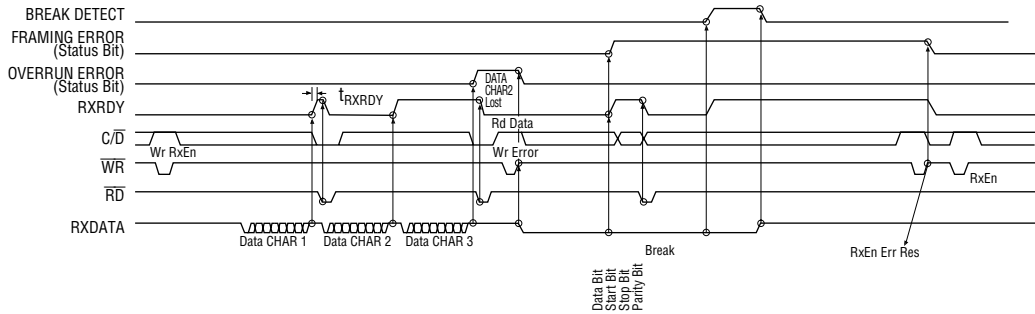


**Transmitter Control and Flag Timing (ASYNC Mode)**



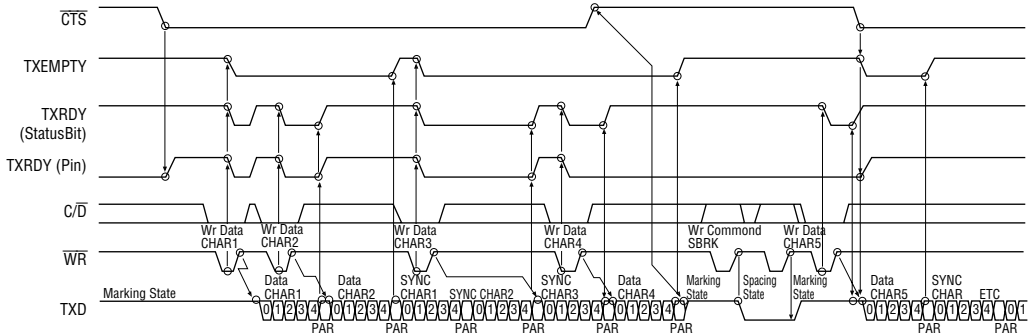
**Note:** The wave-form chart is based on the case of 7-bit data length + parity bit + 2 stop bit.

**Receiver Control and Flag Timing (ASYNC Mode)**



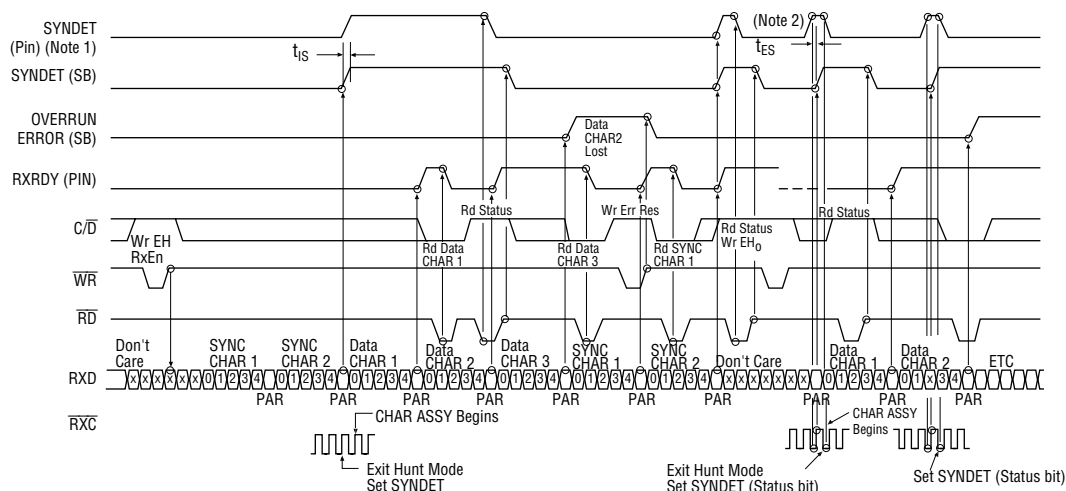
**Note:** The wave-form chart is based on the case of 7 data bit length + parity bit + 2 stop bit.

**Transmitter Control and Flag Timing (SYNC Mode)**



**Note:** The wave-form chart is based on the case of 5 data bit length + parity bit and 2 synchronous characters.

Receiver Control and Flag Timing (SYNC Mode)



- Note:** 1. Internal Synchronization is based on the case of 5 data bit length + parity bit and 2 synchronous character.
- 2. External Synchronization is based on the case of 5 data bit length + parity bit.

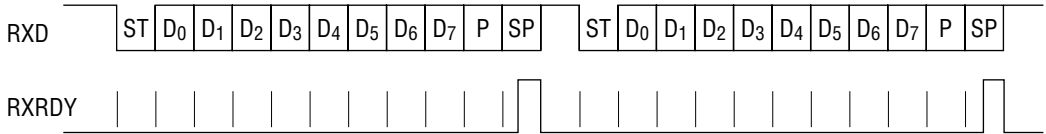
Note: 1. Half-bit processing for the start bit  
 When the HG82C51 is used in the asynchronous mode, some problems are caused in the processing for the start bit whose length is smaller than the 1-data bit length. (See Fig. 1.)

| Start bit Length                      | Mode | Operation   |
|---------------------------------------|------|---|
| Smaller than 7-Receiver Clock Length  | ×16  | The short start bit is ignored. (Normal)                |
| Smaller than 31-Receiver Clock Length | ×64  | The short start bit is ignored. (Normal)                |
| 8-Receiver Clock Length               | ×16  | Data cannot be received correctly due to a malfunction. |
| 32-Receiver Clock Length              | ×64  | Data cannot be received correctly due to a malfunction. |
| 9 to 16-Receiver Clock Length         | ×16  | The bit is regarded as a start bit. (normal)            |
| 33 to 64-Receiver Clock Length        | ×64  | The bit is regarded as a start bit. (normal)            |

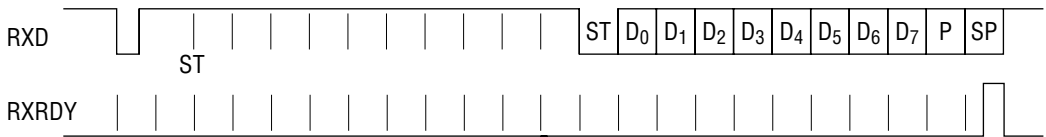
- 2. Parity flag after a break signal is received (See Fig. 2.)  
 When the HG82C51 is used in the asynchronous mode, a parity flag may be set when the next normal data is read after a break signal is received.  
 A parity flag is set when the rising edge of the break signal (end of the break signal) is changed between the final data bit and the parity bit, through a RXRDY signal may not be outputted.  
 If this occurs, the parity flag is left set when the next normal data is received, and the received data seems to be a parity error.

**Half-bit Processing Timing Chart for the Start bit (Fig. 1)**

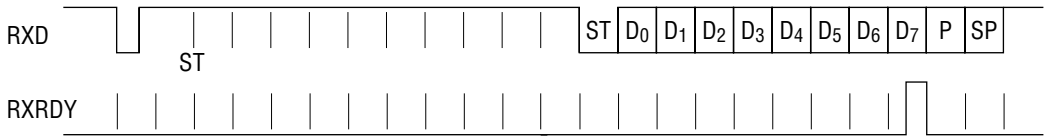
**Normal Operation**



**The Start bit Is Shorter Than a 1/2 Data bit**

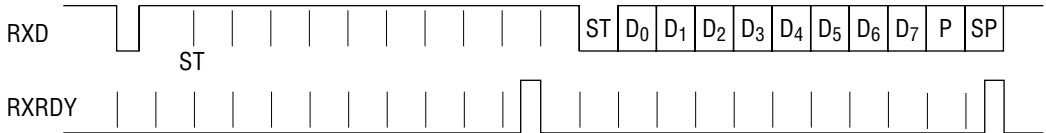


**The Start bit Is a 1/2 Data bit (A problem of HG82C51)**



A RXRDY signal is outputted during data reception due to a malfunction.

**The Start bit Is Longer Than a 1/2 Data bit**



ST: Start bit  
 SP: Stop bit  
 P: Parity bit  
 D<sub>0</sub> - D<sub>7</sub>: Data bits

!

**NOTICE ON REPLACING LOW-SPEED DEVICES WITH HIGH-SPEED DEVICES**

The conventional low speed devices are replaced by high-speed devices as shown below. When you want to replace your low speed devices with high-speed devices, read the replacement notice given on the next pages.

| <b>High-speed device (New)</b> | <b>Low-speed device (Old)</b> | <b>Remarks</b>  |
|--------------------------------|-------------------------------|-----------------|
| M80C85AH                       | M80C85A/M80C85A-2             | 8bit MPU        |
| M80C86A-10                     | M80C86A/M80C86A-2             | 16bit MPU       |
| M80C88A-10                     | M80C88A/M80C88A-2             | 8bit MPU        |
| M82C84A-2                      | M82C84A/M82C84A-5             | Clock generator |
| M81C55-5                       | M81C55                        | RAM.I/O, timer  |
| M82C37B-5                      | M82C37A/M82C37A-5             | DMA controller  |
| M82C51A-2                      | M82C51A                       | USART           |
| M82C53-2                       | M82C53-5                      | Timer           |
| M82C55A-2                      | M82C55A-5                     | PPI             |

## Differences between MSM82C51A and MSM82C51A-2

### 1) Manufacturing Process

These devices use a 3  $\mu$  Si-Gate CMOS process technology and have the same chip size.

### 2) Function

These devices have the same logics except for changes in AC characteristics listed in (3-2).

### 3) Electrical Characteristics

#### 3-1) DC Characteristics

| Parameter                              | Symbol          | MSM82C51A    | MSM82C51A-2 |
|--|-----------------|--------------|-------------|
| V <sub>OL</sub> measurement conditions | I <sub>OL</sub> | +2.0 mA      | +2.5 mA     |
| V <sub>OH</sub> measurement conditions | I <sub>OH</sub> | -400 $\mu$ A | -2.5 mA     |

Although the output voltage characteristics of these devices are identical, but the measurement conditions of the MSM82C51A-2 are more restricted than the MSM82C51A.

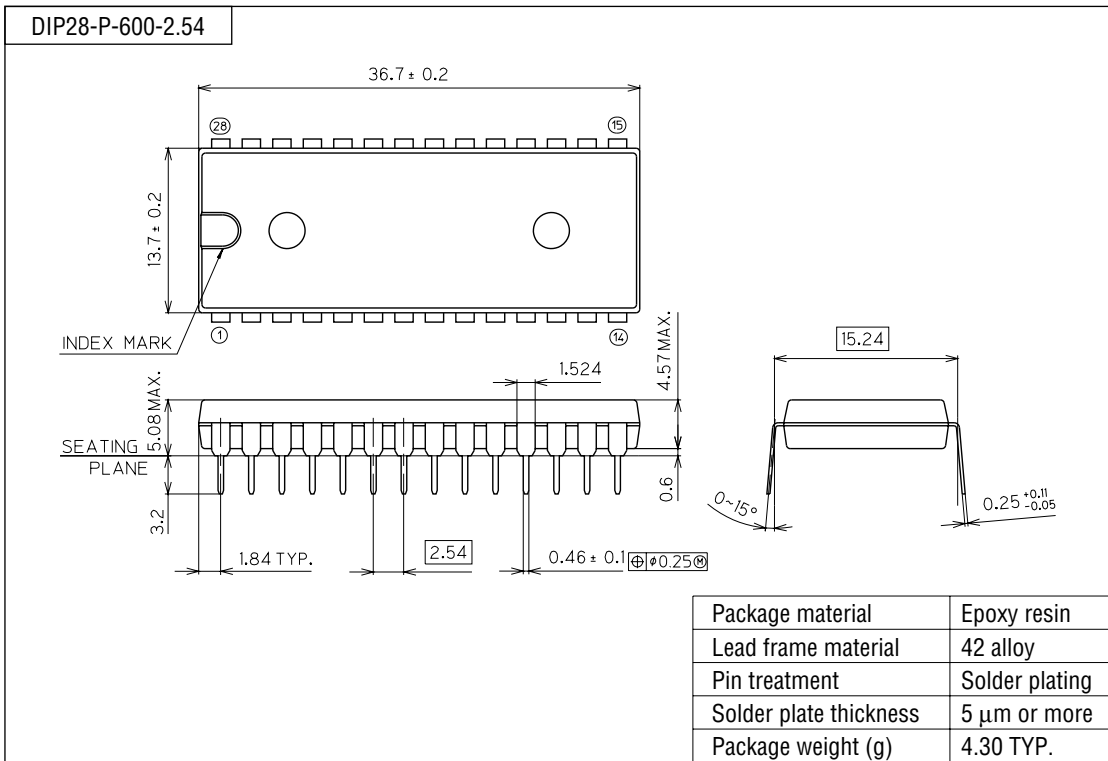
#### 3-2) AC Characteristics

| Parameter                                  | Symbol                         | MSM82C51A  | MSM82C51A-2                                     |
|--|--------------------------------|--|---|
| $\overline{RD}$ Pulse Width                | t <sub>RR</sub>                | 250 ns minimum                                   | 130 ns minimum                                  |
| $\overline{RD}$ Rising to Data Definition  | t <sub>RD</sub>                | 200 ns maximum                                   | 100 ns maximum                                  |
| $\overline{RD}$ Rising to Data Float       | t <sub>RF</sub>                | 100 ns maximum                                   | 75 ns minimum                                   |
| $\overline{WR}$ Pulse Width                | t <sub>WW</sub>                | 250 ns minimum                                   | 100 ns minimum                                  |
| Data Setup Time for $\overline{WR}$ Rising | t <sub>DW</sub>                | 150 ns minimum                                   | 100 ns minimum                                  |
| Data Hold Time for $\overline{WR}$ Rising  | t <sub>WD</sub>                | 20 ns minimum                                    | 0 ns minimum                                    |
| Master Clock Period                        | t <sub>CY</sub>                | 250 ns minimum                                   | 160 ns minimum                                  |
| Clock Low Time                             | t <sub><math>\phi</math></sub> | 90 ns minimum                                    | 50 ns minimum                                   |
| Clock High Time                            | t <sub><math>\phi</math></sub> | 120 ns minimum<br>t <sub>CY</sub> -90 ns maximum | 70 ns minimum<br>t <sub>CY</sub> -50 ns maximum |

As shown above, the MSM82C51A-2 satisfies the characteristics of the MSM82C51A.

PACKAGE DIMENSIONS

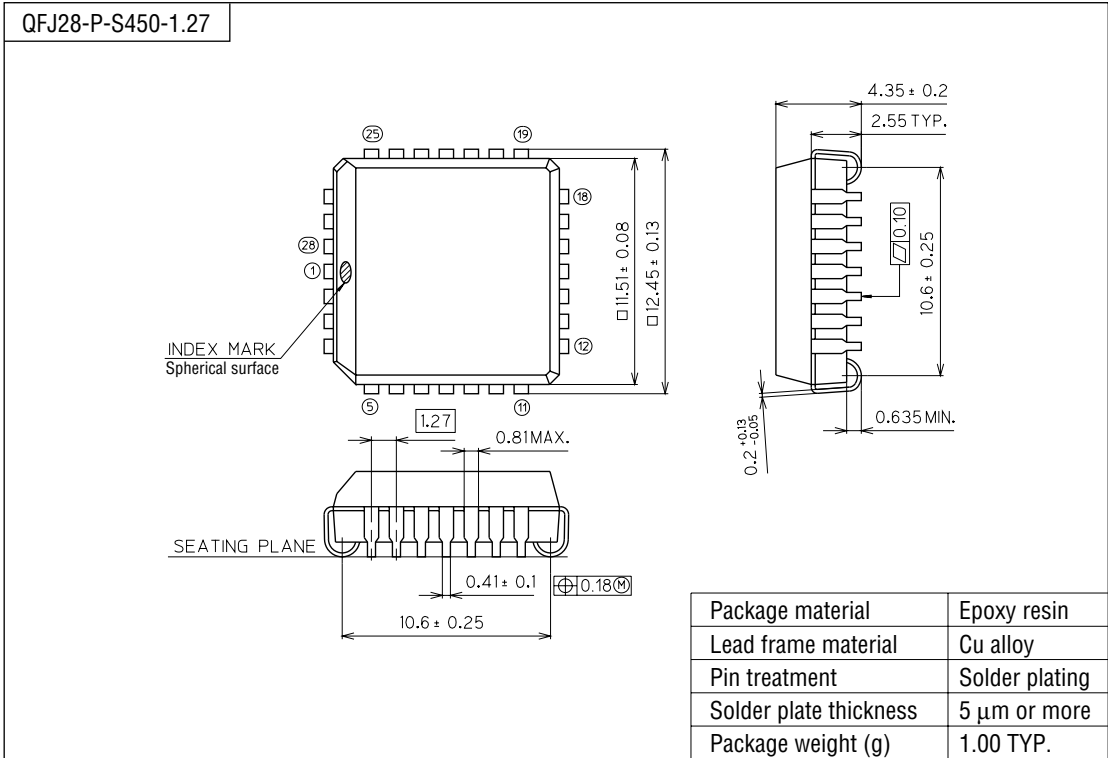
(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

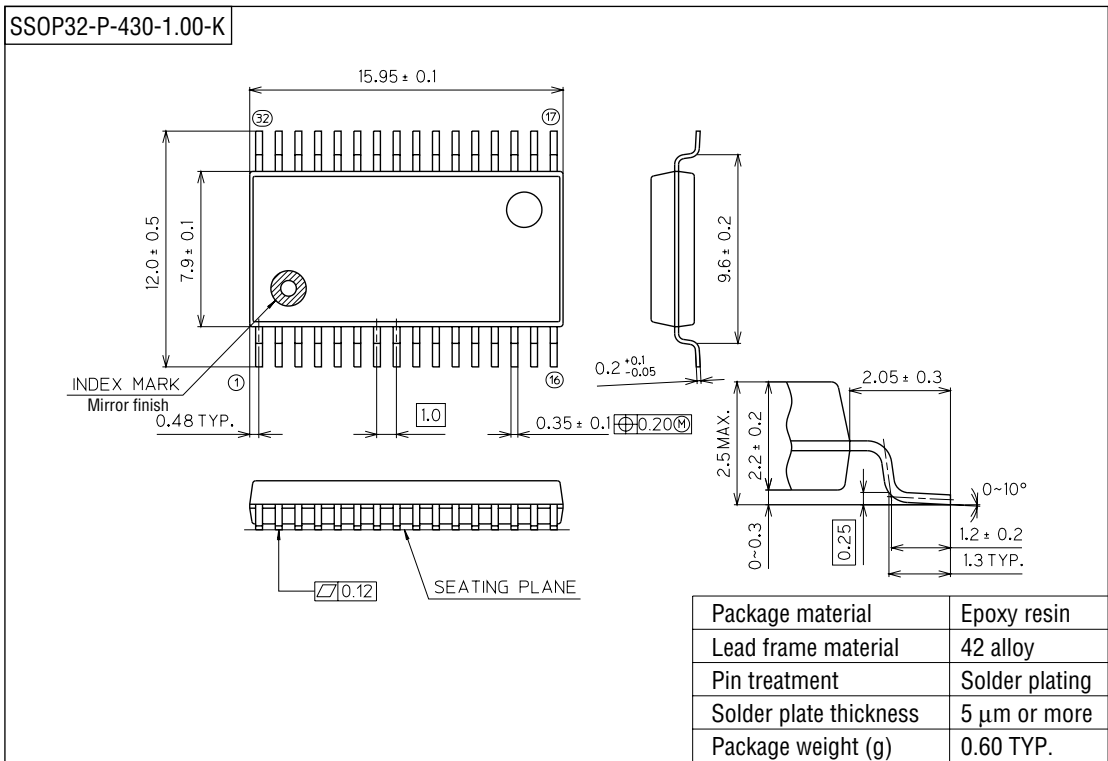


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(Unit : mm)



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#### 4) Notices on use

Note the following when replacing devices as the ASYNC pin is differently treated between the MSM82C84A and the MSM82C84A-5/MSM82C84A-2:

Case 1: When only a pullup resistor is externally connected to.  
The MSM82C84A can be replaced by the MSM82C84A-2.

Case 2: When only pulldown resistor is externally connected to.  
When the pulldown resistor is 8 kilohms or less, the MSM82C84A can be replaced by the MSM82C84A-2.  
When the pulldown resistor is greater than 8 kilohms, use a pulldown resistor of 8 kilohms or less.

Case 3: When an output of the other IC device is connected to the device.  
The MSM82C84A can be replaced by the MSM82C84A-2 when the  $I_{OL}$  pin of the device to drive the  $\overline{ASYNC}$  pin of the MSM82C84A-2 has an allowance of 100  $\mu\text{A}$  or more.