

## SNx4AHCT273 Octal D-Type Flip-Flops With Clear

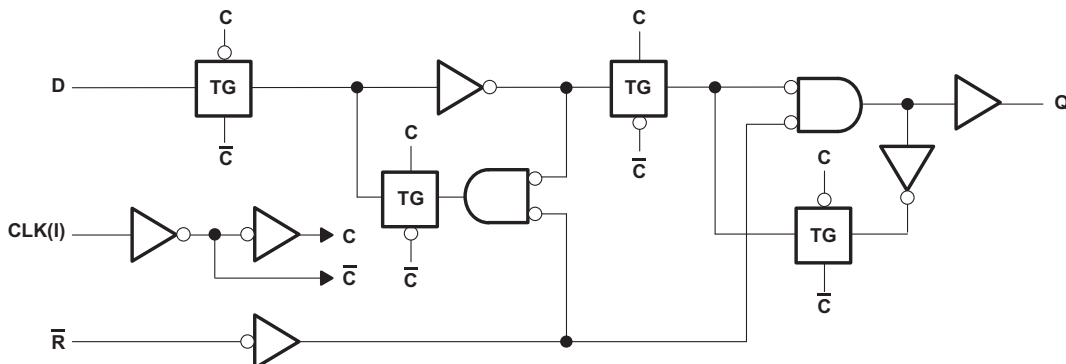
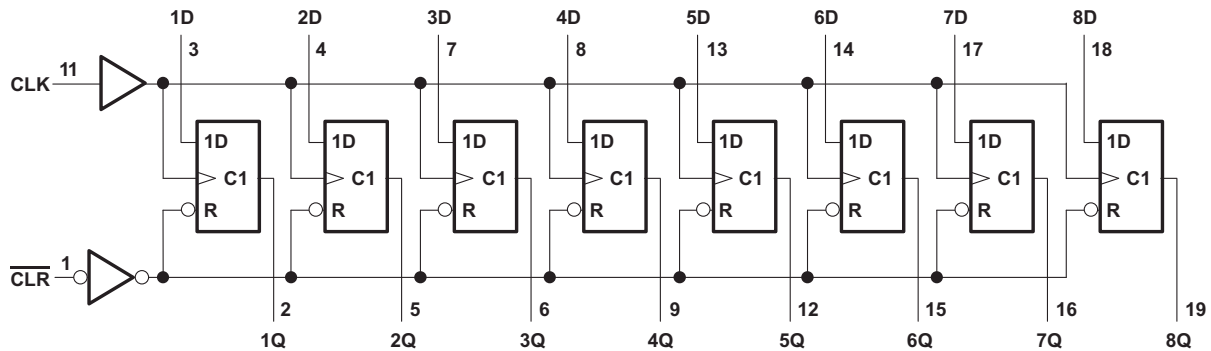
### 1 Features

- Inputs are TTL-Voltage Compatible
- Contain Eight Flip-Flops With Single-Rail Outputs
- Direct Clear Input
- Individual Data Input to Each Flip-Flop
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- Buffers and Storage Registers
- Shift Registers
- Pattern Generators
- Servers
- PCs and Notebooks
- Network Switches
- Memory Systems
- Databases

### 4 Simplified Schematics



### 3 Description

These devices are positive-edge-triggered D-type flip-flops with a direct clear (CLR) input.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4AHCT273	SSOP (20)	7.20 mm × 5.30 mm
	SOIC (20)	12.80 mm × 7.50 mm
	PDIP (20)	22.48 mm × 6.35 mm
	TSSOP (20)	6.50 mm × 4.40 mm
	TVSOP (20)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>9 Detailed Description</b> .....	<b>8</b>
<b>2 Applications</b> .....	<b>1</b>	9.1 Overview .....	8
<b>3 Description</b> .....	<b>1</b>	9.2 Functional Block Diagrams .....	8
<b>4 Simplified Schematics</b> .....	<b>1</b>	9.3 Feature Description .....	9
<b>5 Revision History</b> .....	<b>2</b>	9.4 Device Functional Modes .....	9
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	<b>10 Application and Implementation</b> .....	<b>10</b>
<b>7 Specifications</b> .....	<b>4</b>	10.1 Application Information .....	10
7.1 Absolute Maximum Ratings .....	4	10.2 Typical Application .....	10
7.2 Handling Ratings .....	4	<b>11 Power Supply Recommendations</b> .....	<b>11</b>
7.3 Recommended Operating Conditions .....	4	<b>12 Layout</b> .....	<b>11</b>
7.4 Thermal Information .....	5	12.1 Layout Guidelines .....	11
7.5 Electrical Characteristics .....	5	12.2 Layout Example .....	11
7.6 Timing Requirements .....	5	<b>13 Device and Documentation Support</b> .....	<b>12</b>
7.7 Switching Characteristics .....	6	13.1 Related Links .....	12
7.8 Noise Characteristics .....	6	13.2 Trademarks .....	12
7.9 Operating Characteristics .....	6	13.3 Electrostatic Discharge Caution .....	12
7.10 Typical Characteristics .....	6	13.4 Glossary .....	12
<b>8 Parameter Measurement Information</b> .....	<b>7</b>	<b>14 Mechanical, Packaging, and Orderable Information</b> .....	<b>12</b>

## 5 Revision History

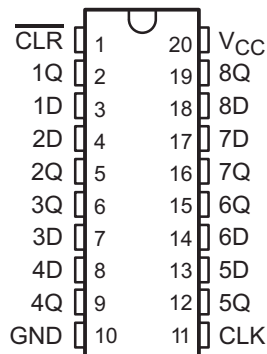
### Changes from Revision E (April 2002) to Revision F

Page

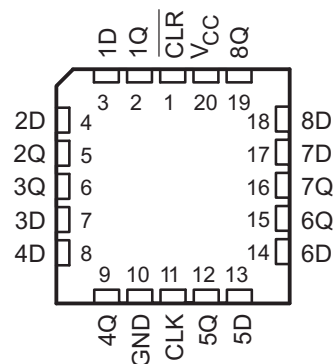
• Updated document to new TI data sheet standards. ....	1
• Deleted Ordering Information table. ....	1
• Added Applications. ....	1
• Added Pin Functions table. ....	3
• Added Handling Ratings table. ....	4
• Changed MAX operating temperature to 125°C in Recommended Operating Conditions table. ....	4
• Added Typical Characteristics section. ....	6
• Added Detailed Description section. ....	8
• Added Application and Implementation section. ....	10

## 6 Pin Configuration and Functions

SN54AHCT273 . . . J OR W PACKAGE  
SN74AHCT273 . . . DB, DGV, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54AHCT273 . . . FK PACKAGE  
(TOP VIEW)



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{\text{CLR}}$	I	Clear Pin
2	1Q	O	1Q Output
3	1D	I	1D Input
4	2D	I	2D Input
5	2Q	O	2Q Output
6	3Q	O	3Q Output
7	3D	I	3D Input
8	4D	I	4D Input
9	4Q	O	4Q Output
10	GND	—	Ground Pin
11	CLK	I	Clock Pin
12	5Q	O	5Q Output
13	5D	I	5D Input
14	6D	I	6D Input
15	6Q	O	6Q Output
16	7Q	O	7Q Output
17	7D	I	7D Input
18	8D	I	8D Input
19	8Q	O	8Q Output
20	$V_{CC}$	—	Power Pin

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	–0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	–0.5	7	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	–0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		–20 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		±20 mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±25 mA
Continuous current through V <sub>CC</sub> or GND				±75 mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 7.2 Handling Ratings

		MIN	MAX	UNIT
T <sub>stg</sub>	Storage temperature range	–65	150	°C
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>		V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>		
		0	2000	
		0	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN54AHCT273 <sup>(2)</sup>		SN74AHCT273		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		–8		–8	mA
I <sub>OL</sub>	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T <sub>A</sub>	Operating free-air temperature	–55	125	–40	125	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI Application Report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.
- (2) Product Preview.

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AHCT273						UNIT
		DB	DW	DGV	N	NS	PW	
		20 PINS						
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	98.7	81.8	118.1	53.9	79.4	104.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	60.4	47.8	33.4	38.8	45.9	38.8	
R <sub>θJB</sub>	Junction-to-board thermal resistance	56.9	49.4	59.6	34.7	46.9	55.7	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	21.6	20.1	1.1	26.9	19.1	2.9	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	53.5	49.0	58.9	34.7	46.5	55.1	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, (SPRA953).

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHCT273 <sup>(1)</sup>		SN74AHCT273		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4		4.4	V	
	I <sub>OH</sub> = -8 mA		3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1	0.1	V	
	I <sub>OL</sub> = 8 mA				0.36		0.44	0.44		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1 <sup>(2)</sup>	±1	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND I <sub>O</sub> = 0	5.5 V			4		40	40	μA	
ΔI <sub>CC</sub> <sup>(3)</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	1.5	mA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2.5	10			10	pF	

(1) Product Preview.

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

(3) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## 7.6 Timing Requirements

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

			T <sub>A</sub> = 25°C		SN54AHCT273 <sup>(1)</sup>		SN74AHCT273		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	CL <sub>R</sub> low	5		6		6		ns
		CLK high or low	5		6.5		6.5		
t <sub>su</sub>	Setup time	Data before CLK↑	5		5		5		ns
		CL <sub>R</sub> before CLK↑	2.5		2.5		2.5		
t <sub>h</sub>	Hold time, data after CLK↑		0		0		0		ns

(1) Product Preview.

## 7.7 Switching Characteristics

 over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHCT273 <sup>(1)</sup>		SN74AHCT273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	75 <sup>(2)</sup>	120 <sup>(2)</sup>		65 <sup>(2)</sup>		65		MHz
			$C_L = 50\text{ pF}$	50	75		45		45		
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q	$C_L = 15\text{ pF}$		7.5 <sup>(2)</sup>	10 <sup>(2)</sup>	1 <sup>(2)</sup>	11.6 <sup>(2)</sup>	1	11.6	ns
$t_{\text{PLH}}$	CLK	Q	$C_L = 15\text{ pF}$		5.5 <sup>(2)</sup>	7.5 <sup>(2)</sup>	1 <sup>(2)</sup>	8.8 <sup>(2)</sup>	1	8.8	ns
$t_{\text{PHL}}$					5.8 <sup>(2)</sup>	8.2 <sup>(2)</sup>	1 <sup>(2)</sup>	10 <sup>(2)</sup>	1	10	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q	$C_L = 50\text{ pF}$		8.5	11	1	12.6	1	12.6	ns
$t_{\text{PLH}}$	CLK	Q	$C_L = 50\text{ pF}$		6.5	8.5	1	9.8	1	9.8	ns
$t_{\text{PHL}}$					6.8	9.2	1	11	1	11	
$t_{\text{sk(o)}}$			$C_L = 50\text{ pF}$			1 <sup>(3)</sup>				1	ns

(1) Product Preview.

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(3) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 7.8 Noise Characteristics

 $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ <sup>(1)</sup>

PARAMETER		SN74AHCT273			UNIT
		MIN	TYP	MAX	
$V_{\text{OL(P)}}$	Quiet output, maximum dynamic $V_{\text{OL}}$		7.6		V
$V_{\text{OL(V)}}$	Quiet output, minimum dynamic $V_{\text{OL}}$		-0.48		V
$V_{\text{OH(V)}}$	Quiet output, minimum dynamic $V_{\text{OH}}$	4.4			V
$V_{\text{IH(D)}}$	High-level dynamic input voltage	2			V
$V_{\text{IL(D)}}$	Low-level dynamic input voltage			0.8	V

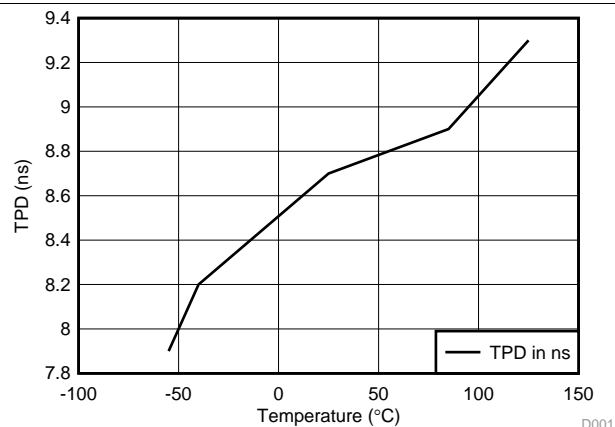
(1) Characteristics are for surface-mount packages only.

## 7.9 Operating Characteristics

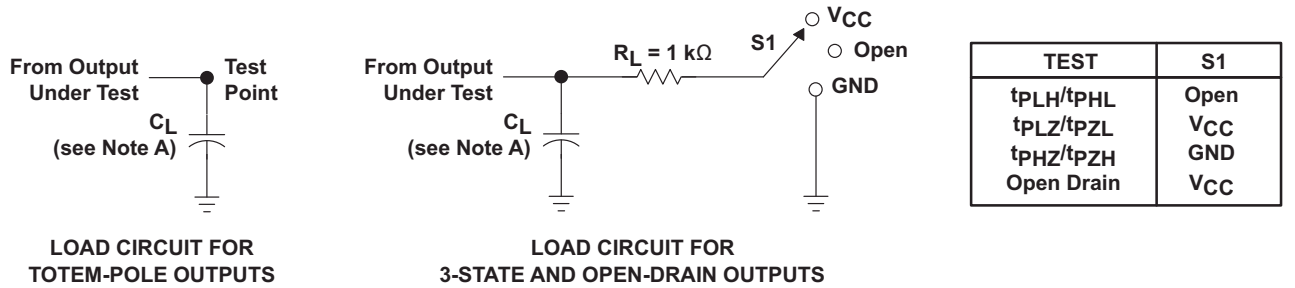
 $T_A = 25^\circ\text{C}$ 

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$	No load, $f = 1\text{ MHz}$	27	pF

## 7.10 Typical Characteristics

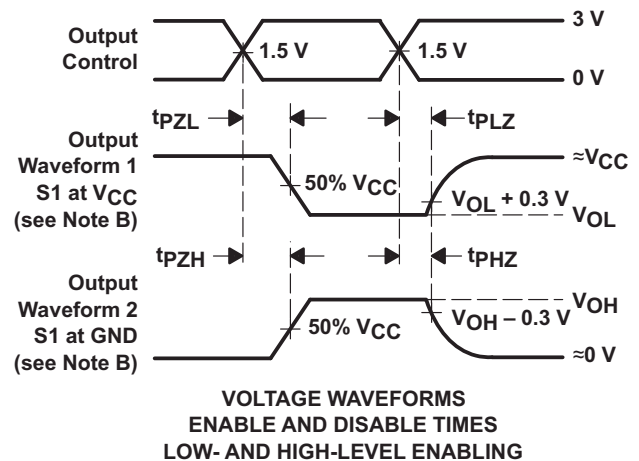
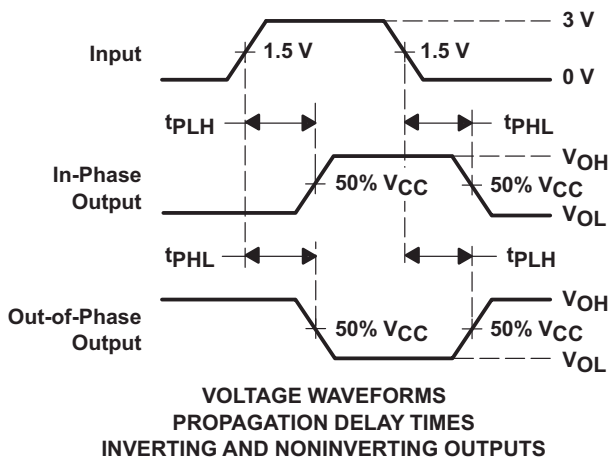
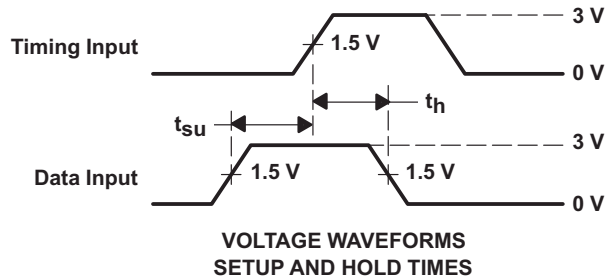
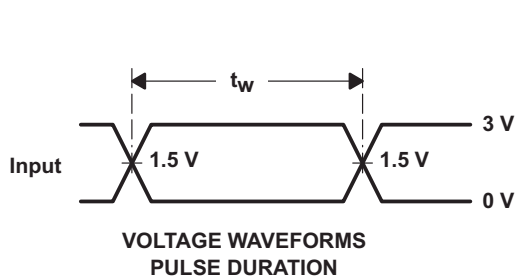

**Figure 1. TPD vs Temperature**

## 8 Parameter Measurement Information



LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ .
  - D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

## 9 Detailed Description

### 9.1 Overview

These circuits are positive-edge-triggered D-type flip-flops with a direct clear ( $\overline{\text{CLR}}$ ) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

The inputs are TTL compatible with  $V_{IL}$  at 0.8 V and  $V_{IH}$  at 2 V. This feature allows the use of these devices as up translators in a mixed 3.3 V to 5 V system environment.

### 9.2 Functional Block Diagrams

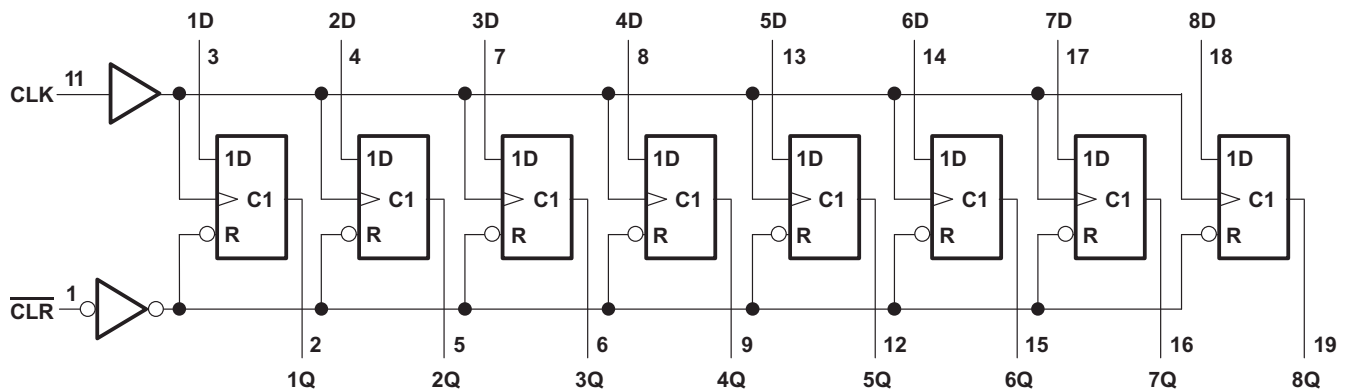


Figure 3. Logic Diagram (Positive Logic)

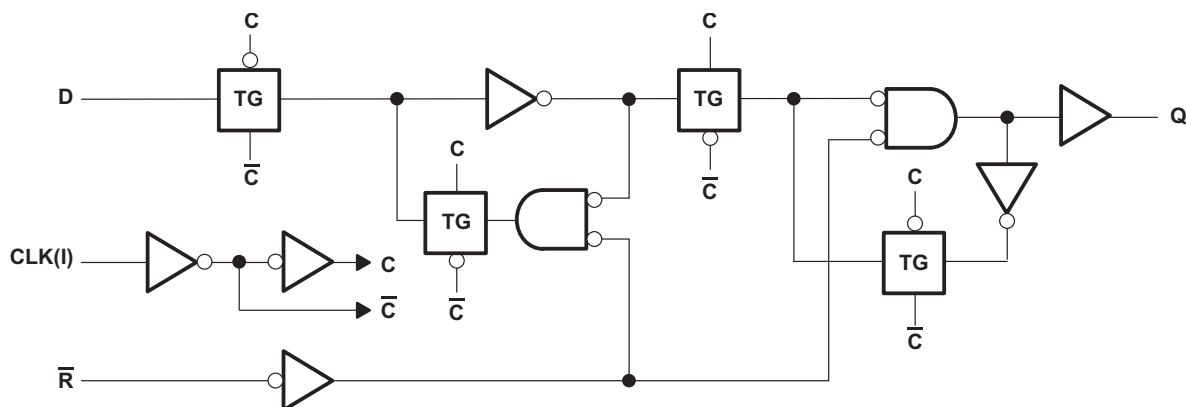


Figure 4. Logic Diagram, Each Flip-flop (Positive Logic)



### 9.3 Feature Description

- Allow up voltage translation from 3.3 V to 5 V
  - Inputs accept TTL voltage levels
- Slow edge rates minimize output ringing

### 9.4 Device Functional Modes

**Table 1. Function Table  
(Each Flip-flop)**

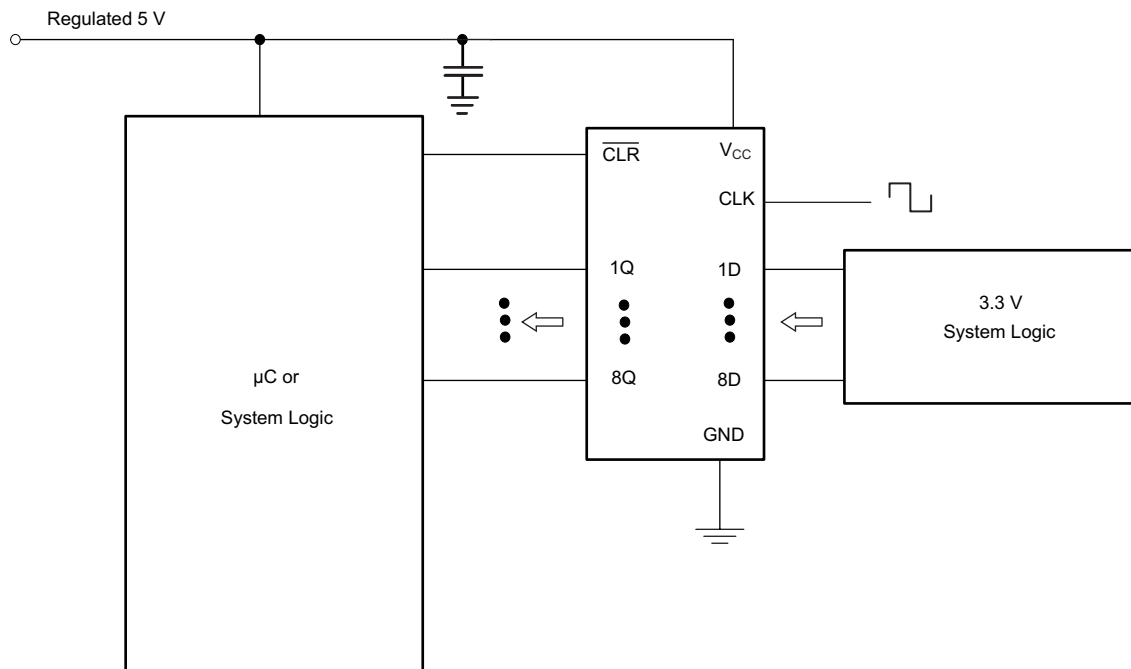
INPUTS			OUTPUT Q
$\overline{\text{CLR}}$	CLK	D	
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q <sub>0</sub>

## 10 Application and Implementation

### 10.1 Application Information

The SNx4AHCT273 is a low-drive CMOS device that can be used for a multitude of applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are TTL compatible. This feature makes it ideal for translating up from 3.3 V to 5 V. Figure 6 shows the reduction in ringing compared to higher drive parts such as AC.

### 10.2 Typical Application



**Figure 5. Typical Application Schematic**

#### 10.2.1 Design Requirements

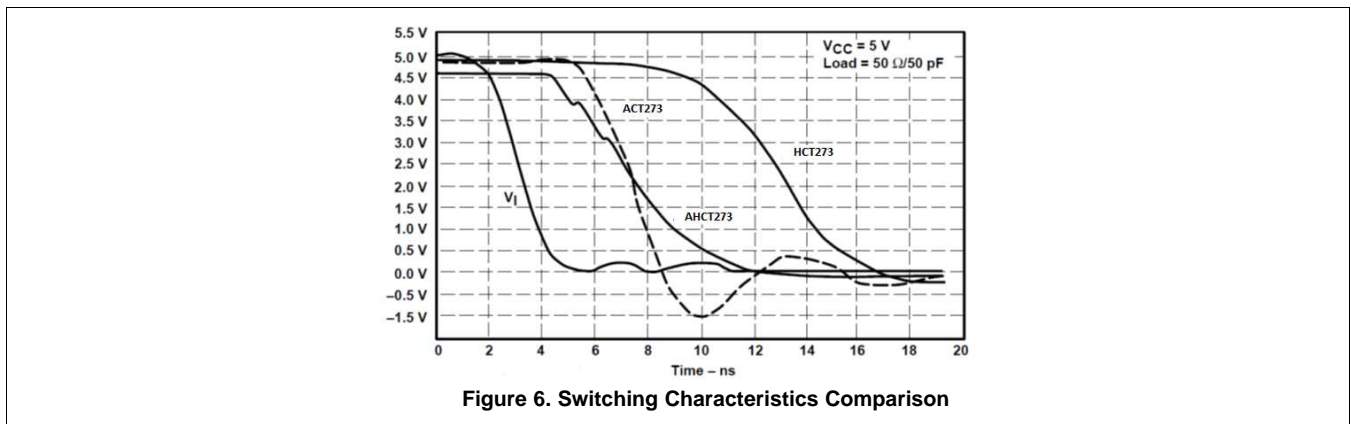
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 10.2.2 Detailed Design Procedure

1. Recommended input conditions
  - Rise time and fall time specs: See ( $\Delta t/\Delta V$ ) in the [Recommended Operating Conditions](#) table.
  - Specified High and low levels: See ( $V_{IH}$  and  $V_{IL}$ ) in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$
2. Recommend output conditions
  - Load currents should not exceed 25 mA per output and 75 mA total for the part
  - Outputs should not be pulled above  $V_{CC}$

## Typical Application (continued)

### 10.2.3 Application Curves



## 11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended. If there are multiple  $V_{CC}$  pins, 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

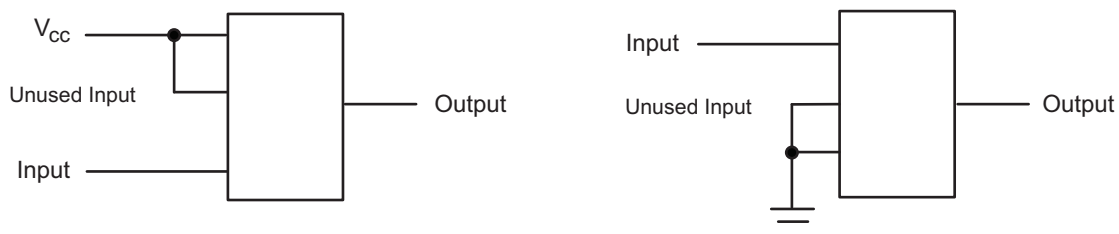
## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in [Figure 7](#) are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally inputs will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver.

### 12.2 Layout Example



## 13 Device and Documentation Support

### 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHCT273	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74AHCT273	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 13.2 Trademarks

All trademarks are the property of their respective owners.

### 13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCT273DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB273	<a href="#">Samples</a>
SN74AHCT273DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB273	<a href="#">Samples</a>
SN74AHCT273DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT273	<a href="#">Samples</a>
SN74AHCT273DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT273	<a href="#">Samples</a>
SN74AHCT273DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT273	<a href="#">Samples</a>
SN74AHCT273N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHCT273N	<a href="#">Samples</a>
SN74AHCT273NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT273	<a href="#">Samples</a>
SN74AHCT273PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB273	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT273DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHCT273DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHCT273NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT273DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74AHCT273DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHCT273NSR	SO	NS	20	2000	367.0	367.0	45.0



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

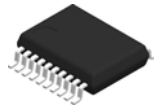
PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

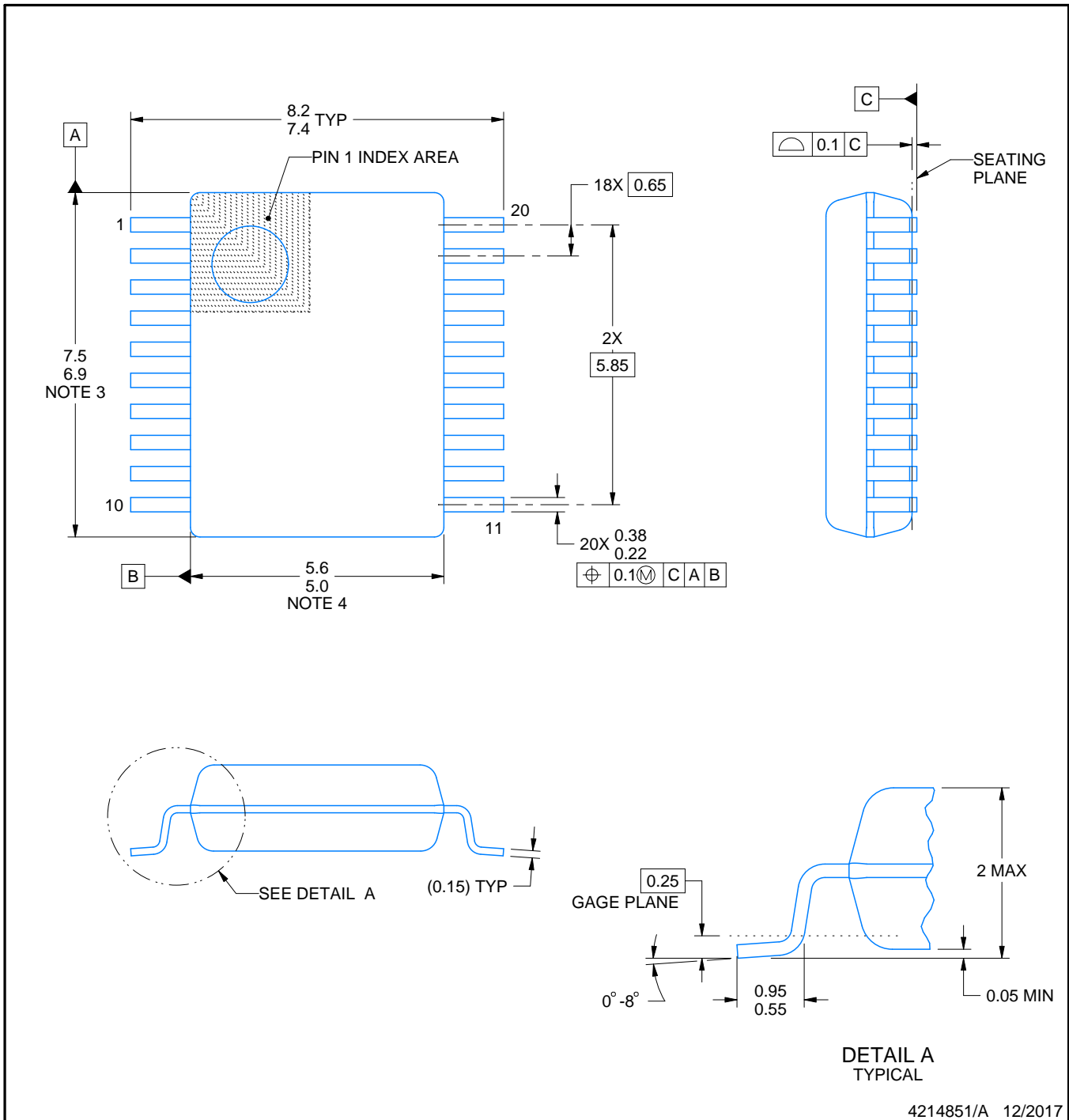
# DB0020A



# PACKAGE OUTLINE

## TSSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/A 12/2017

# EXAMPLE BOARD LAYOUT

DB0020A

TSSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214851/A 12/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

TSSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/A 12/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2019, Texas Instruments Incorporated