

## SN74AUP1T34-Q1 1-Bit Unidirectional Voltage-Level Translator

### 1 Features

- Qualified for Automotive Applications
  - AEC-Q100 Qualified
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  Ambient Operating Temperature
  - Device HBM ESD Classification Level 3A
  - Device CDM ESD Classification Level C5
- Wide Operating VCC Range of 0.9 V to 3.6 V
- Balanced Propagation Delays:  $t_{\text{PLH}} = t_{\text{PHL}}$  (1.8-V to 3.3-V Translation Typical)
- Low Static-Power Consumption: Maximum of 5- $\mu\text{A}$  ICC
- $\pm 6\text{-mA}$  Output Drive at 3 V
- $I_{\text{off}}$  Supports Partial Power-Down-Mode Operation
- VCC Isolation Feature – If  $V_{\text{CCA}}$  Input Is at GND, B Port Is in the High-Impedance state
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input
- ESD Protection Exceeds JESD 22
- 5000-V Human-Body Model (AEC-Q100-002-E)
- Latch-Up Performance Meets 100 mA Per Q100-004-D

### 2 Applications

- Automotive
- Enterprise
- Industrial
- Personal Electronics
- Telecommunications

### 3 Description

The SN74AUP1T34-Q1 device is a 1-bit noninverting translator that uses two separate configurable power-supply rails. It is a unidirectional translator from A to B. The A port is designed to track  $V_{\text{CCA}}$ .  $V_{\text{CCA}}$  accepts supply voltages from 0.9 V to 3.6 V. The B port is designed to track  $V_{\text{CCB}}$ .  $V_{\text{CCB}}$  accepts supply voltages from 0.9 V to 3.6 V. This allows for low-voltage translation between 1-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes. The SN74AUP1T34-Q1 is also fully specified for partial-power-down applications using  $I_{\text{off}}$ . The  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

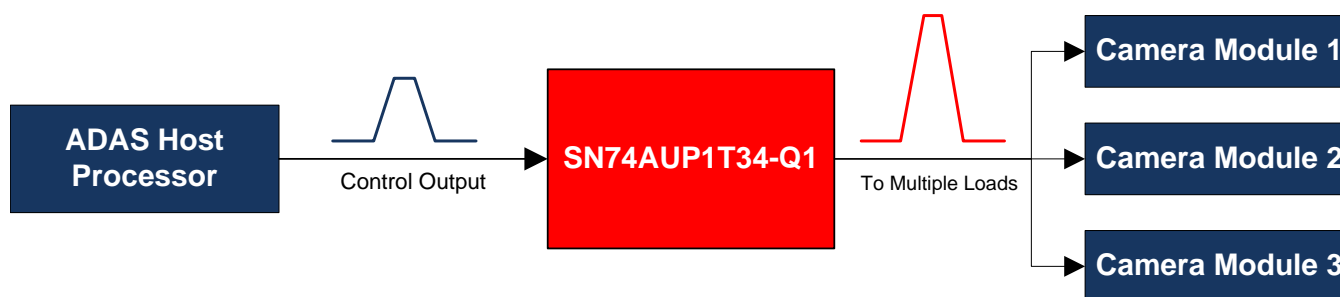
The VCC isolation feature ensures that if  $V_{\text{CCA}}$  input is at GND, the B port is in the high-impedance state. If  $V_{\text{CCB}}$  input is at GND, any input to the A side does not cause the leakage current even floating.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AUP1T34-Q1	SC70 (5)	2.00 mm x 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Example Application Diagram



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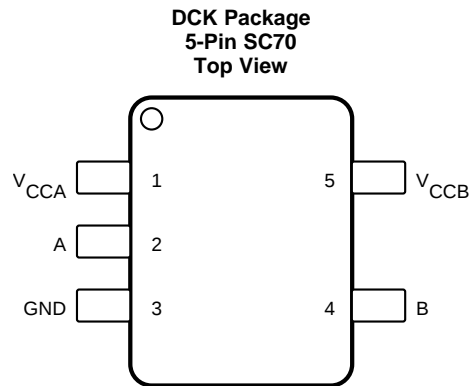
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Original (December 2013) to Revision A</b>	<b>Page</b>
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....	<b>1</b>
• Removed <i>Ordering Information</i> table .....	<b>1</b>

## 5 Pin Configuration and Functions



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
A	2	I	Input Port. Referenced to $V_{CCA}$ .
B	4	O	Output Port. Referenced to $V_{CCB}$ .
GND	3	—	Ground.
$V_{CCA}$	1	—	Input Port DC Power Supply.
$V_{CCB}$	5	—	Output Port DC Power Supply.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CCA}$ , $V_{CCB}$	Supply voltage		-0.3	4	V
$V_I$	Input voltage		-0.5	4.6	V
$V_O$	Voltage applied to any output in the high-impedance or power-off state		-0.5	4.6	V
	Voltage applied to any output in the high or low state		-0.5	4.6	
$I_{IK}$	Input clamp current	$V_I < 0$		-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$		-50	mA
$I_O$	Continuous output current			±50	mA
	Continuous current through $V_{CCA}$ or GND			±100	mA
$T_{stg}$	Storage temperature		-65	150	°C

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup> , Classification 3A	5000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> , Classification C5	750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCCA	VCCB	MIN	MAX	UNIT
$V_{CCA}, V_{CCB}$ Supply voltage				0.9	3.6	V
$V_{IH}$ High-level input voltage		0.9 V to 1.95 V	0.9 V to 1.95 V	$0.65 \times V_{CCA}$	1.6	V
		2.3 V to 2.7 V	0.9 V to 3.6 V			
		3 V to 3.6 V	0.9 V to 3.6 V	2		
$V_{IL}$ Low-level input voltage		0.9 V	0.9 V to 1.95 V	$0.3 \times V_{CCA}$	0.7	V
		1 V to 1.95 V	0.9 V to 1.95 V	$0.35 \times V_{CCA}$		
		2.3 V to 2.7 V	0.9 V to 3.6 V			
		3 V to 3.6 V	0.9 V to 3.6 V	0.9		
$\Delta t/\Delta v$ Input transition rise or fall rate		3 V to 3.6 V	0.9 V to 3.6 V		200	ns/V
$T_A$ Operating free-air temperature				-40	125	°C
$V_{OH}$	$I_{OH} = -100 \mu A$ $I_{OH} = -0.25 mA$ $I_{OH} = -1.5 mA$ $I_{OH} = -2 mA$ $I_{OH} = -3 mA$ $I_{OH} = -6 mA$	$V_I = V_{IH}$	0.9 V to 3.6 V	0.9 V to 3.6 V	$V_{CCB} - 0.2$	V
			0.9 V to 1 V	0.9 V to 1 V	$0.75 \times V_{CCB}$	
			1.2 V	1.2 V	1	
			1.65 V	1.65 V	1.32	
			2.3 V	2.3 V	1.9	
			3 V	3 V	2.72	
$V_{OL}$	$I_{OL} = 100 \mu A$ $I_{OL} = 0.25 mA$ $I_{OL} = 1.5 mA$ $I_{OL} = 2 mA$ $I_{OL} = 3 mA$ $I_{OL} = 6 mA$	$V_I = V_{IL}$	0.9 V to 3.6 V	0.9 V to 3.6 V	0.1	V
			0.9 V to 1 V	0.9 V to 1 V	0.1	
			1.2 V	1.2 V	$0.3 \times V_{CCB}$	
			1.65 V	1.65 V	0.31	
			2.3 V	2.3 V	0.31	
			3 V	3 V	0.31	
$I_i$ Control inputs	$V_i = V_{CCA}$ or GND	0.9 V to 3.6 V	0.9 V to 3.6 V		$\pm 1$	$\mu A$
$I_{off}$ A or B port	$V_I$ or $V_O = 0$ to 3.6 V	0 V	0 V to 3.6 V		$\pm 5$	$\mu A$
		0 V to 3.6 V	0 V		$\pm 5$	
$I_{CCA}$	$V_I = V_{CCI}$ or GND, $I_O = 0$ mA	0.9 V to 3.6 V	0.9 V to 3.6 V		2.7	$\mu A$
		0.9 V to 3.6 V	VCCA		2	
		0 V	0 V to 3.6 V		1	
		0 V to 3.6 V	0 V		1	
$I_{CCB}$	$V_I = V_{CCI}$ or GND, $I_O = 0$ mA	0.9 V to 3.6 V	0.9 V to 3.6 V		2.7	$\mu A$
		0.9 V to 3.6 V	VCCA		2	
		0 V	0 V to 3.6 V		1	
		0 V to 3.6 V	0 V		1	
$I_{CCA} + I_{CCB}$	$V_I = V_{CCI}$ or GND, $I_O = 0$ mA	0.9 V to 3.6 V	0.9 V to 3.6 V		5.4	$\mu A$
$C_{io}$ A or B port		3.3 V	3.3 V		4	pF

### 6.4 Thermal Information

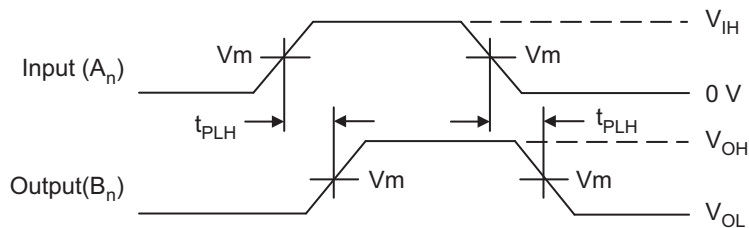
THERMAL METRIC <sup>(1)</sup>	SN74AUP1T34-Q1		UNIT
	DCK (SC70)		
	5 PINS		
$R_{\theta JA}$ Junction-to-ambient thermal resistance	301.9		°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	113		°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	79.1		°C/W
$\psi_{JT}$ Junction-to-top characterization parameter	3.9		°C/W
$\psi_{JB}$ Junction-to-board characterization parameter	78.3		°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

### 6.5 AC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	C <sub>L</sub>	VCCA	VCCB = 0.9 V		VCCB = 1.2 V		VCCB = 1.65 V		VCCB = 2.3 V		VCCB = 3 V		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
t <sub>PLH</sub> /t <sub>PHL</sub>	5 pF	0.9 V	25		18		16.2		16.3		16.8		ns
	5 pF	1.2 V		42.5		24.9		23.2		22.6		22.5	
	5 pF	1.65 V		40		10.7		8.84		8.08		7.88	
	5 pF	2.3 V		41.3		8.02		5.73		4.92		4.2	
	5 pF	3 V		42.5		7.61		4.5		3.65		3.39	
t <sub>PLH</sub> /t <sub>PHL</sub>	10 pF	0.9 V	28.9		19.8		17.9		18		18.5		ns
	10 pF	1.2 V		43.22		12.33		9.57		8.81		8.61	
	10 pF	1.65 V		40.44		9.21		6.57		5.6		4.73	
	10 pF	2.3 V		41.56		8.3		5.54		4.42		4.07	
	10 pF	3 V		42.81		7.87		4.8		3.8		3.36	
t <sub>PLH</sub> /t <sub>PHL</sub>	15 pF	0.9 V	30.6		21.6		19.6		19.7		20.3		ns
	15 pF	1.2 V		43.87		16.2		11.8		11		11	
	15 pF	1.65 V		40.78		14.7		8.8		7.1		6.4	
	15 pF	2.3 V		41.79		14.9		7.6		5.88		5.27	
	15 pF	3 V		43.09		16.2		6.98		5.4		4.7	
t <sub>PLH</sub> /t <sub>PHL</sub>	30 pF	0.9 V	32.1		21.3		18.7		18		18.3		ns
	30 pF	1.2 V		45.65		15.1		12.37		11.61		11.41	
	30 pF	1.65 V		41.72		12.18		8.15		6.94		6.1	
	30 pF	2.3 V		42.44		12.35		7.25		5.55		4.97	
	30 pF	3 V		43.69		11.6		6.92		4.95		4.35	



$$V_{MI} = V_{IH}/2; V_{MO} = V_{CCB}/2$$

$$t_R = t_F = 2.0 \text{ ns, } 10\% \text{ to } 90\%; f = 1 \text{ MHz; } t_W = 500 \text{ ns}$$

Figure 1. Waveform 1 - Propagation Delays

### 6.6 Typical Characteristics

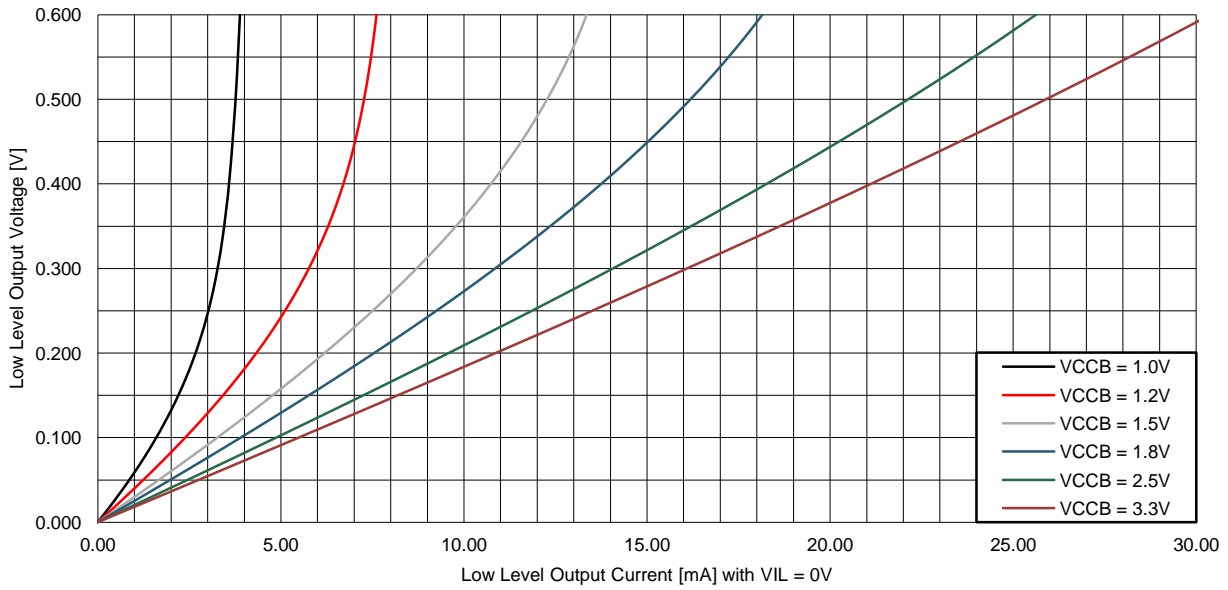
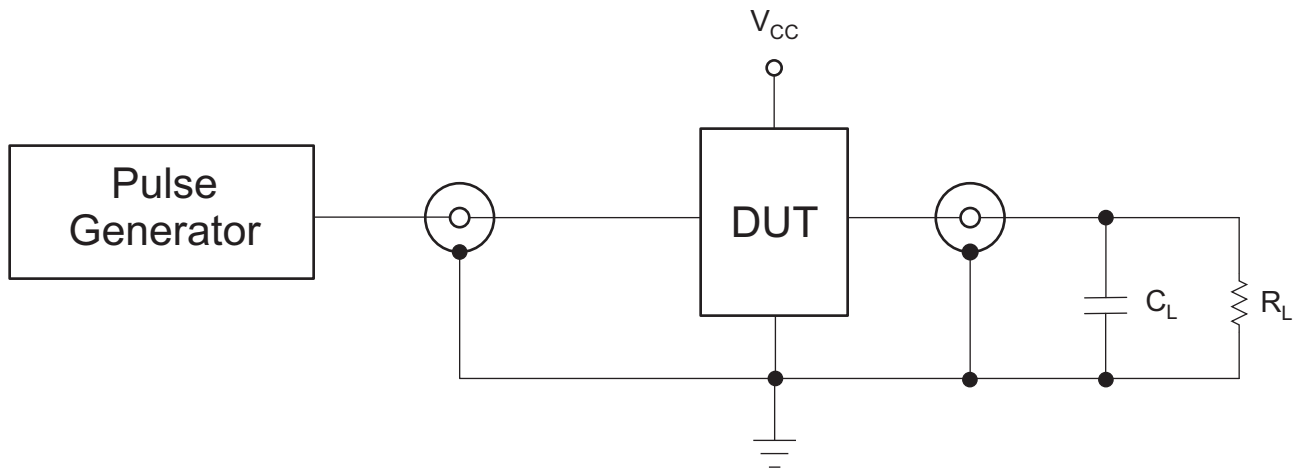


Figure 2. Low Level Output Voltage vs Low Level Output Current

### 7 Parameter Measurement Information



**TEST**

$t_{PLH}$ ,  $t_{PHL}$

$C_L$  = 5 pF, 10 pF, 15 pF, 30 pF or equivalent (includes probe and jig capacitance)

$R_L$  = 1 M $\Omega$  or equivalent

$Z_{OUT}$  of pulse generator = 50  $\Omega$

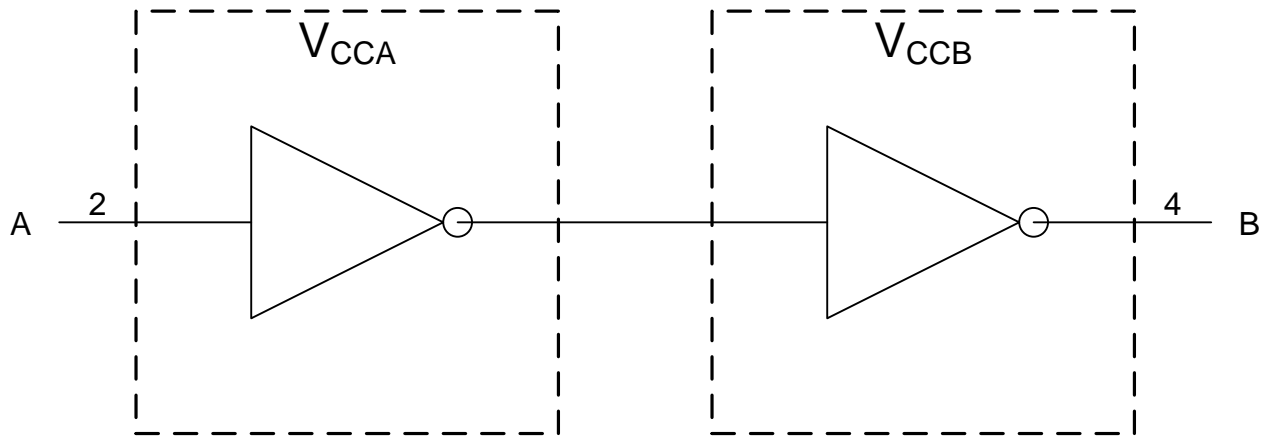
Figure 3. AC (Propagation Delay) Test Circuit

## 8 Detailed Description

### 8.1 Overview

The SN74AUP1T34-Q1 is a unidirectional, single-bit, dual-supply, noninverting voltage-level translator. Pin A, which is referenced to  $V_{CCA}$ , receives the signal that is to be level translated. Pin B, which is referenced to  $V_{CCB}$ , transmits the level translated signal. Both supply pins  $V_{CCA}$  and  $V_{CCB}$  support a voltage range from 0.9 V to 3.6 V.

### 8.2 Functional Block Diagram



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### 8.3 Feature Description

#### 8.3.1 Fully Configurable Dual-Rail Design

Both  $V_{CCA}$  and  $V_{CCB}$  can be supplied at any voltage from 0.9 V to 3.6 V, making the device suitable for translating between any of the voltage nodes (1 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V).

#### 8.3.2 Partial-Power-Down Mode Operation

$I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the SN74AUP1T34-Q1 when it is powered down. This can occur in applications where subsections of a system are powered down (partial-power-down) to reduce power consumption.

#### 8.3.3 $V_{CC}$ Isolation

The  $V_{CC}$  isolation feature ensures that if either  $V_{CCA}$  or  $V_{CCB}$  are at GND (or < 0.4 V), both ports A and B are set to a high-impedance state, preventing false logic levels from being presented to either bus.

#### 8.3.4 Input Hysteresis

Input hysteresis allows the input to support slew rates as slow as 200 ns/V, improving switching noise immunity.

### 8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74AUP1T34-Q1.

Table 1. Function Table

INPUT	OUTPUT
A PORT	B PORT
L	L
H	H

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74AUP1T34-Q1 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

### 9.2 Typical Application

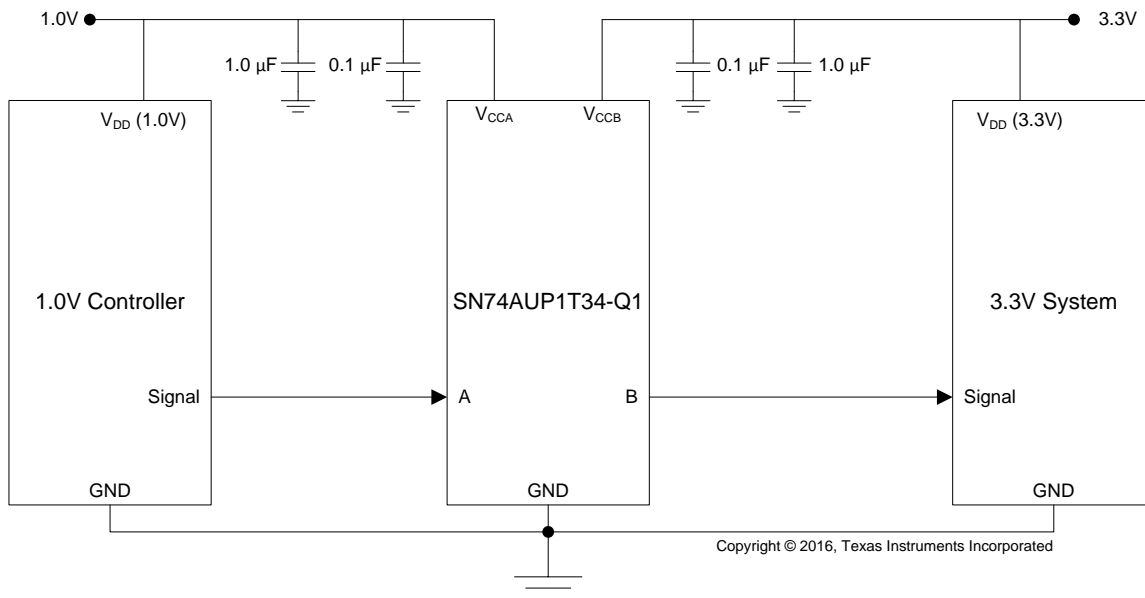


Figure 4. Typical Application Example

#### 9.2.1 Design Requirements

Table 2 lists the design requirements of the SN74AUP1T34-Q1.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0.9 V to 3.6 V
Output Voltage Range	0.9 V to 3.6 V

#### 9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AUP1T34-Q1 device to determine the input voltage range. For a valid logic-high, the value must exceed the  $V_{IH}$  of the input port. For a valid logic low the value must be less than the  $V_{IL}$  of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AUP1T34-Q1 device is driving to determine the output voltage range.



### 9.2.3 Application Curve

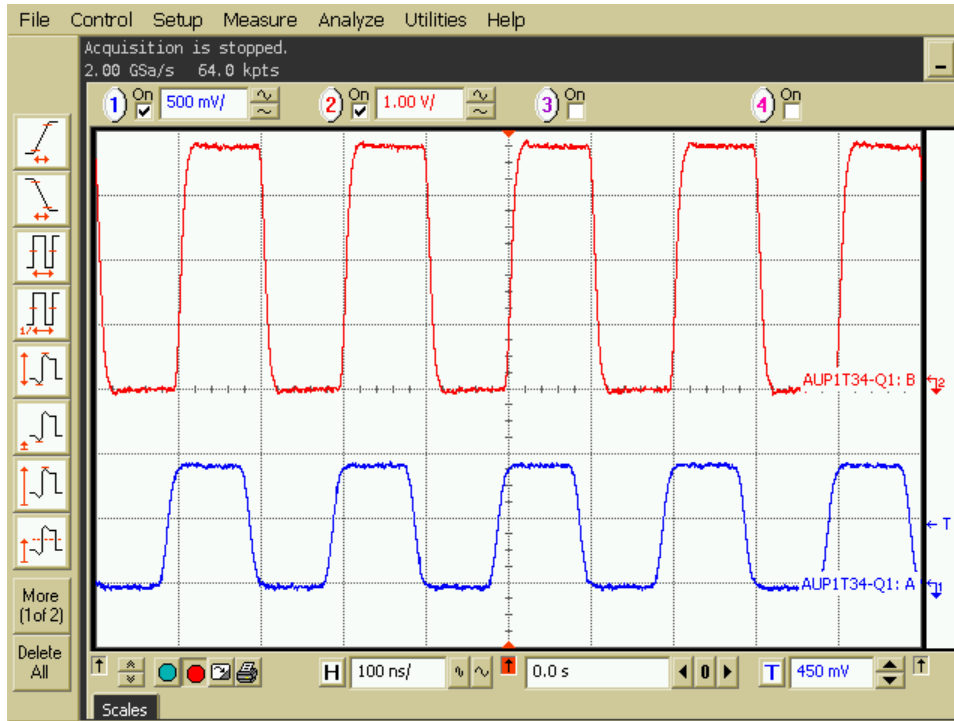


Figure 5. 10 MHz Up Translation (0.9 V to 3.6 V)

## 10 Power Supply Recommendations

Connect ground before applying either  $V_{CCA}$  or  $V_{CCB}$ . There is no specific power sequence requirement for the SN74AUP1T34.  $V_{CCA}$  or  $V_{CCB}$  may be powered up first, and  $V_{CCA}$  or  $V_{CCB}$  may be powered down first.

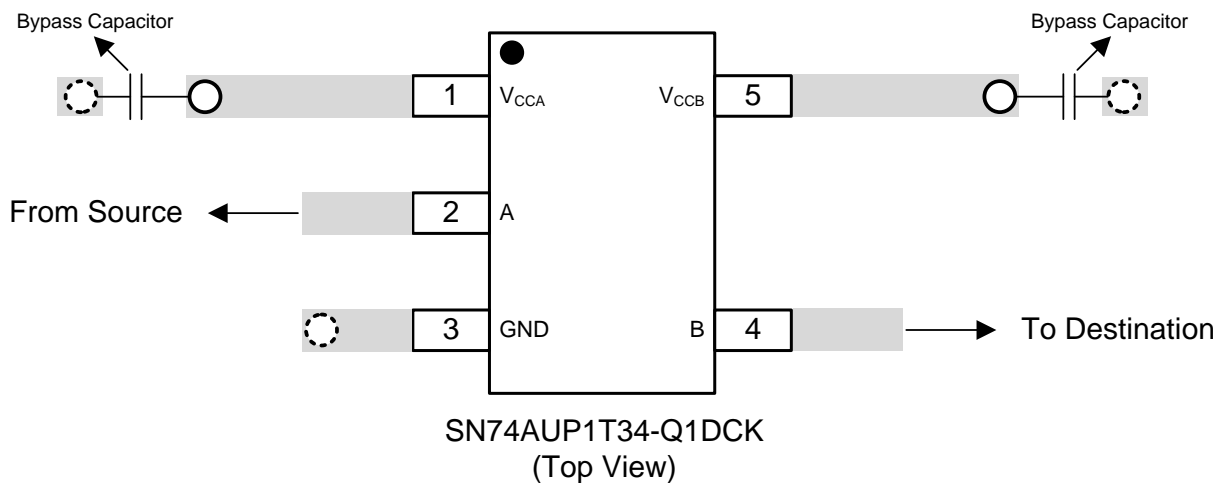
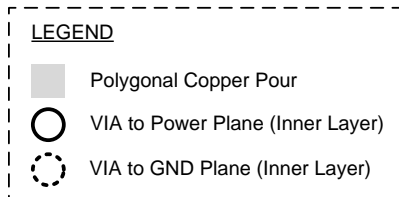
## 11 Layout

### 11.1 Layout Guidelines

To ensure reliability of the device, TI recommends following common printed-circuit board layout guidelines.

- Bypass capacitors must be used on power supplies.
- Short trace lengths must be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors helps adjust rise and fall times of signals depending on the system requirements.

### 11.2 Layout Example



**Figure 6. Example Layout**

## 12 Device and Documentation Support

### 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.2 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1T34QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U4E	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74AUP1T34-Q1 :**

- Catalog: [SN74AUP1T34](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T34QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1T34QDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.



DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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