74AUP1T32Low-power 2-input OR-gate with voltage-level translatorRev. 1 - 23 November 2017Product data sheet

1 General description

The 74AUP1T32 provides the single 2-input OR function. This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 2.3 V to 3.6 V.

The 74AUP1T32 is designed for logic-level translation applications with input switching levels that accept 1.8 V low-voltage CMOS signals, while operating from either a single 2.5 V or 3.3 V supply voltage.

The wide supply voltage range ensures normal operation as battery voltage drops from 3.6 V to 2.3 V.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Schmitt trigger inputs make the circuit tolerant to slower input rise and fall times across the entire V_{CC} range.

2 Features and benefits

- Wide supply voltage range from 2.3 V to 3.6 V
- High noise immunity
- ESD protection:
 - HBM JESD22-A114F Class 3A exceeds 5000 V
 - CDM JESD22-C101E exceeds 1000 V
- Low static power consumption; $I_{CC} = 1.5 \ \mu A$ (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

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3 Ordering information

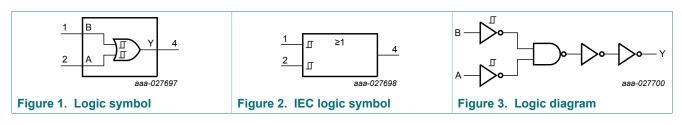
Table 1. Ordering information										
Type number	Package									
	Temperature range	Name	Description	Version						
74AUP1T32GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1						
74AUP1T32GX	-40 °C to +125 °C	X2SON5	X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 × 0.8 × 0.35 mm	SOT1226						

4 Marking

Table 2. Marking							
Type number	Marking code ^[1]						
74AUP1T32GW	5B						
74AUP1T32GX	5B						

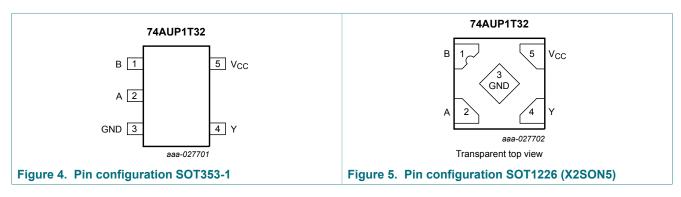
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5 Functional diagram



6 **Pinning information**

6.1 Pinning



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6.2 Pin description

Table 3. Pin description								
Symbol	Pin	Description						
В	1	data input						
A	2	data input						
GND	3	ground (0 V)						
Y	4	data output						
V _{CC}	5	supply voltage						

Functional description 7

Table 4. Function table ^[1]

Input	Output	
A	В	Y
L	L	L
L	Н	Н
Н	L	Н
Н	Н	Н

[1] H = HIGH voltage level;

L = LOW voltage level.

Limiting values 8

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+4.6	V
I _{IK}	input clamping current	V ₁ < 0 V		-50	-	mA
VI	input voltage		[1]	-0.5	+4.6	V
I _{OK}	output clamping current	V _O < 0 V		-50	-	mA
Vo	output voltage	Active mode and Power-down mode	[1]	-0.5	+4.6	V
lo	output current	V_{O} = 0 V to V_{CC}		-	±20	mA
I _{CC}	supply current			-	50	mA
I _{GND}	ground current			-50	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed. [2] For TSSOP5 packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

For X2SON5 packages: above 118 °C the value of Ptot derates linearly with 7.8 mW/K.

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9 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Мах	Unit
V _{CC}	supply voltage		2.3	3.6	V
VI	input voltage		0	3.6	V
Vo	output voltage	Active mode	0	V _{CC}	V
		Power-down mode; $V_{CC} = 0 V$	0	3.6	V
T _{amb}	ambient temperature		-40	+125	°C

10 Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T _{amb} = 2	5 °C				1	
V _{T+}	positive-going threshold	V_{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
	voltage	V _{CC} = 3.0 V to 3.6 V	0.75	-	1.16	V
V _{T-}	negative-going threshold	V_{CC} = 2.3 V to 2.7 V	0.35	-	0.60	V
	voltage	V _{CC} = 3.0 V to 3.6 V	0.50	-	0.85	V
V _H	hysteresis voltage	$(V_{H} = V_{T+} - V_{T-})$				
		V _{CC} = 2.3 V to 2.7 V	0.23	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.25	-	0.56	V
V _{OH}	HIGH-level output voltage	$V_{I} = V_{T+}$ or V_{T-}				
		I_{O} = -20 µA; V_{CC} = 2.3 V to 3.6 V	V _{CC} - 0.1	-	-	V
		$I_{\rm O}$ = -2.3 mA; $V_{\rm CC}$ = 2.3 V	2.05	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.9	-	-	V
		$I_{\rm O}$ = -2.7 mA; $V_{\rm CC}$ = 3.0 V	2.72	-	-	V
		I_{O} = -4.0 mA; V_{CC} = 3.0 V	2.6	-	-	V
V _{OL}	LOW-level output voltage	$V_{I} = V_{T+}$ or V_{T-}				
		I_{O} = 20 µA; V_{CC} = 2.3 V to 3.6 V	-	-	0.10	V
		$I_{\rm O}$ = 2.3 mA; $V_{\rm CC}$ = 2.3 V	-	-	0.31	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.44	V
		I_{O} = 2.7 mA; V_{CC} = 3.0 V	-	-	0.31	V
		I_{O} = 4.0 mA; V_{CC} = 3.0 V	-	-	0.44	V
l _l	input leakage current	V_1 = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.1	μA
I _{OFF}	power-off leakage current	V_1 or V_0 = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.1	μA
ΔI _{OFF}	additional power-off leakage current	$V_1 \text{ or } V_0 = 0 \text{ V to } 3.6 \text{ V;}$ $V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	±0.1	μA
I _{CC}	supply current	V_I = GND or V_{CC} ; I_O = 0 A; V_{CC} = 2.3 V to 3.6 V	-	-	1.2	μA

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Low-power 2-input OR-gate with voltage-level translator

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
CI	input capacitance	V_{CC} = 0 V to 3.6 V; V _I = GND or V _{CC}	-	0.8	-	pF
Co	output capacitance	$V_{O} = GND; V_{CC} = 0 V$	-	1.7	-	pF
T _{amb} = -4	0 °C to +85 °C					
V _{T+}	positive-going threshold	V _{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
	voltage	V _{CC} = 3.0 V to 3.6 V	0.75	-	1.19	V
V _{T-}	negative-going threshold	V _{CC} = 2.3 V to 2.7 V	0.35	-	0.60	V
	voltage	V _{CC} = 3.0 V to 3.6 V	0.50	-	0.85	V
V _H	hysteresis voltage	$(V_{H} = V_{T^{+}} - V_{T^{-}})$				
		V _{CC} = 2.3 V to 2.7 V	0.10	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.15	-	0.56	V
V _{OH}	HIGH-level output voltage	$V_1 = V_{T+}$ or V_{T-}				
		I_{O} = -20 µA; V_{CC} = 2.3 V to 3.6 V	V _{CC} - 0.1	-	-	V
		$I_{\rm O}$ = -2.3 mA; $V_{\rm CC}$ = 2.3 V	1.97	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.85	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.67	-	-	V
		$I_{\rm O}$ = -4.0 mA; $V_{\rm CC}$ = 3.0 V	2.55	-	-	V
V _{OL}	LOW-level output voltage	$V_1 = V_{T+}$ or V_{T-}				
		I_{O} = 20 µA; V_{CC} = 2.3 V to 3.6 V	-	-	0.1	V
		I_0 = 2.3 mA; V_{CC} = 2.3 V	-	-	0.33	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I_0 = 2.7 mA; V_{CC} = 3.0 V	-	-	0.33	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.45	V
l _l	input leakage current	V_1 = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.5	μA
I _{OFF}	power-off leakage current	$V_1 \text{ or } V_0 = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V}$	-	-	±0.5	μA
Δl _{OFF}	additional power-off leakage current	$V_{I} \text{ or } V_{O} = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	±0.5	μA
I _{CC}	supply current	$V_{I} = GND \text{ or } V_{CC}; I_{O} = 0 \text{ A}; V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$	-	-	1.5	μA
Δl _{CC}	additional supply current	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V; } I_{O} = 0 \text{ A}$	1] -	-	0.6	μA
		$V_{\rm CC}$ = 3.0 V to 3.6 V; I _O = 0 A	2] _	-	10	μA

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Low-power 2-input OR-gate with voltage-level translator

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T _{amb} = -4	10 °C to +125 °C			<u> </u>	<u>I</u>	
V _{T+}	positive-going threshold	V _{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
	voltage	V _{CC} = 3.0 V to 3.6 V	0.75	-	1.19	V
V _{T-}	negative-going threshold	V _{CC} = 2.3 V to 2.7 V	0.33	-	0.64	V
	voltage	V _{CC} = 3.0 V to 3.6 V	0.46	-	0.85	V
V _H	hysteresis voltage	$(V_{H} = V_{T+} - V_{T-})$				
		V _{CC} = 2.3 V to 2.7 V	0.10	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.15	-	0.56	V
V _{OH}	HIGH-level output voltage	$V_{I} = V_{T+}$ or V_{T-}				
		I_{O} = -20 µA; V_{CC} = 2.3 V to 3.6 V	V _{CC} - 0.11	-	-	V
		$I_{\rm O}$ = -2.3 mA; $V_{\rm CC}$ = 2.3 V	1.77	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.67	-	-	V
		$I_{\rm O}$ = -2.7 mA; $V_{\rm CC}$ = 3.0 V	2.40	-	-	V
		$I_{\rm O}$ = -4.0 mA; $V_{\rm CC}$ = 3.0 V	2.30	-	-	V
V _{OL}	LOW-level output voltage	$V_{I} = V_{T+}$ or V_{T-}				
		I_{O} = 20 µA; V_{CC} = 2.3 V to 3.6 V	-	-	0.11	V
		$I_{\rm O}$ = 2.3 mA; $V_{\rm CC}$ = 2.3 V	-	-	0.36	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.50	V
		I_{O} = 2.7 mA; V_{CC} = 3.0 V	-	-	0.36	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.50	V
I	input leakage current	V_{I} = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.75	μA
I _{OFF}	power-off leakage current	V_1 or V_0 = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.75	μA
Δl _{OFF}	additional power-off leakage current	$V_{I} \text{ or } V_{O} = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	±0.75	μA
I _{CC}	supply current	$V_{I} = GND \text{ or } V_{CC}; I_{O} = 0 \text{ A};$ $V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$	-	-	3.5	μA
∆l _{CC}	additional supply current	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V; } I_{O} = 0 \text{ A}$	1] _	-	1.8	μA
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V; } I_{O} = 0 \text{ A}$	2] _	-	18	μA

11 Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions		25 °C		-40 °C to +125 °C			Unit
			Min	Тур ^[1]	Max	Min	Мах (85 °С)	Max (125 °C)	
V _{CC} = 2.	3 V to 2.7 V; V _I	= 1.65 V to 1.95 V							
t _{pd}	propagation	A, B to Y; see Figure 6	[2]						
	delay	C _L = 5 pF	2.0	3.3	5.0	0.5	6.8	7.5	ns
		C _L = 10 pF	2.4	3.9	5.7	1.0	7.9	8.7	ns
		C _L = 15 pF	2.7	4.3	6.4	1.0	8.7	9.6	ns
		C _L = 30 pF	3.5	5.5	8.0	1.5	10.8	11.9	ns
V _{CC} = 2.	3 V to 2.7 V; V _I	= 2.3 V to 2.7 V					1		
t _{pd}	propagation	A, B to Y; see Figure 6	[2]						
	delay	C _L = 5 pF	1.6	3.1	5.1	0.5	6.0	6.6	ns
		C _L = 10 pF	1.9	3.7	5.9	1.0	7.1	7.9	ns
		C _L = 15 pF	2.3	4.2	6.5	1.0	7.9	8.7	ns
		C _L = 30 pF	3.1	5.4	8.0	1.5	10.0	11.0	ns
V _{CC} = 2.	3 V to 2.7 V; V _I	= 3.0 V to 3.6 V					1	,	
t _{pd}	propagation	A, B to Y; see Figure 6	[2]						
	delay	C _L = 5 pF	1.2	2.9	4.5	0.5	5.5	6.1	ns
		C _L = 10 pF	1.6	3.5	5.3	1.0	6.5	7.2	ns
		C _L = 15 pF	1.9	3.9	5.9	1.0	7.4	8.2	ns
		C _L = 30 pF	2.8	5.1	7.4	1.5	9.5	10.5	ns
V _{CC} = 3.	0 V to 3.6 V; V _I	= 1.65 V to 1.95 V				1	1	,	
t _{pd}	propagation	A, B to Y; see Figure 6	[2]						
	delay	C _L = 5 pF	1.8	2.7	3.7	0.5	8.0	8.8	ns
		C _L = 10 pF	2.2	3.3	4.5	1.0	8.5	9.4	ns
		C _L = 15 pF	2.6	3.7	5.0	1.0	9.1	10.1	ns
		C _L = 30 pF	3.4	4.9	6.4	1.5	9.8	10.8	ns
V _{CC} = 3.	0 V to 3.6 V; V _I	= 2.3 V to 2.7 V	1				·		
t _{pd}	propagation	A, B to Y; see Figure 6	[2]						
	delay	C _L = 5 pF	1.5	2.6	3.9	0.5	5.3	5.9	ns
		C _L = 10 pF	1.9	3.2	4.7	1.0	6.1	6.8	ns
		C _L = 15 pF	2.2	3.7	5.3	1.0	6.8	7.5	ns
		C _L = 30 pF	2.9	4.8	6.8	1.5	8.5	9.4	ns

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Low-power 2-input OR-gate with voltage-level translator

Symbol	Parameter	rameter Conditions		25 °C		-40 °C to +125 °C			Unit
			Min	Typ ^[1]	Мах	Min	Мах (85 °С)	Max (125 °C)	
V _{CC} = 3.0	V to 3.6 V; V _I :	= 3.0 V to 3.6 V					1		
t _{pd}	propagation	A, B to Y; see <u>Figure 6</u> ^[2]							
	delay	C _L = 5 pF	1.1	2.6	4.0	0.5	4.7	5.2	ns
		C _L = 10 pF	1.5	3.1	4.8	1.0	5.7	6.3	ns
		C _L = 15 pF	1.8	3.6	5.4	1.0	6.2	6.9	ns
		C _L = 30 pF	2.6	4.7	7.0	1.5	7.8	8.6	ns
T _{amb} = 2	5 °C								
C _{PD}	power	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{\text{CC}}$ ^[3]							
	dissipation capacitance	V _{CC} = 2.3 V to 2.7 V	-	4	-	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	5	-	-	-	-	pF

[1] All typical values are measured at nominal V_{CC}. [2] t_{pd} is the same as t_{PLH} and t_{PHL} [3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW). P_D = C_{PD} x V_{CC}² x f₁ x N + Σ (C_L x V_{CC}² x f₀) where: f₁ = input frequency in MHz;

fo = output frequency in MHz;

 C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching; $\Sigma(C_L \times V_{CC}^2 \times f_0)$ = sum of the outputs.

Low-power 2-input OR-gate with voltage-level translator

11.1 Waveforms and test circuit

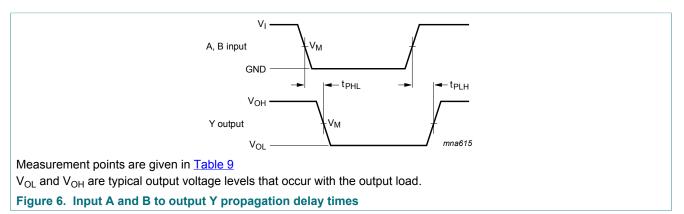


Table 9. Measurement points

Supply voltage	Output	Input				
V _{cc}	V _M	V _M	VI	t _r = t _f		
2.3 V to 3.6 V	$0.5 \times V_{CC}$	0.5 × V _I	1.65 V to 3.6 V	≤ 3.0 ns		

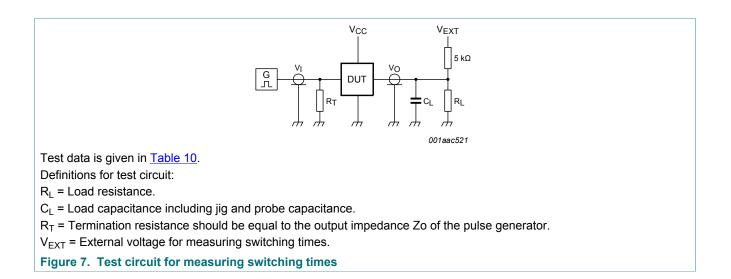


Table 10. Test data

Supply voltage	Load		V _{EXT}			
V _{cc}	CL	R _L ^[1]	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}	
2.3 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 k Ω or 1 M Ω	open	GND	$2 \times V_{CC}$	

[1] For measuring enable and disable times $R_L = 5 k\Omega$.

For measuring propagation delays, setup and hold times and pulse width R_L = 1 M Ω .

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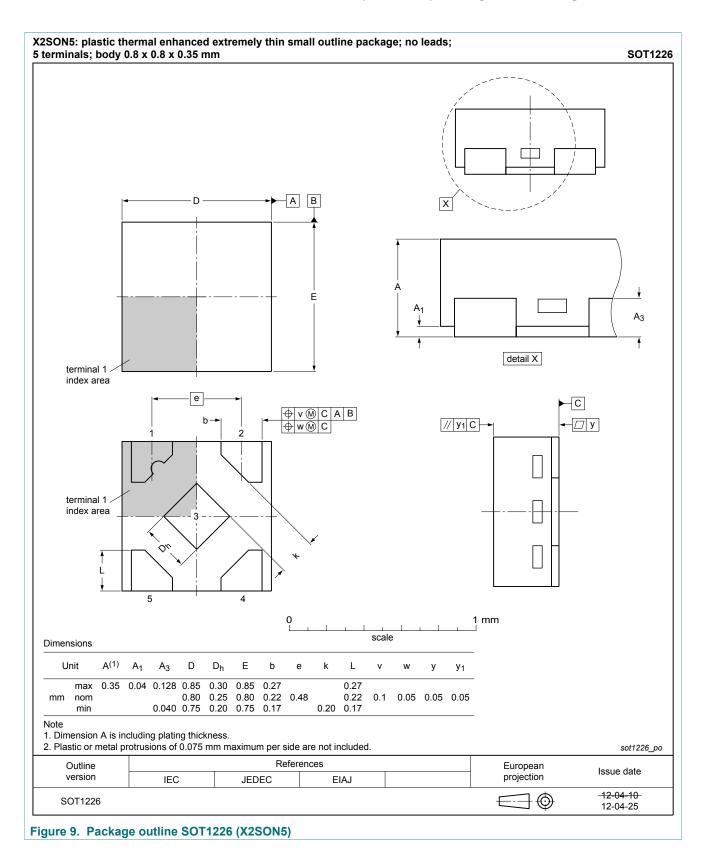
12 Package outline

	. pius	uc in			nall o	utline	раск	age; :	lead	s; bo	dy wic	ith 1.2	5 mn	1			S	DT353
		Ť							с	₹ ₹		E		X) () A			
		-		- z		4				A ₂	A ₁		Lp	(A ₃)	Α Α 4 7 9			
			•	e -	► <u> </u> b _p	- ⊕ w	/ M					detail	x	•				
IMENS	IONS (n	nm are		e ₁	Ì 0 ∟		, ∭ 1.: sca			3 mm		detail	X					
DIMENS	IONS (n A max.	nm are A1		e ₁	Ì 0 ∟		1.5		e	3 mm	HE	detail	×	v	w	У	Z ⁽¹⁾	θ
	Α		the orig	jinal din	0 ∟ nension	s)	1.5 sca	le	e 0.65		НЕ 2.25 2.0			v 0.3	w 0.1	y 0.1	Z(1) 0.60 0.15	θ 7° 0°
UNIT mm Note	A max. 1.1	A₁ 0.1 0	the orig A2 1.0 0.8	jinal din A3 0.15	0 0 0.30 0.15	s) c 0.25 0.08	D (1) 2.25 1.85	E(1) 1.35 1.15	0.65	e ₁	2.25	L	L _p 0.46				0.60	7°
UNIT mm Note	A max.	A₁ 0.1 0	the orig A2 1.0 0.8	jinal din A3 0.15	0 0 0.30 0.15	s) c 0.25 0.08	D (1) 2.25 1.85	E(1) 1.35 1.15	0.65 cluded.	e ₁	2.25	L	L _p 0.46		0.1	0.1	0.60 0.15	7° 0°
UNIT mm Note I. Plastic	A max. 1.1	A₁ 0.1 0	the orig A ₂ 1.0 0.8	jinal din A3 0.15	0 0 0.30 0.15	s) c 0.25 0.08	1.5 sca D(1) 2.25 1.85 side arc REFEI	E(1) 1.35 1.15 e not inc	0.65 cluded.	e ₁	2.25	L	L _p 0.46	0.3	0.1 PEAN	0.1	0.60	7° 0°

Figure 8. Package outline SOT353-1 (TSSOP5)

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Low-power 2-input OR-gate with voltage-level translator



13 Abbreviations

Table 11. Abbreviations						
Acronym	Description					
CDM	Charged Device Model					
CMOS	Complementary Metal-Oxide Semiconductor					
DUT	Device Under Test					
ESD	ElectroStatic Discharge					
НВМ	Human Body Model					

14 Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP1T32 v.1	20171123	Product data sheet	-	-

15 Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

Please consult the most recently issued document before initiating or completing a design. [1]

The term 'short data sheet' is explained in section "Definitions".

[2] [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

15.2 Definitions

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Low-power 2-input OR-gate with voltage-level translator

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Low-power 2-input OR-gate with voltage-level translator

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