74AHC164-Q100; 74AHCT164-Q100

8-bit serial-in/parallel-out shift register

Rev. 1 — 5 July 2013 Product data sheet

1. General description

The 74AHC164-Q100; 74AHCT164-Q100 shift register is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74AHC164-Q100; 74AHCT164-Q100 input signals are 8-bit serial through one of two inputs (DSA or DSB). Either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock input (CP). It enters into output Q0, which is a logical AND of the two data inputs (DSA and DSB). These data inputs existed one set-up time, prior to the rising clock edge.

A LOW-level on the master reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from −40 °C to +85 °C and from −40 °C to +125 °C
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- Input levels:
  - For 74AHC164-Q100: CMOS level
  - For 74AHCT164-Q100: TTL level
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC164-Q100				
74AHC164D-Q100	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHC164PW-Q100	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHC164BQ-Q100	−40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74AHCT164-Q100				
74AHCT164D-Q100	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHCT164PW-Q100	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHCT164BQ-Q100	−40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram

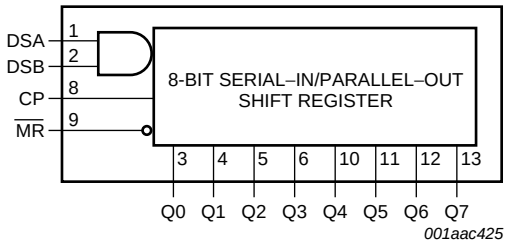


Fig 1. Functional diagram

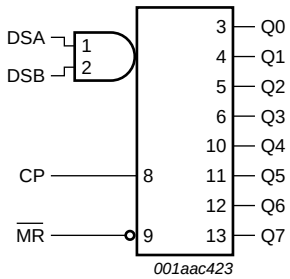


Fig 2. Logic symbol

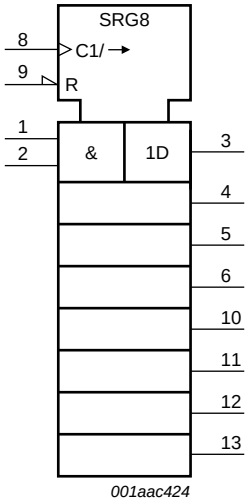


Fig 3. IEC logic symbol

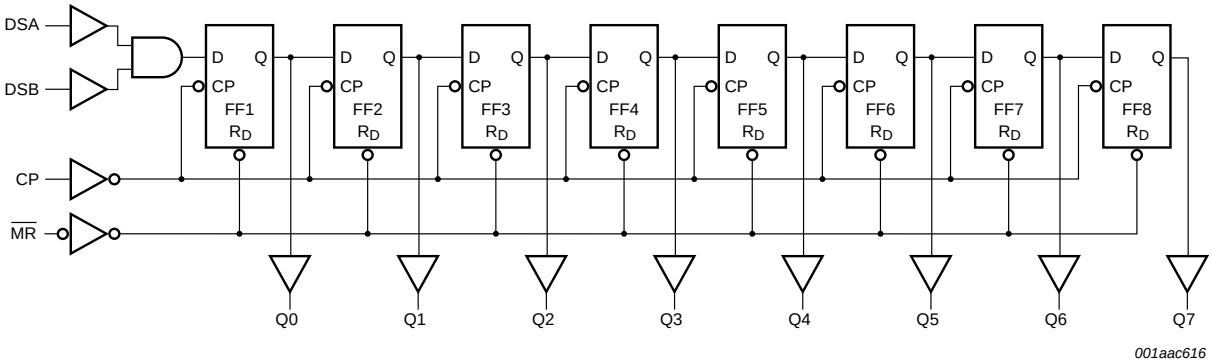


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

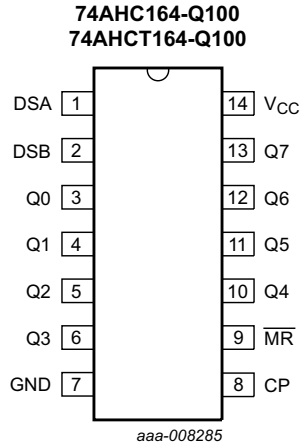
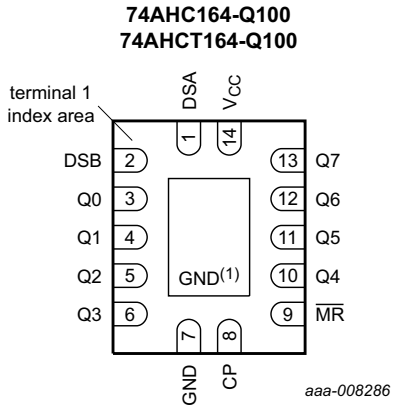


Fig 5. Pin configuration SO14 and TSSOP14



Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It cannot be used as a supply pin or input.

Fig 6. Pin configuration DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
DSA	1	serial data input A
DSB	2	serial data input B
Q0	3	output 0
Q1	4	output 1
Q2	5	output 2
Q3	6	output 3
GND	7	ground (0 V)
CP	8	clock input (LOW-to-HIGH edge-triggered)
$\overline{MR}$	9	master reset input (active LOW)
Q4	10	output 4
Q5	11	output 5
Q6	12	output 6
Q7	13	output 7
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Operating mode	Control		Input		Output	
	$\overline{MR}$	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	L	L to L
Shift	H	↑	l	l	L	q0 to q6
			l	h	L	q0 to q6
			h	l	L	q0 to q6
			h	h	H	q0 to q6

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
↑ = LOW-to-HIGH transition;
X = don't care;
q = lower case letter indicates the state of the referenced input one set-up time prior to the LOW-to-HIGH transition.

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+7.0	V
V_I	input voltage			−0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	[1]	−20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	−20	+20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)		−25	+25	mA
I_{CC}	supply current			-	+75	mA
I_{GND}	ground current			−75	-	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
For TSSOP14 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.
For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly at 4.5 mW/K.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74AHC164-Q100						
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 3.0 V to 3.6 V	-	-	100	ns/V
		V_{CC} = 4.5 V to 5.5 V	-	-	20	ns/V
74AHCT164-Q100						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 4.5 V to 5.5 V	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC164-Q100										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V_{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V_{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = –50 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –50 μA; V_{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I_O = –50 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –4.0 mA; V_{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 50 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 μA; V_{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V

Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	μA
C_I	input capacitance		-	3	10	-	-	-	-	pF
74AHCT164-Q100										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = –50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC}$ – 2.1 V; I_O = 0 A; other pins at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance		-	3	10	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 10.

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC164-Q100											
t_{pd}	propagation delay	CP to Qn; see Figure 7	[2]								
		V_{CC} = 3.0 V to 3.6 V									
		C_L = 15 pF		-	6.5	12.8	1.0	15.0	1.0	16.0	ns
		C_L = 50 pF		-	9.3	16.3	1.0	18.5	1.0	20.5	ns
		V_{CC} = 4.5 V to 5.5 V									
		C_L = 15 pF		-	4.5	9.0	1.0	10.5	1.0	11.5	ns
		C_L = 50 pF		-	6.4	11.0	1.0	12.5	1.0	14.0	ns
		$\overline{MR}$ to Qn; see Figure 8	[3]								
		V_{CC} = 3.0 V to 3.6 V									
		C_L = 15 pF		-	5.3	12.8	1.0	15.0	1.0	16.0	ns
		C_L = 50 pF		-	7.6	16.3	1.0	18.5	1.0	20.5	ns
		V_{CC} = 4.5 V to 5.5 V									
		C_L = 15 pF		-	4.0	8.6	1.0	10.0	1.0	11.0	ns
		C_L = 50 pF		-	5.8	10.6	1.0	12.0	1.0	13.5	ns
f_{max}	maximum frequency	see Figure 7									
		V_{CC} = 3.0 V to 3.6 V									
		C_L = 15 pF		80	125	-	65	-	50	-	MHz
		C_L = 50 pF		50	75	-	45	-	35	-	MHz
		V_{CC} = 4.5 V to 5.5 V									
		C_L = 15 pF		125	175	-	105	-	85	-	MHz
		C_L = 50 pF		85	115	-	75	-	65	-	MHz
t_W	pulse width	CP HIGH or LOW; see Figure 7									
		V_{CC} = 3.0 V to 3.6 V		5.0	-	-	5.0	-	5.0	-	ns
		V_{CC} = 4.5 V to 5.5 V		5.0	-	-	5.0	-	5.0	-	ns
t_{WL}	pulse width LOW	$\overline{MR}$; see Figure 8									
		V_{CC} = 3.0 V to 3.6 V		5.0	-	-	5.0	-	5.0	-	ns
		V_{CC} = 4.5 V to 5.5 V		5.0	-	-	5.0	-	5.0	-	ns
t_{su}	set-up time	DSA, DSB to CP; see Figure 9									
		V_{CC} = 3.0 V to 3.6 V		5.0	-	-	6.0	-	6.0	-	ns
		V_{CC} = 4.5 V to 5.5 V		4.5	-	-	4.5	-	4.5	-	ns
t_h	hold time	DSA, DSB to CP; see Figure 9									
		V_{CC} = 3.0 V to 3.6 V		1.5	-	-	1.5	-	1.5	-	ns
		V_{CC} = 4.5 V to 5.5 V		2.0	-	-	2.0	-	2.0	-	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 10.

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
t_{rec}	recovery time	$\overline{MR}$ to CP; see Figure 8									
		V_{CC} = 3.0 V to 3.6 V		2.5	-	-	2.5	-	2.5	-	ns
		V_{CC} = 4.5 V to 5.5 V		2.5	-	-	2.5	-	2.5	-	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC}	[4]	-	48	-	-	-	-	-	pF
74AHCT164-Q100; V_{CC} = 4.5 V to 5.5 V											
t_{pd}	propagation delay	CP to Qn; see Figure 7	[2]								
		C_L = 15 pF		-	3.4	9.0	1.0	10.5	1.0	11.5	ns
		C_L = 50 pF		-	4.9	11.0	1.0	12.5	1.0	14.0	ns
		$\overline{MR}$ to Qn; see Figure 8	[3]								
		C_L = 15 pF		-	3.5	8.6	1.0	10.0	1.0	11.0	ns
		C_L = 50 pF		-	5.0	10.6	1.0	12.0	1.0	13.5	ns
f_{max}	maximum frequency	see Figure 7									
		C_L = 15 pF		125	175	-	105	-	85	-	MHz
		C_L = 50 pF		85	115	-	75	-	65	-	MHz
t_W	pulse width	CP HIGH or LOW; see Figure 7		5.0	-	-	5.0	-	5.0	-	ns
t_{WL}	pulse width LOW	$\overline{MR}$; see Figure 8		5.0	-	-	5.0	-	5.0	-	ns
t_{su}	set-up time	DSA, DSB to CP; see Figure 9		4.5	-	-	4.5	-	4.5	-	ns
t_h	hold time	DSA, DSB to CP; see Figure 9		2.0	-	-	2.0	-	2.0	-	ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Figure 8		2.5	-	-	2.5	-	2.5	-	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC}	[4]	-	51	-	-	-	-	-	pF

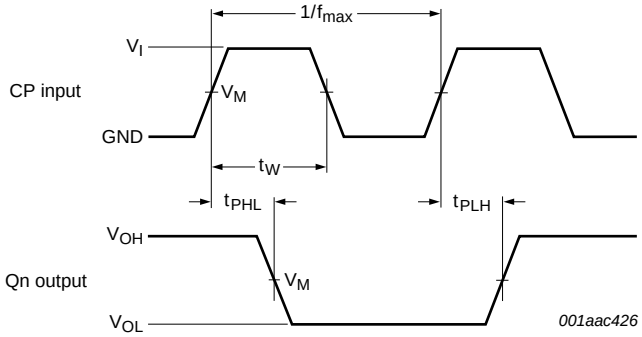
[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{pd} is the same as t_{PHL} only.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

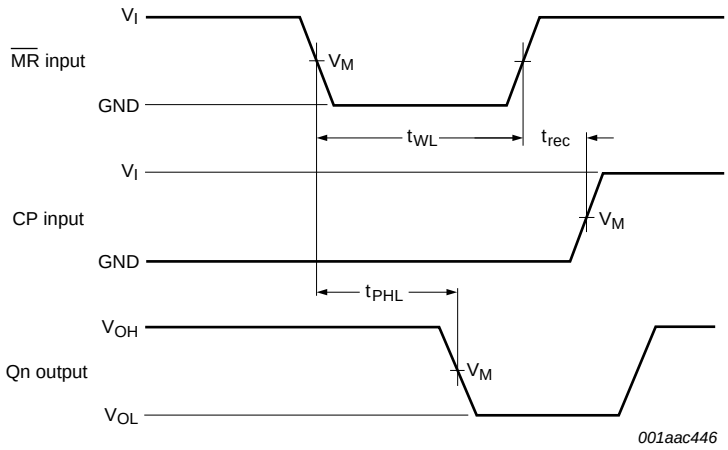
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

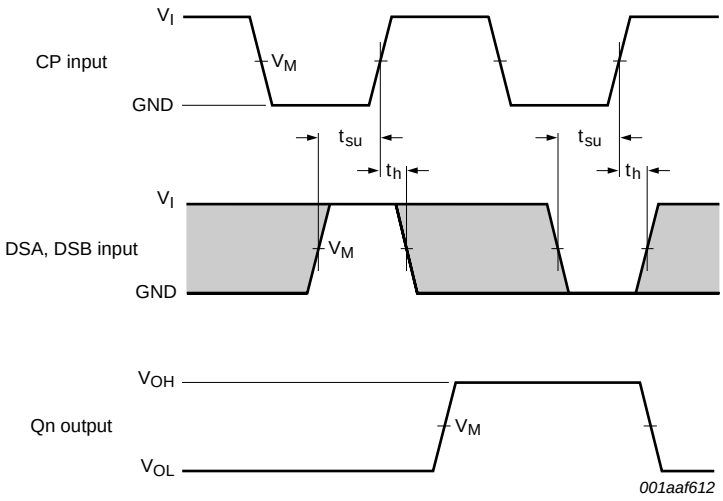
Fig 7. Clock pulse width, maximum frequency and input to output propagation delays



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Master reset pulse width, recovery time and propagation delays



Measurement points are given in Table 8.

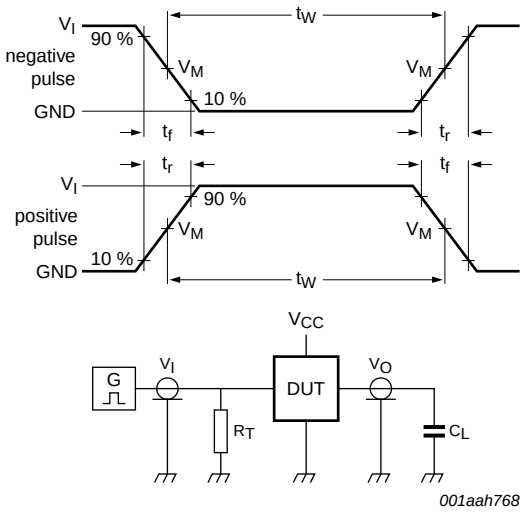
The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 9. Data set-up and hold times

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74AHC164-Q100	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT164-Q100	1.5 V	$0.5 \times V_{CC}$



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

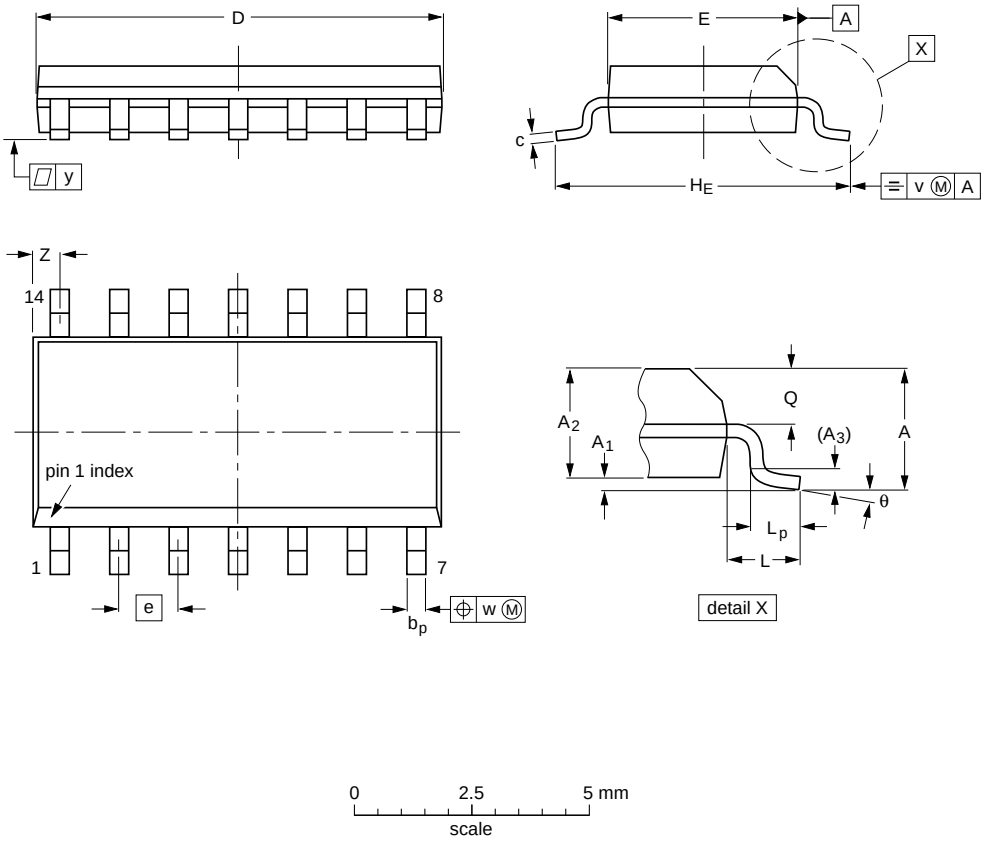
Fig 10. Load circuitry for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74AHC164-Q100	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74AHCT164-Q100	3.0 V	≤ 3.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

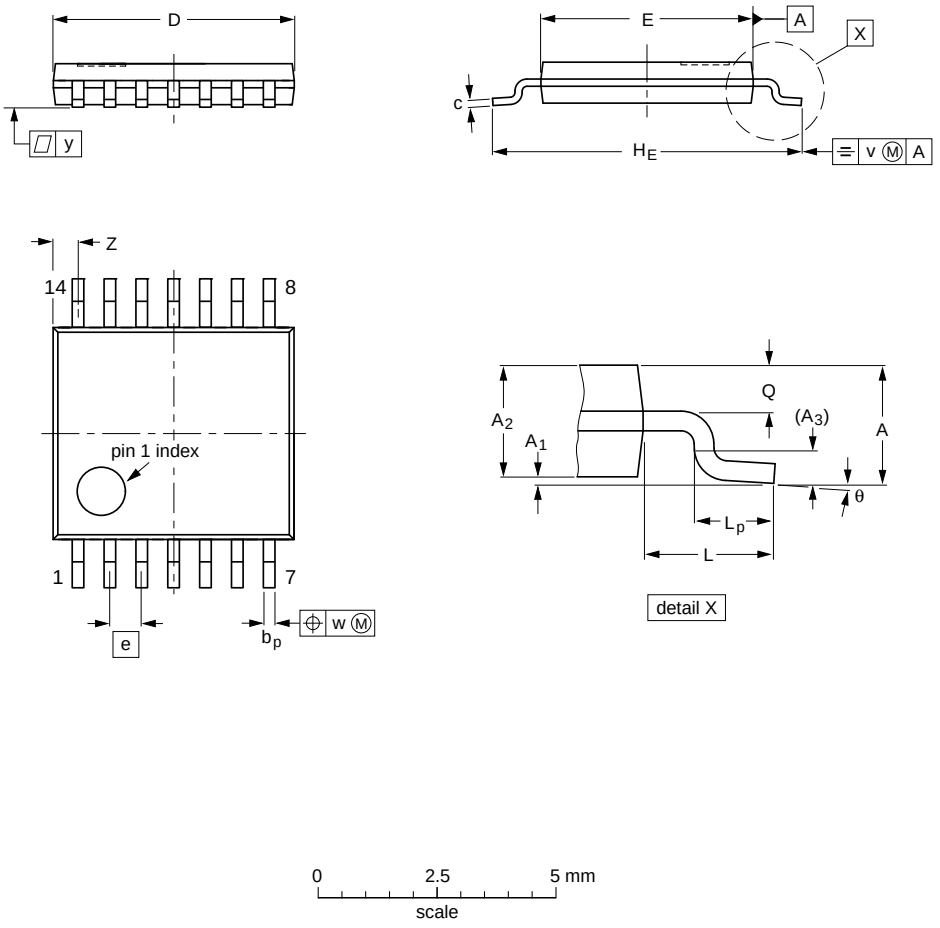
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

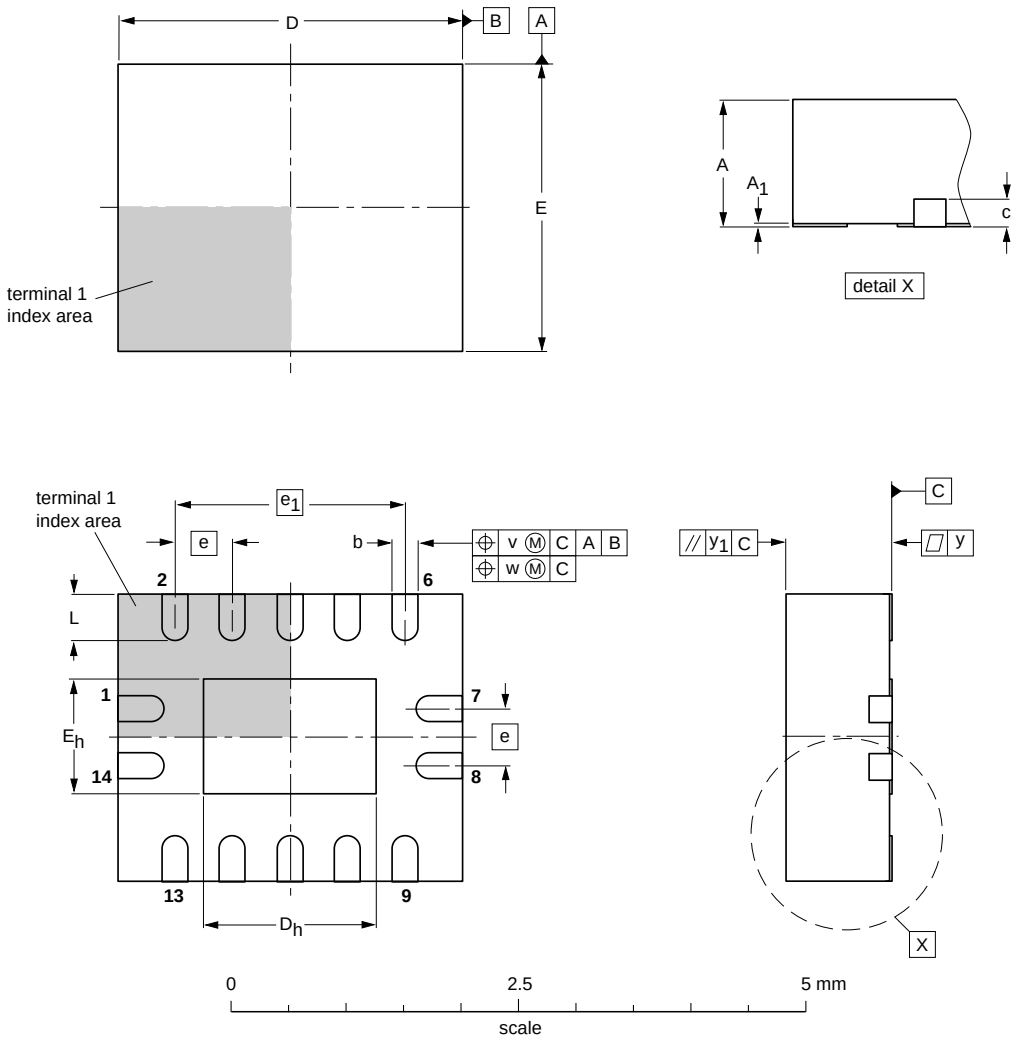
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 12. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 13. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
MIL	Military
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT164_Q100 v.1	20130705	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This Nexperia product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: **http://www.nexperia.com**

For sales office addresses, please send an email to: **salesaddresses@nexperia.com**

17. Contents

For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 05 July 2013

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Nexperia:
74AHC164BQ-Q100X 74AHC164PW-Q100J 74AHCT164D-Q100J 74AHC164D-Q100J 74AHCT164BQ-Q100X
74AHCT164PW-Q100J