CIPOS™ Nano QFN-based IPM application note

PCB design and assembly technique

About this document

Scope and purpose

The scope of this application note is to get an insight into the CIPOS™ Nano IPM thermally efficient design and its main benefits on board-mounted power applications. It also provides information about the desired soldering profile and assembly process, and illustrates how this IPM family offers different power levels in a standard footprint, allowing flexibility and scalability in system designs.

Intended audience

This application guide is intended for customers using an intelligent power module from Infineon Technologies.

1 Scope

Motor controllers for use in home appliances and light industrial drives are typically designed using an intelligent power module (IPM) containing gate drivers using HVIC technology, power switches (MOSFETs) configured as a half-bridge or three-phase bridge, and protection components. The module connects directly between the motor and the processor hosting the motor-control algorithm, and replaces as many as 30 or more discrete components, depending on the configuration. As an integrated solution, the intelligent power module not only simplifies design, lowers bill of materials costs and saves PCB space, but also enhances reliability and helps reduce electromagnetic interference (EMI).

To simplify board mounting and improve reliability, Infineon manufactures CIPOS™ Nano IPMs to exacting standards. These high standards have evolved through evaluating many different materials and designs. In most applications such as inverters in HVAC equipment, fans, pumps, compressors and variable-speed drives up to 250 W power rating, the CIPOS™ Nano IPM is intended to operate without a heatsink. This further reduces bill of materials costs, and simplifies assembly.

The modules are packaged as 12 x 12 mm or 8 x 9 mm or 8 x 7 mm QFN (quad flat no leads) packages, depending on MOSFET size and inverter configuration, which are designed to dissipate heat through large electrical contacts soldered down onto the PCB. The goal of this application note is to define basic design rules on substrates, soldering profile and material, assembly processes, reworking and inspections, and to provide recommendations to designers for the implementation of their final PCB board.

The application note concerns the following products:

IRSM836-015MA
IRSM836-024MA
IRSM836-025MA
IRSM836-035MA
IRSM836-035MB
IRSM836-044MA
IRSM836-045MA
IRSM836-084MA
IRSM808-105MH
IRSM808-204MH
IRSM807-045MH
IRSM807-105MH
IRSM005-301MH
IRSM005-800MH

CIPOS™ Nano IPMs are a family of highly integrated, ultra-compact power modules for high-efficiency consumer, residential and light industrial applications, including rectifiers, converters, and inverters in power management circuits as well as motor drives for hair dryers, air purifiers, ceiling fans, circulation pumps, and ventilators.

1.1 Product line-up

Table 1 Line-up of CIPOS™ Nano IPMs

Part number	Motor I_{rms} range	Topology	Line-up	Package dimensions
IRSM836-0x4MA	0.1 to 1.2 A_{rms}	3 phase	250 V MOSFET 0.45 Ω, 1.05 Ω, 2.2 Ω	12 x 12 x .09 mm
IRSM836-0x5MA			500 V MOSFET 1.7 Ω, 2.2 Ω, 4.0 Ω, 6.0 Ω	12 x 12 x .09 mm
IRSM808-204MH	0.4 to 2 A_{rms}	Half bridge	250 V MOSFET 0.15 Ω	8 x 9 x 0.9 mm
IRSM807-105MH			500 V MOSFET 0.8 Ω, 1.7 Ω	8 x 9 x 0.9 mm
IRSM807-045MH			500 V MOSFET 0.8Ω, 1.7Ω	8 x 9 x 0.9 mm
IRSM005-800MH	1 to 10A_{rms}		40V MOSFET 4.5 mΩ	7 x 8 x 0.9 mm
IRSM005-301MH			100 V MOSFET 21 mΩ	7 x 8 x 0.9 mm

2 Device construction

CIPOS™ Nano IPMs are surface mounted, and use current plastic-molding techniques with wire bond interconnects, as shown in Figure 1.

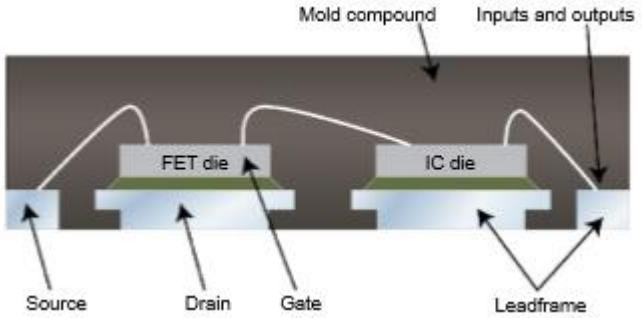


Figure 1 *Sectional view*

Figure 2 shows a sample contact configuration for a CIPOS™ Nano IPM. Specific pad assignments are shown in the data sheet for each product.

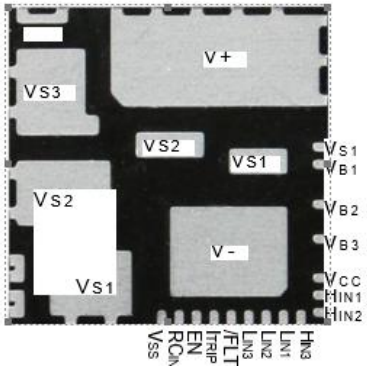


Figure 2 *QFN 12x12 package*

The position of Pin 1 is indicated in two ways:

- A dot on the top side (Figure 3).
- A chamfer on a pad on the underside (Figure 4); this is on the pad area closest to Pin 1.

Figure 3 *Pin 1 indicator on a CIPOS™ Nano IPM*

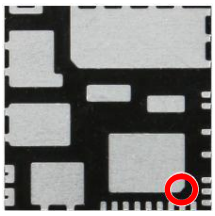


Figure 4 *Pin 1 indicator on a CIPOS™ Nano IPM*

3 PCB design considerations

3.1 Substrates

CIPOS™ Nano IPMs were originally developed and evaluated for use with epoxy glass-woven substrates. The test substrates were finished in organic solderability preservative (OSP), but any of the numerous surface finishes available are suitable.The substrate finish can affect the amount of energy required to make solder joints; this can in turn be a factor in solder quality issues such as solder balling, tombstoning (or tilt) and the formation of voids.

3.1.1 Substrate designs

To achieve low-loss track layouts, CIPOS™ Nano IPMs were designed for use with layouts that use solder-mask-defined (SMD) pad lands and non-solder-mask-defined (NSMD) lead lands. SMD pad lands allow the underlying copper traces to be as large as possible, which increases their ability to carry current and cool devices. NSMD (also known as copper-defined) lead lands maximize the tolerance of misaligned leads and the control of land pad dimensions.

However, CIPOS™ Nano IPMs have also been evaluated only with NSMD layouts. Using SMD pad lands is not essential and may be eliminated if doing so improves compatibility with existing processes.

When using SMD lands, the underlying copper trace should be at least 0.05 mm larger on each edge than the openings in the solder mask. This allows for layers to be misaligned by up to 0.1 mm on both axes.

When using NSMD lands, the openings in the solder mask should be at least 0.025 mm larger on each edge than the copper pads. This allows for layers to be misaligned by up to 0.05mm on both axes.

The solder mask between lead lands, and between lead and pad lands, should be at least 0.15 mm wide. Narrower strips may allow solder bridges to form.

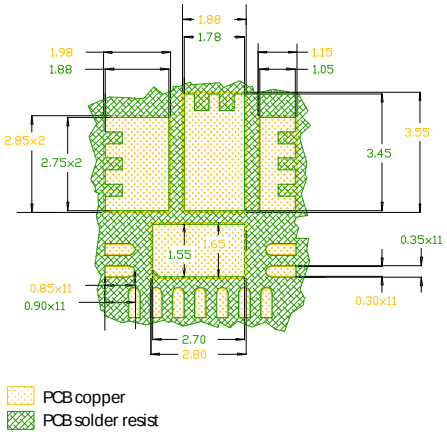


Figure 5 *Sizing the areas of copper and solder mask*

CIPOS™ Nano IPMS can be placed in parallel using simple layouts (Figure 6). Infineon recommends a minimum separation of 0.500 mm (0.020"). The separation can be adjusted to reflect local process capabilities but should allow for rework. Micro-screen design and desoldering tool types may affect how closely devices are placed to each other and to other components.

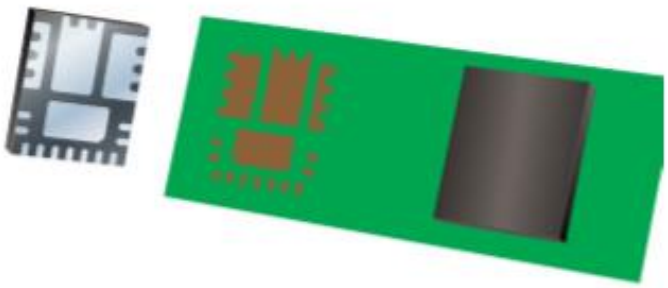


Figure 6 *Placing CIPOS™ Nano IPMs in parallel*

Refer to the Appendix for device outlines, substrate layouts and stencil designs for each package size and device outline in the CIPOS™ Nano IPM range.

4 Assembly considerations

Infineon designed CIPOS™ Nano IPMs to be as easy as possible to assemble using standard surface-mounting techniques. However, procedures and conditions can have a profound influence on assembly quality. It is therefore necessary to develop an effective process based on the individual requirements for the application.

4.1 Packaging

CIPOS™ Nano IPMs are supplied in tape and reel format (Figure 7)

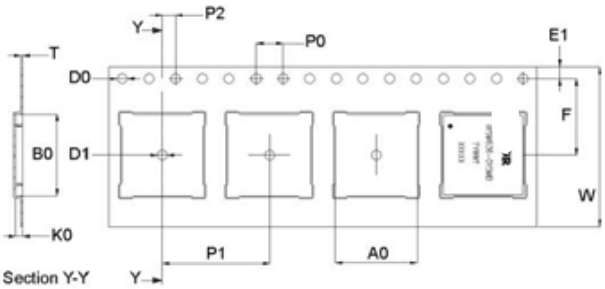


Figure 7 *Tape and reel packaging*

	Dimensions (mm)					
	7x8		8x9		12x12	
Code	Min	Max	Min	Max	Min	Max
A0	7.15	7.35	8.20	8.40	12.20	12.40
B0	8.15	8.35	9.20	9.40	12.20	12.40
D0	1.50	1.60	1.50	1.60	1.50	1.60
D1	1.50	—	1.50	—	1.50	—
E1	1.65	1.85	1.65	1.85	1.65	1.85
F	7.40	7.60	7.40	7.60	11.40	11.60
K0	1.10	1.30	1.20	1.40	1.00	1.20
P0	3.90	4.10	3.90	4.10	3.90	4.10
P1	11.90	12.10	11.90	12.10	15.90	16.10
P2	1.90	2.10	1.90	2.10	1.90	2.10
T	0.25	0.35	0.25	0.35	0.25	0.35
W	15.70	16.30	15.70	16.30	23.70	24.30

4.2 Storage requirements

CIPOS™ Nano IPMs are packed in sealed, nitrogen-purged, antistatic bags. The sealed bags provide adequate protection against normal light levels, however, it is prudent to avoid prolonged exposure to bright light sources. The bags also provide protection from the ambient atmosphere. Devices in sealed, unopened bags have a shelf life of one year.

The package labeling shows whether devices should be treated as moisture sensitivity level (MSL) 1, 2 or 3 after a bag has been opened. Appropriate storage is important to guarantee good solderability.

Infineon recommends that, when not in use, reels of devices should be resealed into the protective bags in which they were supplied.

4.3 Solder pastes

Infineon evaluated different types of soldering paste from various manufacturers. The properties of pastes vary from manufacturer to manufacturer, meaning that some perform better than others. In general, high slumping pastes tend to suffer more from solder balling than slump-resistant pastes; solder balling is discussed in the next section on stencil design. In addition, some pastes appear to be more prone to voiding than others.

Solder alloys, metal contents and flux constituents all influence the rheology of the solder paste. This in turn influences how the paste reacts during processing. The assembly and board-level reliability of the QFN package have only been evaluated using lead-free pastes (Sn96.5 Ag3.0 Cu0.5).

Infineon testing has also shown that halogen-free (or zero-halogen) solder pastes perform better than pastes that contain halogen. The flux residues after reflow are cleaner and more inert. There are fewer instances of voltage tracking.

Infineon qualifies devices using the reflow profile outlined in J STD 020C but the reflow profile that delivers the best results will depend on the solder paste used in board mounting. Different pastes from different suppliers behave in different ways. The technical datasheet for the solder paste in use may include advice on setting up the optimal reflow profile and should be consulted as a starting point.

4.4 Stencil design

The stencil design is instrumental in controlling the quality of the solder joint. Appendix A shows stencil designs that have given good results with the recommended substrate outlines. The reductions relative to the PCB pad size in these designs depend on the pad size itself. In general, larger pads require greater reduction. For example, the smaller single pads around the outer edges of a device typically have a reduction of 10-15%, while the larger central power pad has a reduction of up to 45%.

Designs are shown for stencil thicknesses of 0.127 mm (0.005") and 0.150 mm (0.006"). A thickness of 0.127 mm (0.005") is optimal. Infineon does not recommend the use of stencils thinner than 0.100 mm and thicker than 0.150 mm.

As a general guideline, the reductions relative to the PCB pad sizes for stencils of different thicknesses are:

- 50% for a 0.127 mm (0.005") stencil
- 45% for a 0.150 mm (0.006") stencil

The aim when depositing solder paste is to produce a solder joint where voids account for less than 25% of the area. The solder joints on the small outer edge pads should be at least 0.05 mm (0.002") thick. There is no minimum requirement for the larger pads.

Note: The thickness of the solder mask on the PCB can affect the thickness of the solder joints. This is because the solder mask can act as a gasket, with the effect of making the solder paste stencil thicker. This can cause the solder joints to be thicker than expected (or calculated). The designs in Appendix A assume a solder mask thickness of 0.025 mm (0.001").

4.5 Solder joint voiding

The main causes of solder joint voiding are applying the incorrect volume of solder paste and/or using a reflow profile that is not optimized.

If an unacceptable amount of voiding is observed in solder joints, experimentation may be required to design a solder paste stencil that applies an appropriate amount of solder paste. Breaking up pads into smaller blocks can yield good results (Figure 8).

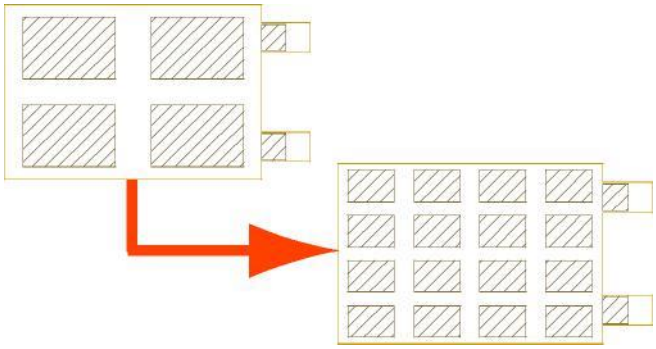


Figure 8 *Dividing large pads into smaller blocks*

4.6 Device placement

Inaccurate placement may result in poor solder joints or in devices being tilted and/or misaligned. Ideally, CIPOS™ Nano IPMs should be placed to an accuracy of 0.050 mm on both X and Y axes but, during evaluations, devices centered themselves from placement inaccuracies of more than 0.300 mm. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes

4.7 Reflow equipment

CIPOS™ Nano IPMs are suitable for assembly using surface mount technology reflowing equipment and are recommended for use with convection, vapor phase and infrared equipment. PbF qualified devices have a good resistance to short-term exposure to high temperatures, making them suitable for reflow profiles of up to 260°C (measured by attaching a thermocouple to a CIPOS™ Nano IPM).

There are no special requirements for successful assembly, but all reflow processes used in evaluation and qualification complied with the recommendations of solder paste suppliers. Using incorrect reflow profiles can cause solder quality issues such as solder balling, tombstoning (or tilt) and the formation of voids; if such problems arise, the reflow profile should be checked.

The QFN package is designed to have superior thermal conductivity properties. For this reason, it is essential that the core of the substrate reaches thermal equilibrium during the pre-heating stage of the reflow profile to ensure that adequate thermal energy reaches the solder joint.

The designs for PCB layouts and solder paste stencils shown in Appendix A are suitable for all assembly styles, irrespective of size and complexity. The only caveat is that the reflow profile at the device must comply with the solder paste manufacturer's recommendations. If, for example, the PCB is large and/or heavy, the reflow profile may need to be slowed down to achieve good thermal equilibrium across the whole PCB. The same result may be achieved by making the pre-heat soak or plateau longer and/or hotter.

Failure to meet these requirements may result in unspent or non-volatilized flux residues being left underneath the device (Figure 9). This can result in current leakage and/or short circuits.

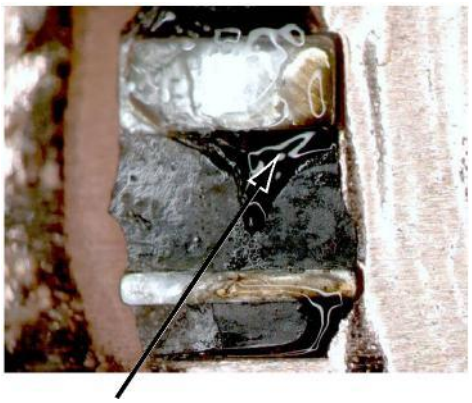


Figure 9 *Flux residue compromising isolation*

4.8 Inspection

The best way to inspect devices after reflow is through a combination of visual inspection of the peripheral solder joints and X-ray imaging of the connections directly under the package.

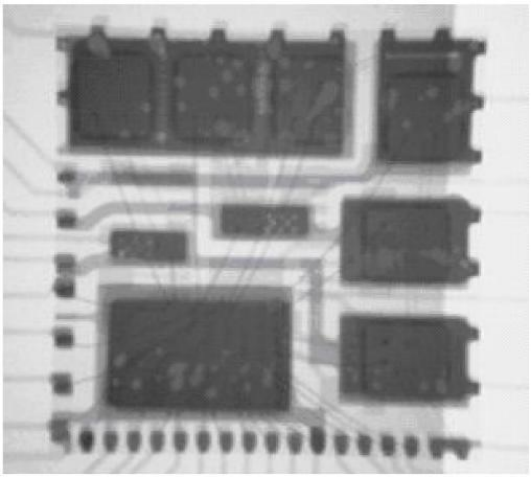


Figure 10 *X-ray of a CIPOS™ Nano IPM*

Figure 10 is a typical X-ray image of a board-mounted CIPOS™ Nano IPM, which shows the solder joints, device alignment and solder voiding level. Regarding solder joint voiding, most customers use 25–30% as the acceptable limit, often citing industry standards such as IPC-A-610 or IPC-7093. However, having tested board-mounted devices deliberately voided up to 45%, Infineon has been unable to detect any deterioration in electrical or thermal performance in application compared with devices voided to 5–10%.

4.9 Rework guidelines

Modern rework stations for ball grid array and leadless packages often use two heating stages:

- The first stage heats the substrate, either with a conventional hot-plate or a hot-air system. This reduces the amount of heating required from the hot-air de-soldering tool, which in turn reduces the risk of damaging either the substrate or surrounding components.
- The second stage uses a hot-air system for localized heating, often with the option of unheated air for faster cooling of the solder interconnections on the replaced device; this improves the solder grain structure.

The device placement mechanism or arm usually has a hot-air de-soldering gun as part of the pick head, equipped with a vacuum cup and thermocouple. Once the solder reflow temperature has been reached, the vacuum is automatically engaged to allow the device to be removed from the substrate. This reduces the risk of causing damage by premature removal.

Most rework stations have the facility to attach a micro-stencil supplied by the vendor, with the aperture design being supplied by the user. The apertures are aligned with the pads on the board before manually screening the solder paste. Alternatively, it is possible to use a standalone micro-stencil and squeegee to apply the paste.

The objective of rework is to remove a non-functional device and replace with a functional device. Infineon does not recommend reusing devices removed from a substrate. To permit subsequent failure analysis, take care when removing devices not to exacerbate the existing failure.
To replace a CIPOS™ Nano IPM:

Note: If you usually bake to remove residual moisture before rework, insert your normal procedure here.

1. Heat the site to approximately 100°C (150°C for lead-free assembly) using the substrate heating stage.

Note: Pb devices are qualified for a maximum reflow peak temperature of 240°C (260°C for PbF devices). To avoid overheating the device or substrate, adjust the settings on your equipment to achieve a maximum air temperature of 300°C.

2. Lower the placement arm to bring the de-soldering tool into contact with the device. When the device and the solder interconnects reach reflow temperature, lift the placement arm to remove the device from the substrate. Discard the device.
3. Clear residual solder from the site using a blade-type de-soldering tool and de-soldering braid. Clear residual flux using a flux-reducing agent. Take care in cleaning the site: damage to the solder mask may produce undesirable results.
4. When the site is ready, apply new solder paste with a micro-stencil and squeegee.
5. Position a new device on the vacuum tip of the placement head and lower the placement arm until the device is in contact with the solder paste.
6. Switch off the vacuum on the placement head and retract the placement arm, leaving the device in place.
7. Heat the site to approximately 100°C (150°C for lead-free assembly) using the substrate heating stage.
8. Use the de-soldering tool to heat both device and solder interconnects to reflow temperature, waiting until all the solder has reflowed.
9. Retract the arm, leaving the device in place. Cool as quickly as possible.

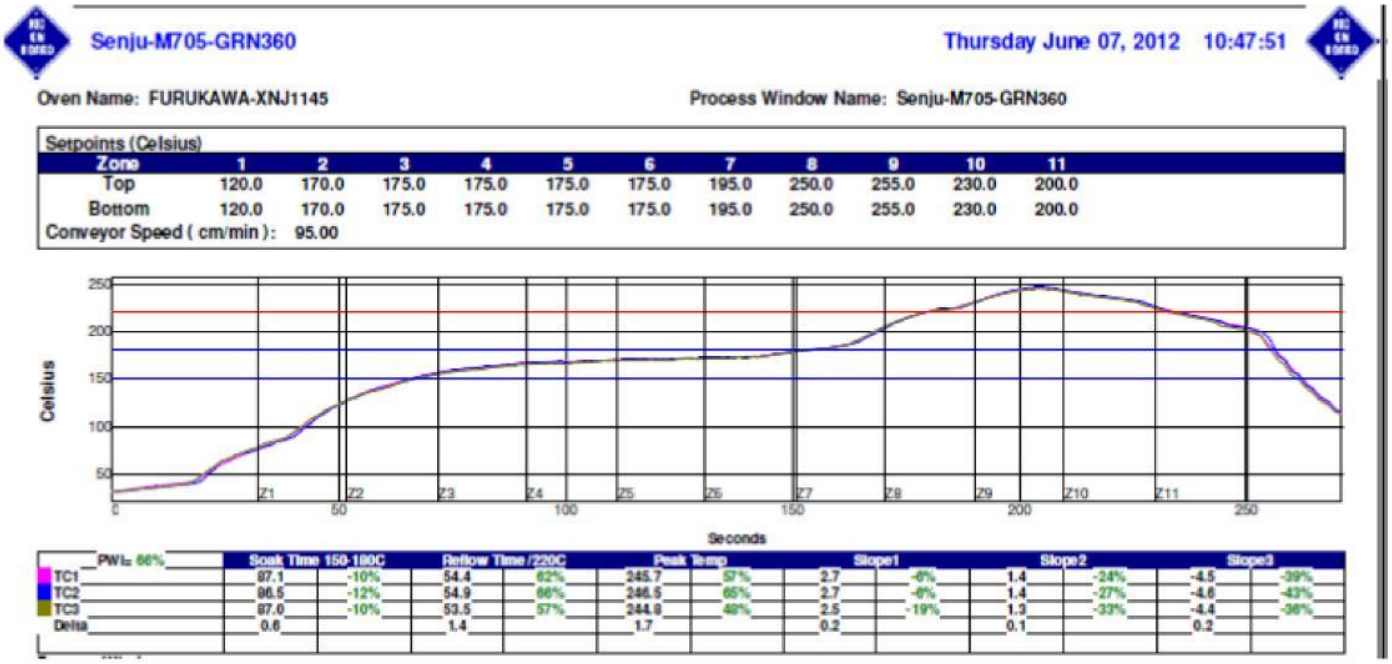
4.10 Sample process

CIPOS™ Nano IPMs are suitable for a wide range of assembly conditions and are not considered to be process-sensitive. However, Infineon has used the following conditions successfully and offers them as an example of a suitable process. They do not constitute a recommendation; other processes may be more appropriate in different environments.

Material	High Tg FR4
Copper thickness	2 oz on outer layers
Pad surface finish	Electroless Nickel Immersion Gold (ENIG)

Solder paste

Stencil thickness	0.0127 mm / 5 mil / 0.005 inch
Solder paste	Senju M705-S101ZH-S4 Sn96.5 / Ag3.0 / Cu0.5



5 Mechanical test results

Infineon has subjected board-mounted CIPOS™ Nano IPMs to extensive mechanical tests, conducted in accordance with industry standards and practices.

This section contains summarized results for shock tests, bend tests, vibration tests, cyclic temperature tests and warpage tests. Full reports are available on request.

5.1 Shock tests

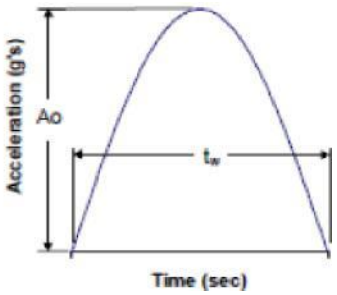
Method

These tests were carried out in accordance with JEDEC JESD22-B111:

- Shock: 1500 G

$$A(t) = A_o \sin\left(\frac{\pi t}{t_w}\right)$$

$$\sqrt{2gH} = \frac{2A_o}{C}\frac{t_w}{\pi}$$



- Duration: 0.5 ms
- Quantity: 30 drops

Figure 11 *Typical shock test half-sine pulse*

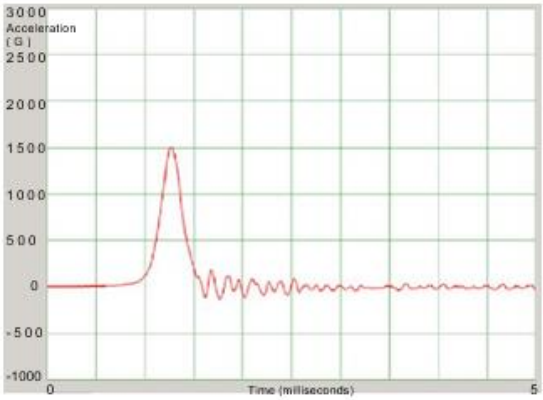


Figure 12 *Actual shock pulse applied*

Results

All devices passed.

5.2 Cyclic bend tests

Method

These tests were carried out in accordance with JEDEC JESD22-B113:

- 200,000 cycles
- 3 Hz test rate
- 1 mm deflection

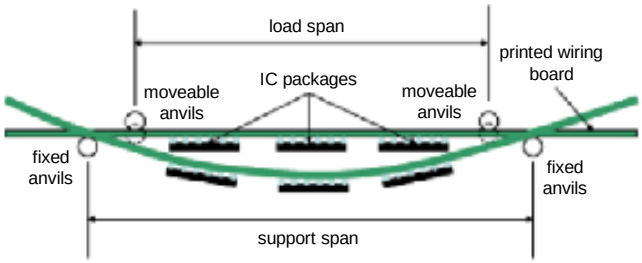


Figure 13 *Four-point bend test set-up*

Results

All devices passed.

5.3 Vibration tests

These method tests were carried out in accordance with MIL-STD-810 Vibration Testing (Method 514, Procedure 1, Category 24).

Devices were subjected to the vibration profile shown in Figure 14.

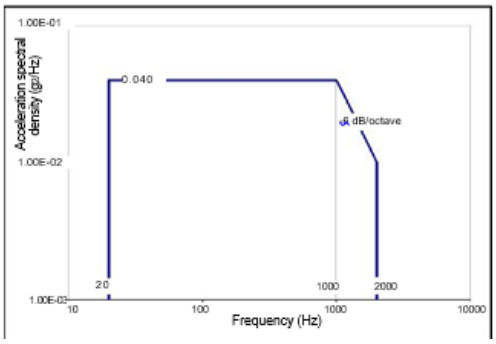


Figure 14 *Vibration profile*

Results

All devices passed.

5.4 Temperature cycle tests

Method

Infineon subjected board-mounted devices (often referred to as ‘second level testing’ or L2 testing) to temperature cycling from -40°C to + 85°C.

Results

All devices passed 1000 cycles.

Figure 16 shows the Weibull plot of the characteristic life of devices mounted on boards using both 0.100 mm (0.004") and 0.127 mm (0.005") solder paste stencils.

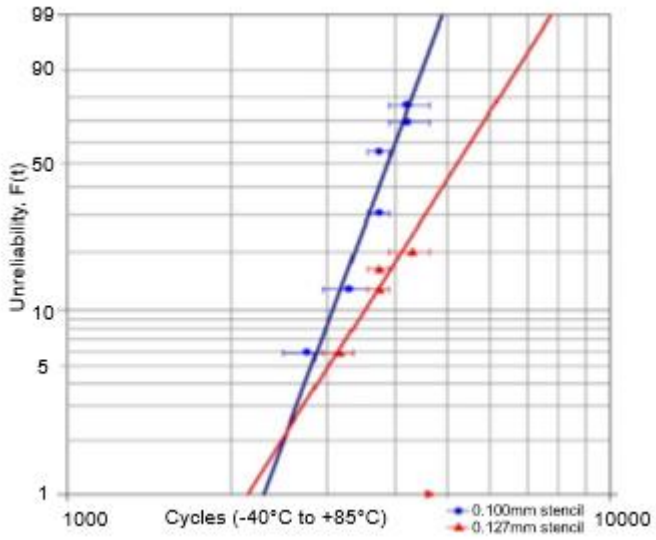


Figure 15 *Temperature cycling test results*

The devices were then left on test to determine their characteristic life. The results were:

- Stencil thickness of 0.127 mm (0.005”) = 5640 cycles
- Stencil thickness of 0.100 mm (0.004”) = 4053 cycles

5.5 Warpage tests

Method

These tests were carried out in accordance with JESD22-B112A.

The failure threshold was derived from IPC/JEDEC J-STD-020D, which states that warpage must not exceed JEDEC’s maximum dimensions for the coplanarity and stand-off of CIPOS™ Nano IPMs. Therefore, for 12x12 CIPOS™ Nano IPMs with a maximum coplanarity of 0.08 mm and maximum stand-off of 0.05 mm, the limit for warpage is 0.08 mm (0.003").

Devices were measured for warpage after three reflow passes with a peak temperature of 260°C using the following procedure:

- Packages placed with leads uppermost (known as the ‘dead bug’ position)
- Samples of five units per assembly lot selected
- Five points measured (see Figure 17), using a Kunoh BK-02 non-contact measurement microscope.

Warpage was calculated for each sample device by subtracting the measurement at the lowest point from the measurement at the highest point.

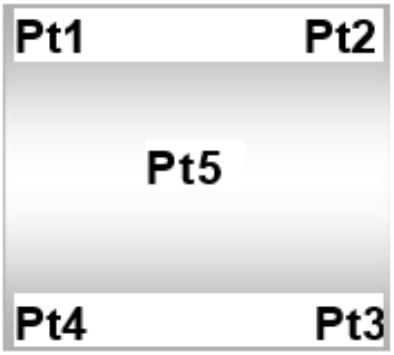


Figure 16 *Five measurement points on device*

Results
All devices passed.

6 Appendix

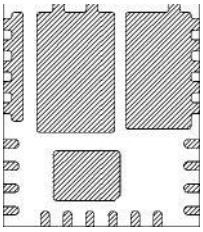
This appendix contains the following information about various CIPOS™ Nano IPMs:

- Device outline drawing
- Recommended substrate/PCB layout
- Stencil designs for thicknesses of 0.127 mm (0.005") and 0.150 mm (0.006")

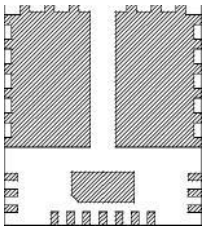
The footprint and stencil designs are recommendations only, and may need to be adjusted to specific requirements. During a study conducted on various package types, Infineon found the designs gave repeatable device alignment and proper solder connections.

For more details about individual devices, and to find out their size and outline, refer to the relevant product data sheet.

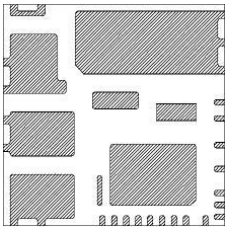
QFN 7x8 outline



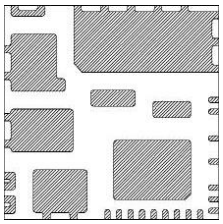
QFN 8x9 outline



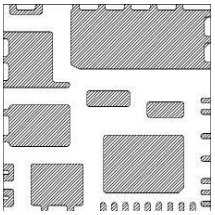
QFN 12x12 V outlines:



27L



36L



37L

6.1 QFN 7x8

Device outline

Figure A.1.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of ±0.050 mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

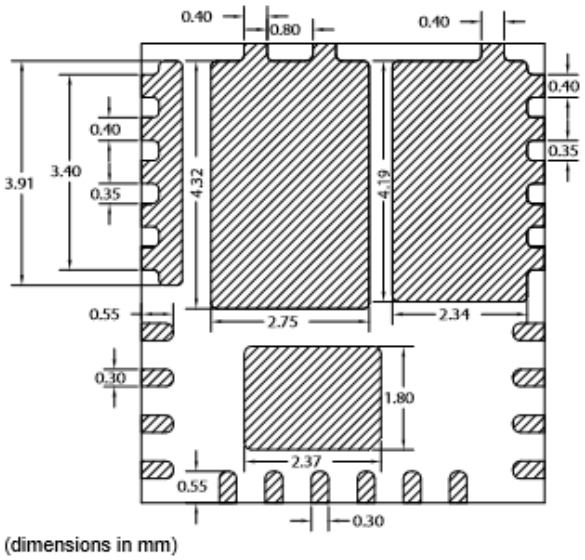


Figure A.1.1 *7x8 CIPOS™ Nano IPM outline*

6.1.1 Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.1.2 (a and b).

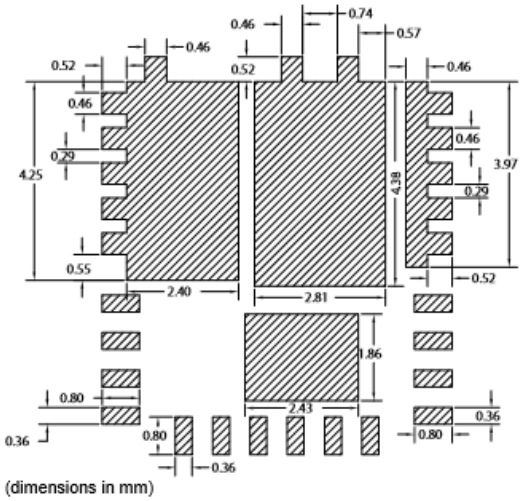


Figure A. 1.2(a)

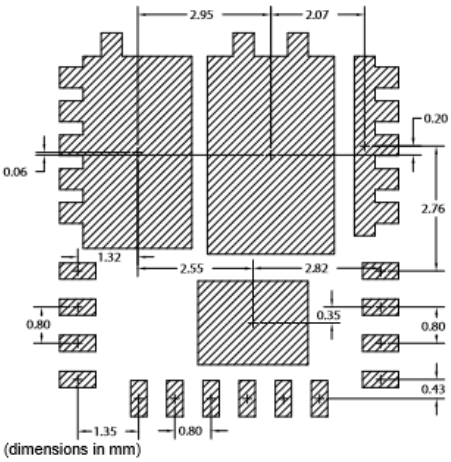
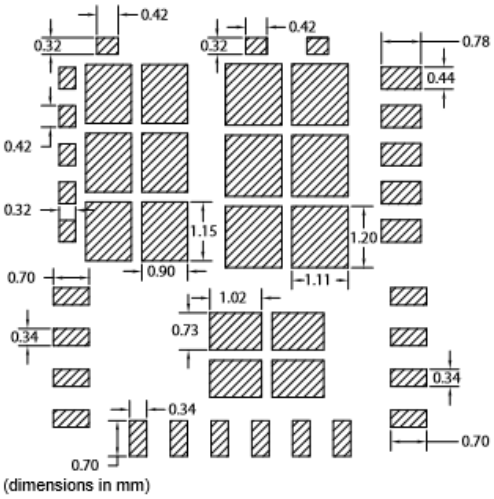
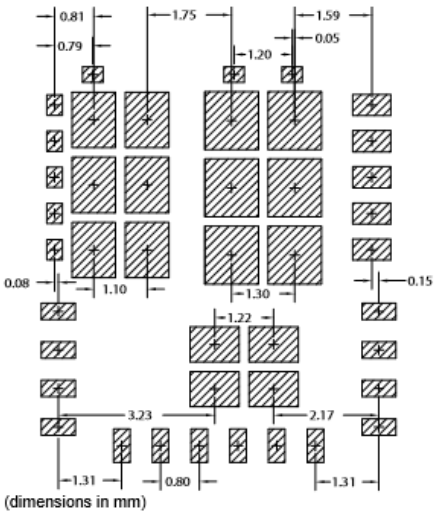


Figure A. 1.2(b)

6.1.2 Stencil design

Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.1.3 . This design is for a stencil thickness of 0.127 mm (0.005").





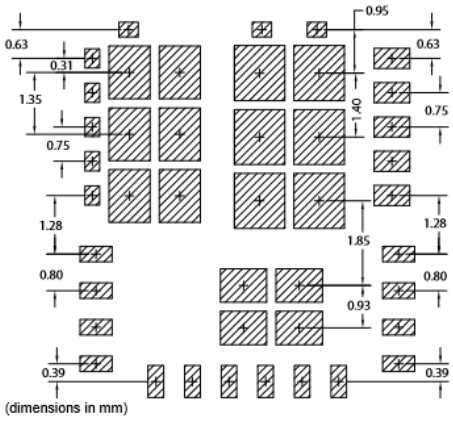


Figure A. 1.3(a) ***Figure A. 1.3(b)*** ***Figure A. 1.3(c)***

6.2 QFN 8x9

Device outline

Figure A.2.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of ±0.050 mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

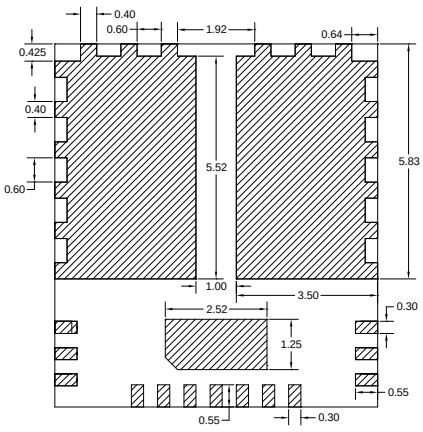


Figure A.2.1 *8x9 mm device*

6.2.1 Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.2.2 (a and b).

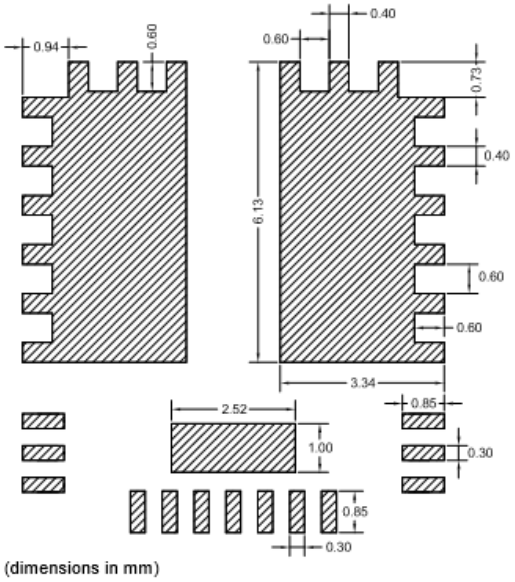


Figure A.2.2(a) *8x9 mm Nano substrate/PCB layout*

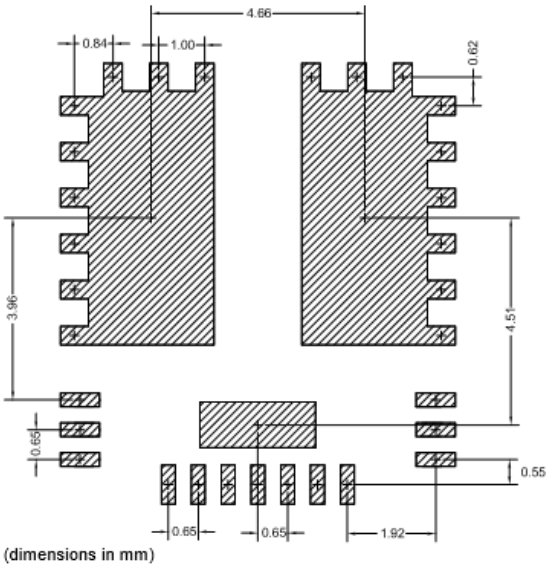


Figure A.2.2(b) *8x9 mm Nano substrate/PCB layout*

6.2.2 Stencil design

Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.2.3 (a and b). This design is for a stencil thickness of 0.127 mm (0.005").

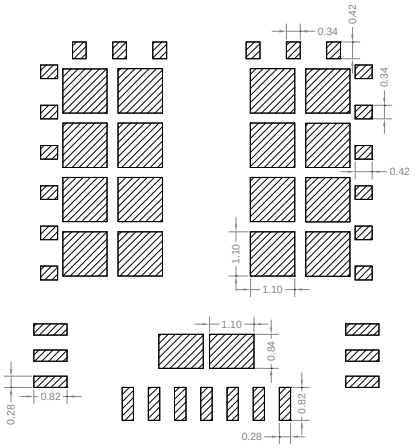


Figure A.2.3 (a)

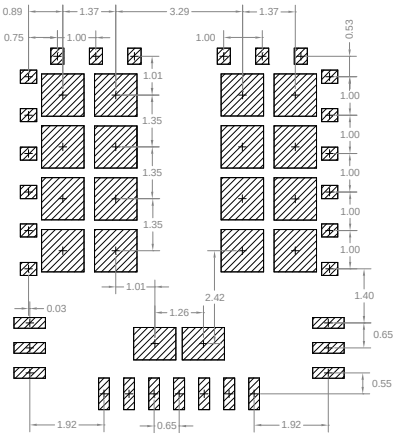


Figure A.2.3 (b)

6.3 QFN 12x12 (27L)

Device outline

Figure A.3.1(a) shows the outline for these devices. The relative pad positions are controlled to an accuracy of ±0.050 mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

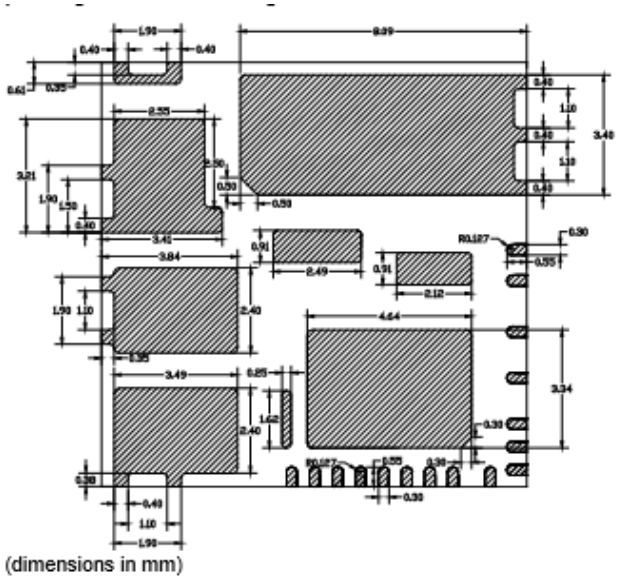


Figure A.3.1(a) *12x12 (27L) device outline*

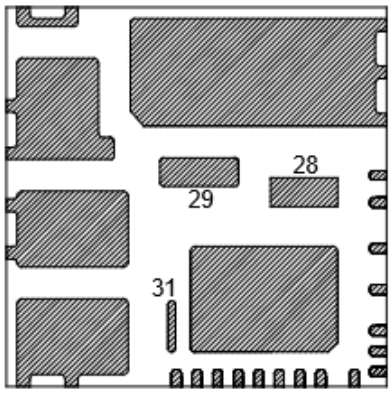


Figure A.3.1(b) *12x12 (27L) – optional pads*

Pads 28, 29 and 31 on the underside of the device (Figure A.3.1(b)) are a result of the internal package construction, and are not required for electrical or thermal connection. While soldering them to the PCB increases mechanical stability, it also traps more flux under the device and restricts the release of gas from the flux during reflow. This can increase the risk of board-level leakage in operation. Consequently, Infineon recommends that these pads are not soldered and excludes them from its recommended PCB layout.

6.3.1 Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.3.2 (a and b)

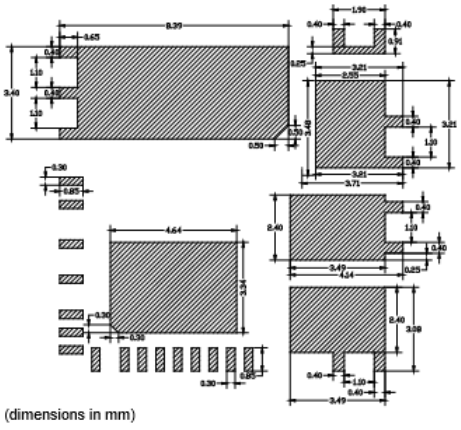


Figure A.3.2(a) *12x12 (27L) substrate/PCB layout*

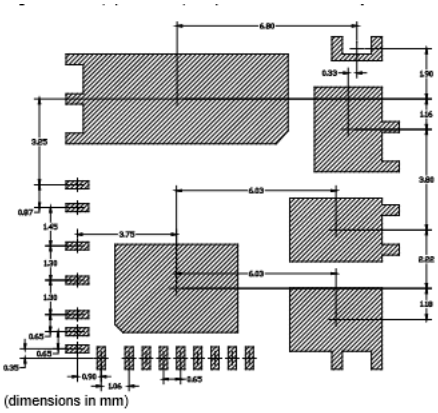


Figure A.3.2(b) *12x12 (27L) substrate/PCB layout*

6.3.2 Stencil design

Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.3.3 (a and b). This design is for a stencil thickness of 0.127 mm (0.005").

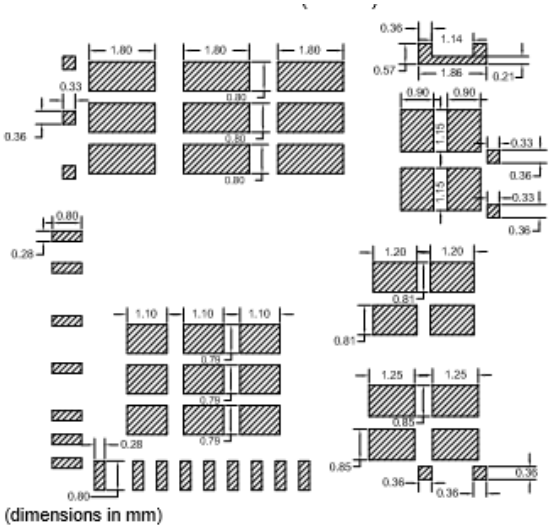


Figure A.3.3(a) *12x12 (27L) 0.127 mm stencil design design*

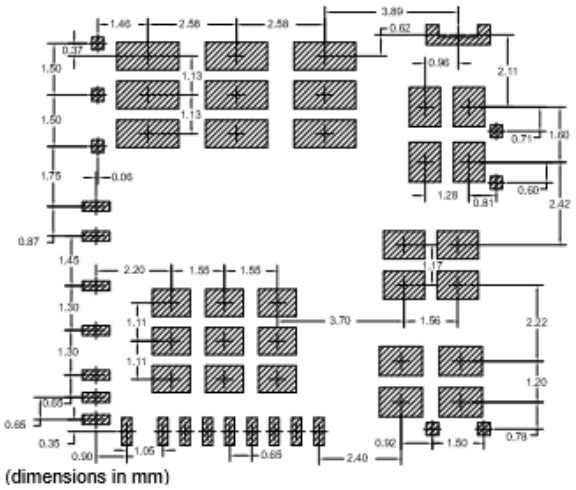


Figure A.3.3(b) *12x12 (27L) 0.127 mm stencil*

If you want to use a thicker stencil, 0.150 mm (0.006"), use the pad sizes shown in Figure A.3.4 with the pad spacings shown in Figure A.3.3(b).

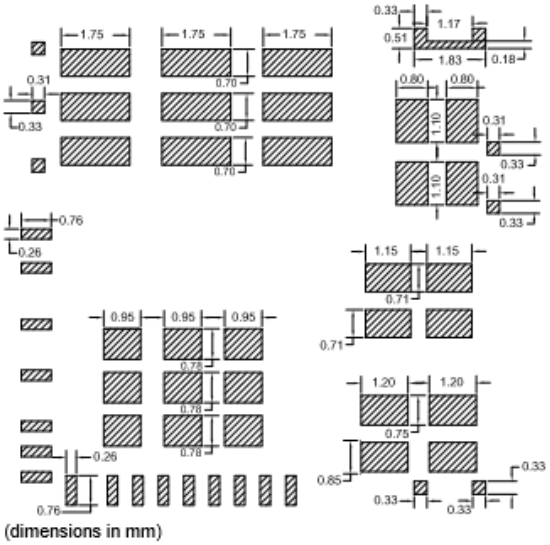


Figure A.3.4 *12x12 (27L) 0.150 mm stencil design*

6.4 QFN 12x12 (36L)

Device outline

Figure A.4.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of ±0.050 mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

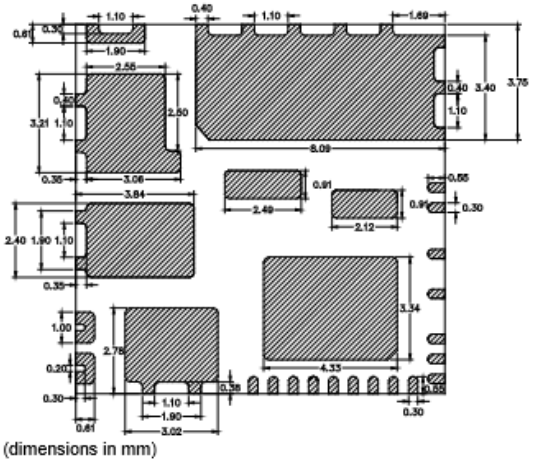


Figure A.4.1 *12x12 (36L) device outline*

6.4.1 Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.4.2 (a, b and c).

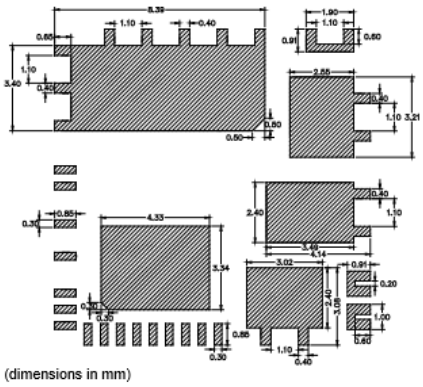


Figure A.4.2(a) *12x12 (36L) substrate/PCB layout*

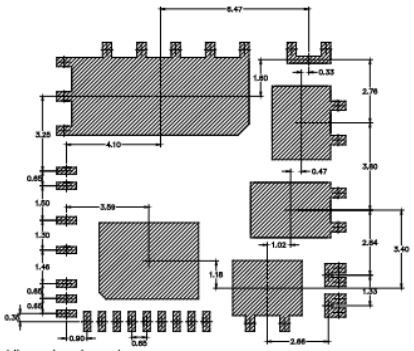


Figure A.4.2(b)

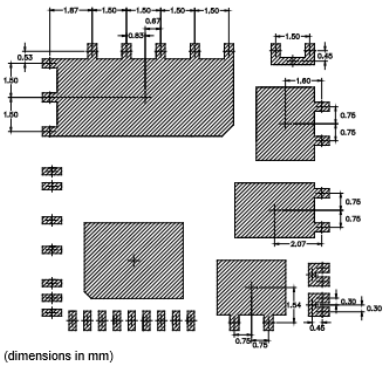


Figure A.4.2(c)

6.4.2 Stencil design

Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.4.3 (a and b). This design is for a stencil thickness of 0.127 mm (0.005").

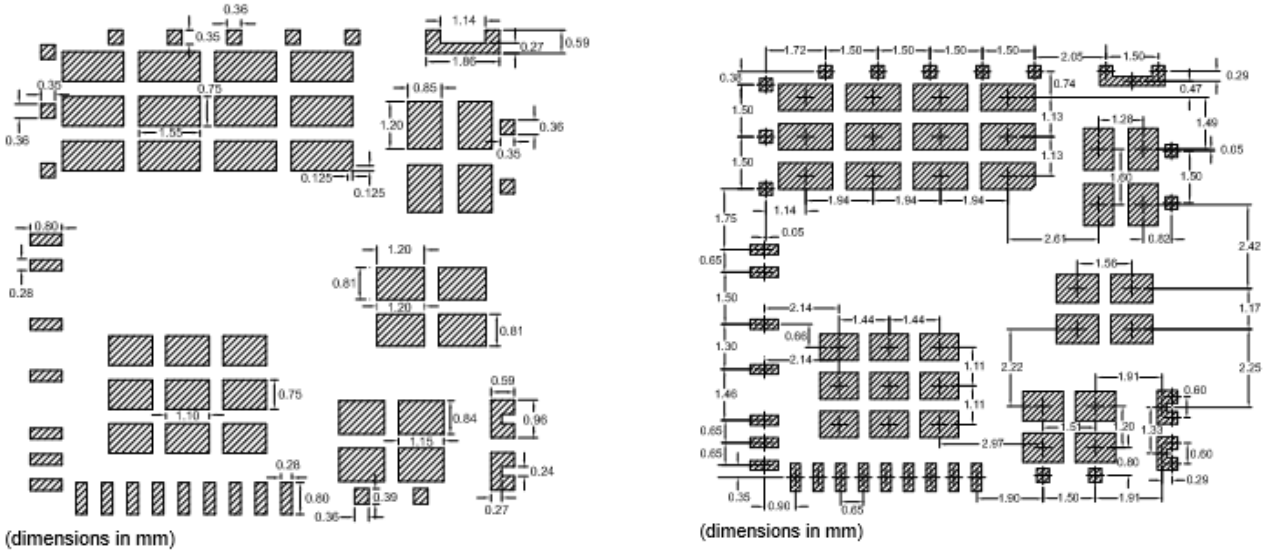


Figure A.4.3 (a and b) *12x12 (36L) 0.127 mm stencil design*

If you want to use a thicker stencil, 0.150 mm (0.006"), use the pad sizes shown in Figure A.3.4 with the pad spacings shown in Figure A.3.3(b).

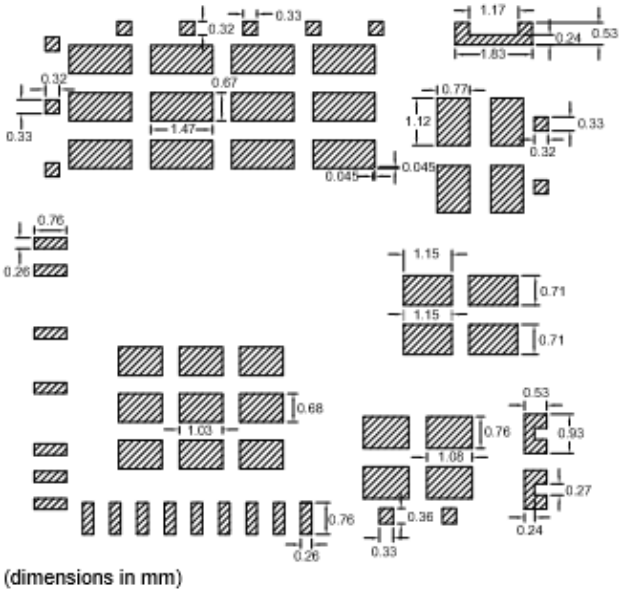


Figure A.3.4 *12x12 (36L) 0.150 mm stencil design*

6.5 QFN 12x12 (37L)

Device outline

Figure A.5.1 shows the outline for these devices. The relative pad positions are controlled to an accuracy of ±0.050 mm. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.

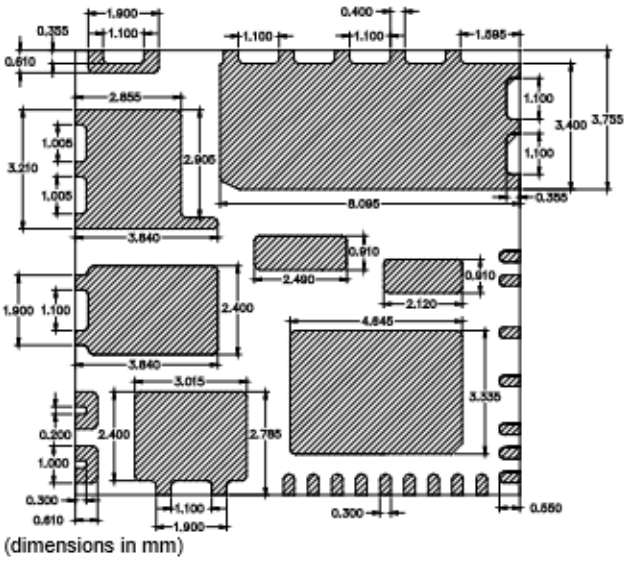


Figure A.5.1 *12x12 (37L) device outline*

6.5.1 Substrate/PCB layout

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout shown in Figure A.5.2 (a, b and c).

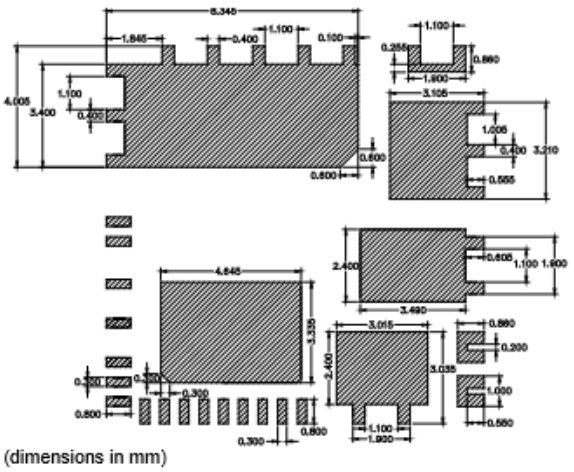


Figure A.5.2(a) *12x12 (37L) substrate/PCB layout*

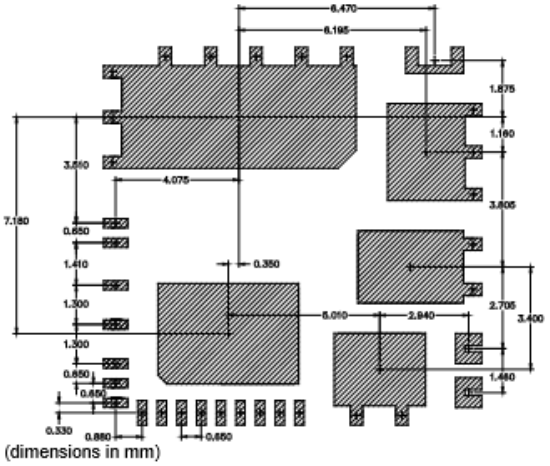


Figure A.5.2(b) *12x12 (37L) 0.127 mm stencil design*

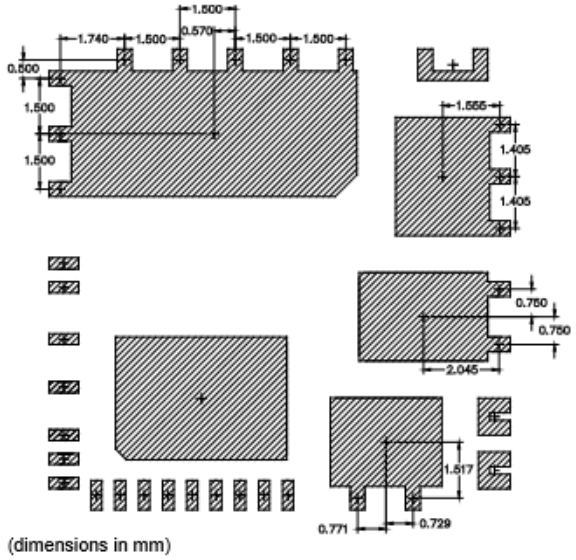


Figure A.5.2(c) *12x12 (37L) substrate/PCB layout*

6.5.2 Stencil Design

Evaluations have shown that the best overall performance is achieved using the stencil design shown in Figure A.5.3 (a and b). This design is for a stencil thickness of 0.127 mm (0.005").

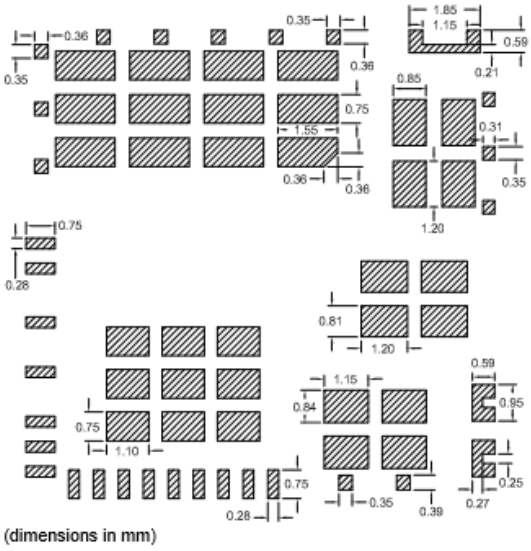


Figure A.5.3(a) *12x12 (37L) 0.127 mm stencil design design*

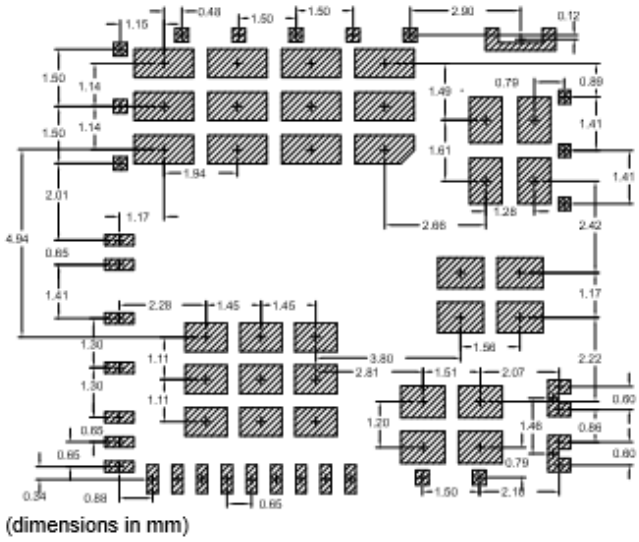


Figure A.5.3(b) *12x12 (37L) 0.127 mm stencil*

If you want to use a thicker stencil, 0.150 mm (0.006"), use the pad sizes shown in Figure A.5.4 with the pad spacings shown in Figure A.5.3(b).

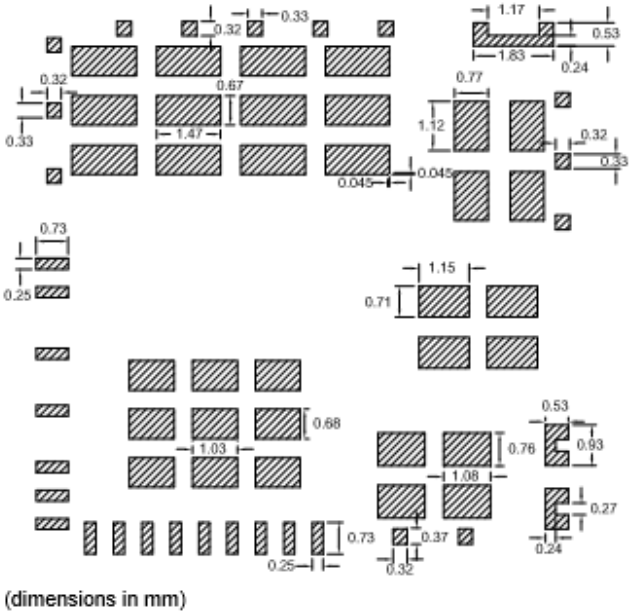


Figure A.5.4 *12x12 (37L) 0.150 mm stencil design*

Revision history

Document version	Date of release	Description of changes
V2.0	2018-08-13	Updated the formatting to Infineon standards

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