

LM2904-Q1, LM2904B-Q1 Industry-Standard Dual Operational Amplifiers for Automotive Applications

1 Features

- AEC Q-100 qualified for automotive applications
 - Temperature grade 1: –40°C to +125°C
 - Device HBM ESD classification 2
 - Device CDM ESD classification C5
- Wide supply range of 3 V to 36 V (LM2904B-Q1)
- Supply-current of 300 µA per channel (LM2904B-Q1, typical)
- Unity-gain bandwidth of 1.2 MHz (LM2904B-Q1)
- Common-mode input voltage range includes ground, enabling direct sensing near ground
- Low input offset voltage of 3 mV at 25°C (LM2904B-Q1, maximum)
- Internal RF and EMI filter (LM2904B-Q1)
- **Functional Safety-Capable**
 - [Documentation available to aid functional safety system design](#)

2 Applications

- [Automotive lighting](#)
- [Body electronics](#)
- [Automotive head unit](#)
- [Telematics control unit](#)
- [Emergency call \(eCall\)](#)
- [Passive safety: brake system](#)
- Electric vehicle / hybrid electric:
 - [Inverter and motor control](#)
 - [On-board \(OBC\) and wireless charger](#)
 - [Battery management system \(BMS\)](#)

3 Description

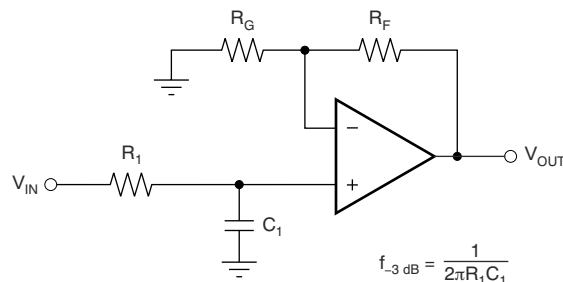
The LM2904-Q1 and LM2904B-Q1 are industry-standard operational amplifiers that have been qualified for automotive use in accordance to the AEC-Q100 specifications. The LM2904B-Q1 is the next-generation version of the LM2904-Q1, which include two high-voltage (36 V) operational amplifiers (op amps). The LM2904B-Q1 provides outstanding value for cost-sensitive applications, with features including low offset (1 mV, typical), common-mode input range to ground, and high differential input voltage capability.

The LM2904B-Q1 simplifies circuit design with enhanced features such as unity-gain stability, lower offset voltage of 1 mV (typical), and lower quiescent current of 300 µA (typical). High ESD (2 kV, HBM) and integrated EMI and RF filters enable the LM2904B-Q1 devices to be used in the most rugged, environmentally challenging applications for the automotive marketplace.

Device Information

PART NUMBER ⁽¹⁾	PACKAGE	BODY SIZE (NOM)
LM2904B-Q1	SOIC (8)	4.90 mm × 3.90 mm
	TSSOP (8)	3.00 mm × 4.40 mm
	VSSOP (8)	3.00 mm × 3.00 mm
LM2904-Q1	SOIC (8)	4.90 mm × 3.90 mm
	TSSOP (8)	3.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1 C_1}\right)$$

Single-Pole, Low-Pass Filter



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (June 2020) to Revision J (February 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added Functional Safety-Capable feature and link to supporting document in <i>Features</i> section	1
• Deleted preview tag on VSSOP (8) package throughout the data sheet.....	1
• Deleted SOT-23 (8) package information throughout the data sheet.....	1
• Deleted preview tag from VSSOP package in <i>Pin Configuration and Functions</i> section.....	5
• Deleted DDF (SOT23-8) package in <i>Pin Configuration and Functions</i> section.....	5
• Updated VSSOP package thermal information in <i>Thermal Information</i> section.....	7

Changes from Revision H (December 2019) to Revision I (June 2020)	Page
• Added applications link in <i>Application</i> section.....	1
• Deleted preview tag on TSSOP (8) package in <i>Device Information</i> table	1
• Added information on VSSOP-8 package to <i>Device Information</i> table.....	1
• Added information on VSSOP-8 package to the <i>Device Comparison Table</i> section.....	4
• Deleted preview tag on TSSOP-8 package in the <i>Device Comparison Table</i> section.....	4
• Deleted preview tag from TSSOP package in <i>Pin Configuration and Functions</i> section.....	5
• Added VSSOP package information in <i>Pin Configuration and Functions</i> section.....	5
• Added VSSOP package to <i>Thermal Information</i> table	7
• Changed section title from <i>Community Resources</i> to <i>Support Resources</i> in the <i>Device and Documentation Support</i> section.....	24

Changes from Revision G (February 2019) to Revision H (December 2019)	Page
• Added information on SOT23-8 package to Device Information table.....	1
• Added information on SOT23-8 package to the <i>Device Comparison Table</i>	4
• Added the <i>Typical Characteristics</i> section for the LM2904B-Q1 device.....	10
• Added test circuit for THD+N and small-signal step response, $G = -1$ in the <i>Parameter Measurement Information</i> section.....	17
• Changed specific voltages to a <i>Recommended Operating Conditions</i> reference.....	18

- Changed the functional block diagram for LM2904B-Q1 in the *Detailed Description* section..... 18

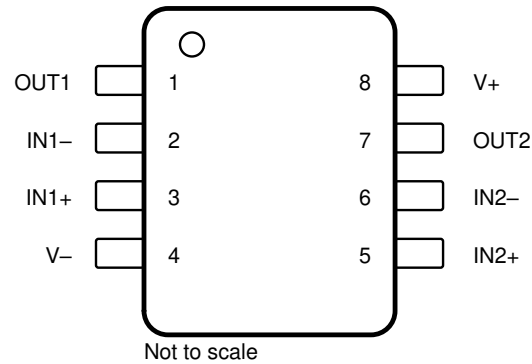
Changes from Revision F (April 2008) to Revision G (February 2019) Page

- Added *Applications* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
 - Added new device to data sheet..... 1
 - Added AEC-Q100 qualification statement..... 1
-

5 Device Comparison Table

PART NUMBER	SUPPLY VOLTAGE	AMBIENT TEMPERATURE RANGE	V_{OS} (MAXIMUM AT 25°C)	I_Q / CH (TYPICAL AT 25°C)	INTEGRATED EMI FILTER	PACKAGE
LM2904B-Q1	3 V to 36 V	-40°C to 125°C	3 mV	300 μ A	Yes	D, DGK, PW
LM2904-Q1	3 V to 26 V	-40°C to 125°C	7 mV	350 μ A	No	D, PW
LM2904V-Q1	3 V to 32 V	-40°C to 125°C	7 mV	350 μ A	No	D, PW
LM2904AV-Q1	3 V to 32 V	-40°C to 125°C	2 mV	350 μ A	No	D, PW

6 Pin Configuration and Functions



**Figure 6-1. D, DGK, and PW Package
 8-Pin SOIC, VSSOP, and TSSOP
 Top View**

Table 6-1. Pin Functions

PIN ⁽¹⁾		I/O	DESCRIPTION
NAME	NO.		
IN1-	2	I	Negative input
IN1+	3	I	Positive input
IN2-	6	I	Negative input
IN2+	5	I	Positive input
OUT1	1	O	Output
OUT2	7	O	Output
V-	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

(1) For a listing of which devices are available in what packages, see [Section 5](#).

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
Supply voltage, $V_S = ([V+] - [V-])$	LM2904B-Q1		40	V	
	LM2904V-Q1, LM2904AV-Q1		32		
	LM2904-Q1		26		
Differential input voltage, V_{ID} ⁽²⁾	LM2904B-Q1, LM2904V-Q1, LM2904AV-Q1	-32	32	V	
	LM2904-Q1	-26	26		
Input voltage, V_I	Either input	LM2904B-Q1	-0.3	40	V
		LM2904V-Q1, LM2904AV-Q1	-0.3	32	
		LM2904-Q1	-0.3	26	
Duration of output short circuit (one amplifier) to V_- at (or below) $T_A = 25^\circ\text{C}$, $V_S \leq 15\text{ V}$ ⁽³⁾		Unlimited		s	
Operating ambient temperature, T_A		-40	125	$^\circ\text{C}$	
Operating virtual-junction temperature, T_J			150	$^\circ\text{C}$	
Storage temperature, T_{stg}		-65	150	$^\circ\text{C}$	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Differential voltages are at $IN+$, with respect to $IN-$.
- (3) Short circuits from outputs to the supply pins can cause excessive heating and eventual destruction.

7.2 ESD Ratings

		VALUE	UNIT
LM2904B-Q1			
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	± 2000	V
	Charged-device model (CDM), per AEC Q100-011	± 750	
LM2904-Q1, LM2904AV-Q1, AND LM2904V-Q1			
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	± 1000	V
	Charged-device model (CDM), per AEC Q100-011	± 500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V _S	Supply voltage, V _S = ([V+] – [V–])	LM2904B-Q1	3	36	V
		LM2904AV-Q1, LM2904V-Q1	3	30	
		LM2904-Q1	3	26	
V _{CM}	Common-mode voltage	V–	(V+) – 2	V	
T _A	Operating ambient temperature	–40	125	°C	

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM2904-Q1, LM2904AV-Q1, LM2904B-Q1, LM2904V-Q1 ⁽²⁾			UNIT
		D (SOIC)	DGK (VSSOP)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	124.7	186.1	171.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	66.9	77.1	68.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	67.9	107.7	99.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	19.2	17.2	11.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	67.2	106.1	97.9	°C/W

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).
(2) For a listing of which devices are available in what packages, see [Section 5](#).

7.5 Electrical Characteristics: LM2904B-Q1

$V_S = (V+) - (V-) = 5\text{ V} - 36\text{ V} (\pm 2.5\text{ V} - \pm 18\text{ V})$, $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{k}$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	LM2904B-Q1			± 0.3	± 3.0	mV
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			± 4	
dV_{OS}/dT	Input offset voltage drift		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ (1)		± 3.5	12	$\mu\text{V}/^\circ\text{C}$
PSRR	Power supply rejection ratio				± 2	15	$\mu\text{V}/\text{V}$
	Channel separation, dc	$f = 1\text{ kHz}$ to 20 kHz			± 1		$\mu\text{V}/\text{V}$
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range	$V_S = 3\text{ V}$ to 36 V		(V-)	(V+) - 1.5		V
		$V_S = 5\text{ V}$ to 36 V	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	(V-)	(V+) - 2		
CMRR	Common-mode rejection ratio	$(V-) \leq V_{CM} \leq (V+) - 1.5\text{ V}$	$V_S = 3\text{ V}$ to 36 V		20	100	$\mu\text{V}/\text{V}$
		$(V-) \leq V_{CM} \leq (V+) - 2.0\text{ V}$	$V_S = 5\text{ V}$ to 36 V	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	25	316	
INPUT BIAS CURRENT							
I_B	Input bias current				± 10	± 35	nA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ (1)			± 50	
I_{OS}	Input offset current				0.5	4	nA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ (1)			5	
dI_{OS}/dT	Input offset current drift		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		10		$\text{pA}/^\circ\text{C}$
NOISE							
E_n	Input voltage noise	$f = 0.1$ to 10 Hz			3		μV_{PP}
e_n	Input voltage noise density	$f = 1\text{ kHz}$			40		$\text{nV}/\sqrt{\text{Hz}}$
INPUT IMPEDANCE							
Z_{ID}	Differential				$10 \parallel 0.1$		$\text{M}\Omega \parallel \text{pF}$
Z_{IC}	Common-mode				$4 \parallel 1.5$		$\text{G}\Omega \parallel \text{pF}$
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	$V_S = 15\text{ V}$; $V_O = 1\text{ V}$ to 11 V ; $R_L \geq 10\text{ k}\Omega$, connected to (V-)			70	140	V/mV
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		35		
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				1.2		MHz
SR	Slew rate	$G = +1$			0.5		V/ μs
ϕ_m	Phase margin	$G = +1$, $R_L = 10\text{ k}\Omega$, $C_L = 20\text{ pF}$			56		$^\circ$
t_{OR}	Overload recovery time	$V_{IN} \times \text{gain} > V_S$			10		μs
t_s	Settling time	To 0.1%, $V_S = 5\text{ V}$, 2-V step, $G = +1$, $C_L = 100\text{ pF}$			4		μs
THD+N	Total harmonic distortion + noise	$G = +1$, $f = 1\text{ kHz}$, $V_O = 3.53\text{ V}_{RMS}$, $V_S = 36\text{ V}$, $R_L = 100\text{k}$, $I_{OUT} \leq \pm 50\text{ }\mu\text{A}$, $\text{BW} = 80\text{ kHz}$			0.001%		
OUTPUT							
V_O	Voltage output swing from rail	Positive rail (V+)		$I_{OUT} = 50\text{ }\mu\text{A}$	1.35	1.42	V
				$I_{OUT} = 1\text{ mA}$	1.4	1.48	
				$I_{OUT} = 5\text{ mA}$ (1)	1.5	1.61	
		Negative rail (V-)		$I_{OUT} = 50\text{ }\mu\text{A}$	100	150	mV
				$I_{OUT} = 1\text{ mA}$	0.75	1	V
		$V_S = 5\text{ V}$, $R_L \leq 10\text{ k}\Omega$ connected to (V-)	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	5	20	mV	
I_O	Output current	$V_S = 15\text{ V}$; $V_O = V-$; $V_{ID} = 1\text{ V}$	Source(1)		-20	-30	mA
				$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-10		
		$V_S = 15\text{ V}$; $V_O = V+$; $V_{ID} = -1\text{ V}$	Sink(1)		10	20	
				$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	5		
		$V_{ID} = -1\text{ V}$; $V_O = (V-) + 200\text{ mV}$		60	100	μA	
I_{SC}	Short-circuit current	$V_S = 20\text{ V}$, (V+) = 10 V , (V-) = -10 V , $V_O = 0\text{ V}$			± 40	± 60	mA
C_{LOAD}	Capacitive load drive				100		pF
R_O	Open-loop output resistance	$f = 1\text{ MHz}$, $I_O = 0\text{ A}$			300		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	$V_S = 5\text{ V}$; $I_O = 0\text{ A}$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		300	460	μA
		$V_S = 36\text{ V}$; $I_O = 0\text{ A}$				800	

(1) Specified by characterization only.

7.6 Electrical Characteristics: LM2904-Q1, LM2904AV-Q1, LM2904V-Q1

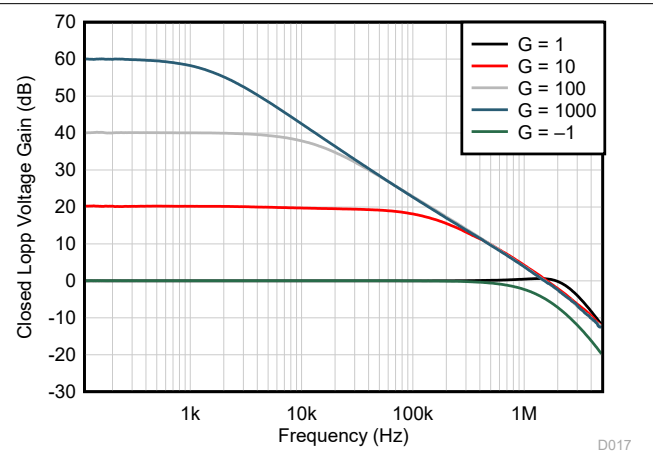
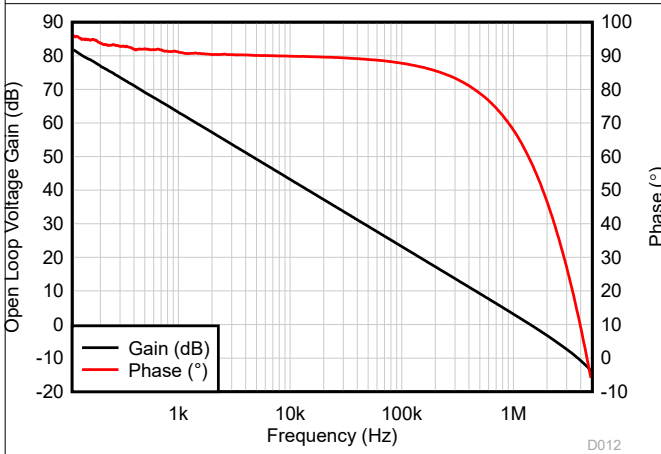
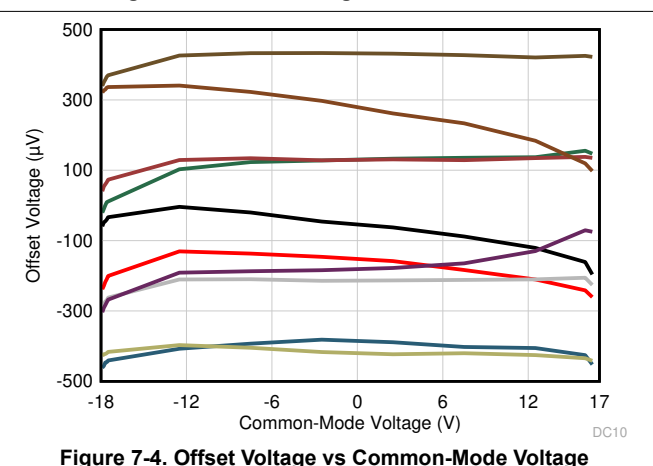
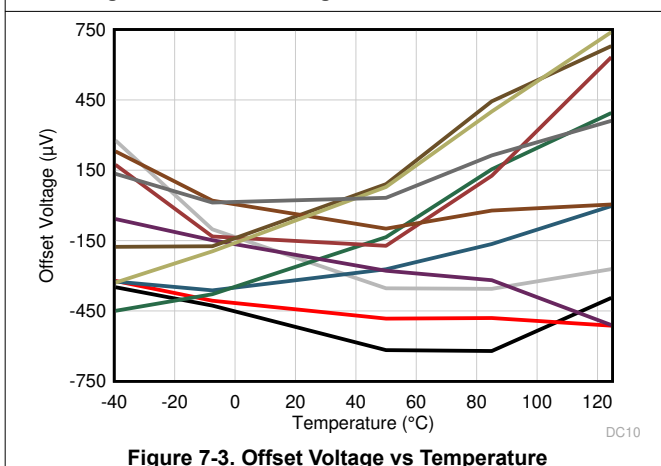
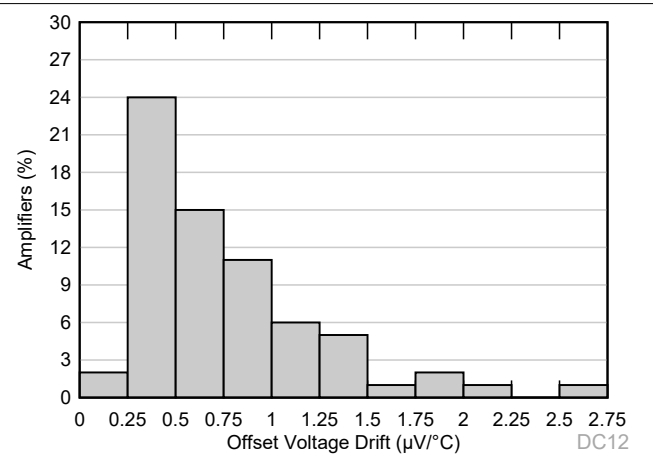
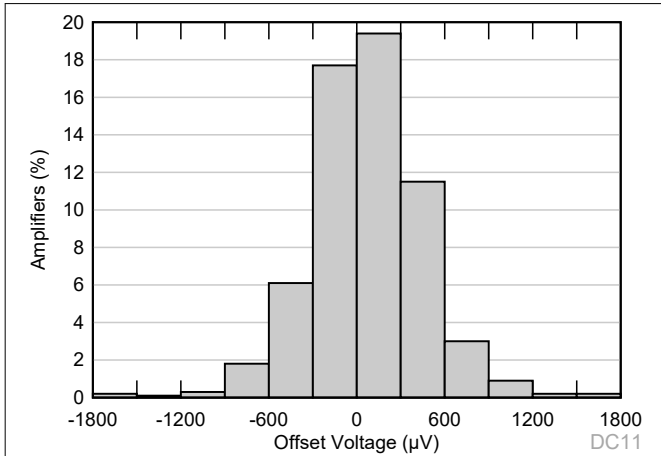
For $V_S = (V_+) - (V_-) = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to V_- (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP	MAX	UNIT		
OFFSET VOLTAGE									
V_{OS}	Input offset voltage	$V_S = 5\text{ V}$ to maximum; $V_{CM} = 0\text{ V}$; $V_O = 1.4\text{ V}$	LM2904-Q1, LM2904V-A1	$T_A = -40^\circ\text{C}$ to 125°C	± 3	± 7	mV		
					± 10				
			LM2904AV-Q1	$T_A = -40^\circ\text{C}$ to 125°C	± 1	± 2			
				$T_A = -40^\circ\text{C}$ to 125°C		± 4			
dV_{OS}/dT	Input offset voltage drift			$T_A = -40^\circ\text{C}$ to 125°C	± 7		$\mu\text{V}/^\circ\text{C}$		
PSRR	Input offset voltage vs power supply ($\Delta V_{IO}/\Delta V_S$)	$V_S = 5\text{ V}$ to 30 V			65	100	dB		
V_{O1}/V_{O2}	Channel separation	$f = 1\text{ kHz}$ to 20 kHz				120	dB		
INPUT VOLTAGE RANGE									
V_{CM}	Common-mode voltage range	$V_S = 5\text{ V}$ to maximum			(V_-)	(V_+) – 1.5	V		
				$T_A = -40^\circ\text{C}$ to 125°C	(V_-)	(V_+) – 2			
CMRR	Common-mode rejection ratio	$V_S = 5\text{ V}$ to maximum; $V_{CM} = 0\text{ V}$			65	80	dB		
INPUT BIAS CURRENT									
I_B	Input bias current	$V_O = (V_-) + 1.4\text{ V}$				–20	–250	nA	
				$T_A = -40^\circ\text{C}$ to 125°C			–500		
I_{OS}	Input offset current	$V_O = (V_-) + 1.4\text{ V}$	LM2904-Q1			2	50	nA	
					$T_A = -40^\circ\text{C}$ to 125°C		300		
				LM2904AV-Q1, LM2904V-Q1			2		50
				$T_A = -40^\circ\text{C}$ to 125°C		150			
dI_{OS}/dT	Input offset current drift			$T_A = -40^\circ\text{C}$ to 125°C	10		$\mu\text{A}/^\circ\text{C}$		
NOISE									
e_n	Input voltage noise density	$f = 1\text{ kHz}$			40		$\text{nV}/\sqrt{\text{Hz}}$		
OPEN-LOOP GAIN									
A_{OL}	Open-loop voltage gain	$V_S = 15\text{ V}$; $V_O = (V_-) + 1\text{ V}$ to $(V_-) + 11\text{ V}$; $R_L \geq 2\text{ k}\Omega$, connected to (V_-)			25	100	V/mV		
				$T_A = -40^\circ\text{C}$ to 125°C	15				
FREQUENCY RESPONSE									
GBW	Gain bandwidth product				0.7		MHz		
SR	Slew rate	$G = +1$			0.3		V/ μs		
OUTPUT									
V_O	Voltage output swing from rail	Positive rail	LM2904-Q1	$V_S = \text{maximum}$; $R_L = 2\text{ k}\Omega$	$T_A = -40^\circ\text{C}$ to 125°C	$V_S = 1.5$		V	
						4			
			LM2904AV-Q1, LM2904V-Q1	$V_S = \text{maximum}$; $R_L \geq 10\text{ k}\Omega$		3			2
						6			4
	Negative rail	$V_S = 5\text{ V}$; $R_L \leq 10\text{ k}\Omega$	$T_A = -40^\circ\text{C}$ to 125°C		5	20	mV		
I_O	Output current	$V_S = 15\text{ V}$; $V_O = V_-$; $V_{ID} = 1\text{ V}$	Source			–20	–30	mA	
					$T_A = -40^\circ\text{C}$ to 125°C	–10			
		$V_S = 15\text{ V}$; $V_O = V_+$; $V_{ID} = -1\text{ V}$	Sink			10	20		
					$T_A = -40^\circ\text{C}$ to 125°C	5			
		$V_{ID} = -1\text{ V}$; $V_O = (V_-) + 200\text{ mV}$	LM2904-Q1			30	μA		
			LM2904AV-Q1, LM2904V-Q1			12	40		
I_{SC}	Short-circuit current	$V_S = 10\text{ V}$; $V_O = V_S / 2$				± 40	± 60	mA	
POWER SUPPLY									
I_Q	Quiescent current per amplifier	$V_O = V_S / 2$; $I_O = 0\text{ A}$			350	600	μA		
		$V_S = \text{maximum}$; $V_O = \text{maximum} / 2$; $I_O = 0\text{ A}$	$T_A = -40^\circ\text{C}$ to 125°C			500		1000	

(1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified. Maximum V_S for testing purposes is 26 V for LM2904-Q1 and 32 V for LM2904AV-Q1/LM2904V-Q1.

7.7 Typical Characteristics

Typical characteristics section is applicable for LM2904B-Q1. The typical characteristics data section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V} (\pm 18\text{ V})$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).



7.7 Typical Characteristics (continued)

Typical characteristics section is applicable for LM2904B-Q1. The typical characteristics data section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V} (\pm 18\text{ V})$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

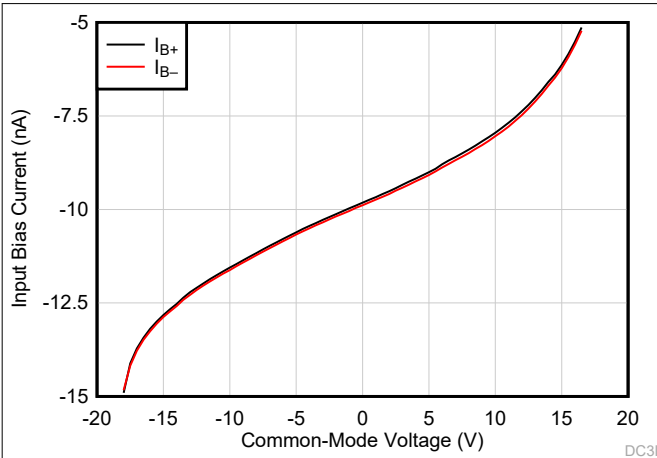


Figure 7-7. Input Bias Current vs Common-Mode Voltage

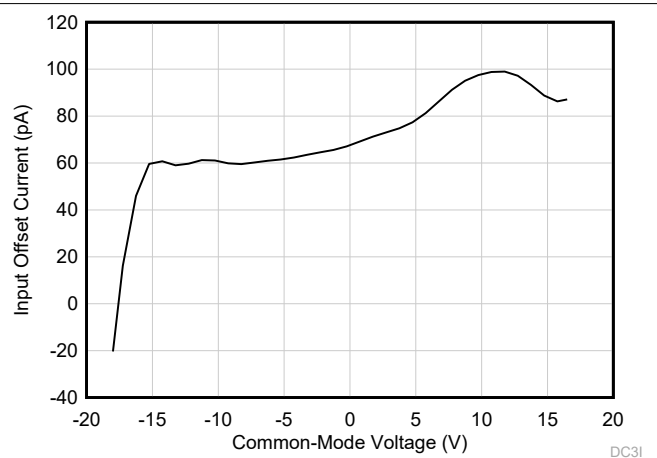


Figure 7-8. Input Offset Current vs Common-Mode Voltage

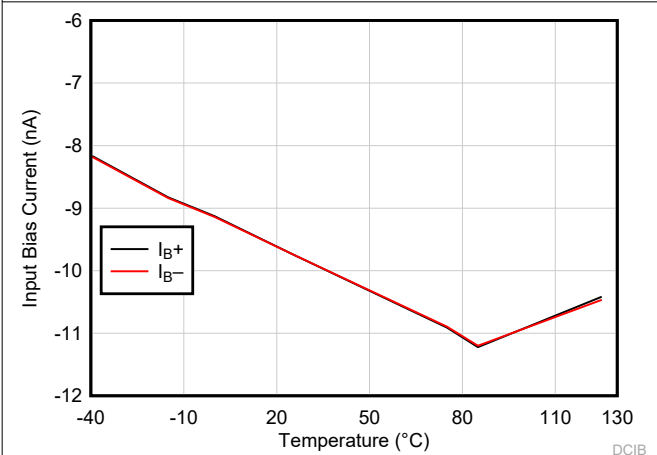


Figure 7-9. Input Bias Current vs Temperature

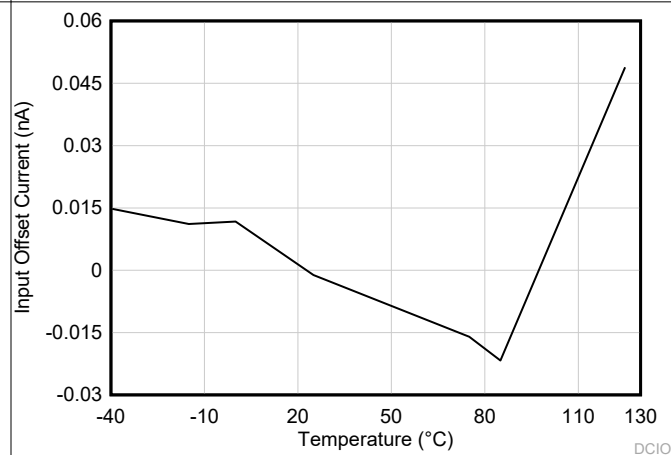


Figure 7-10. Input Offset Current vs Temperature

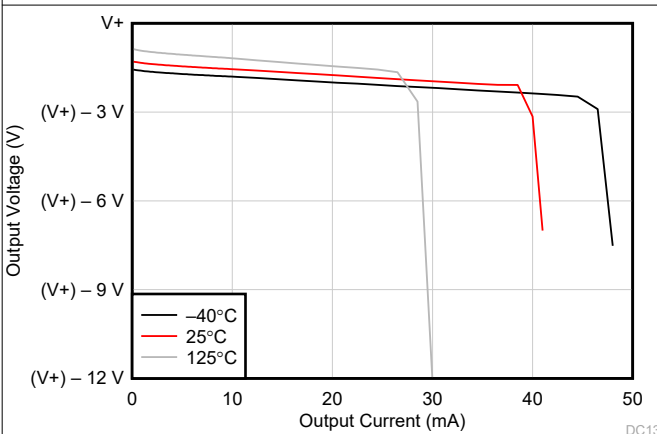


Figure 7-11. Output Voltage Swing vs Output Current (Sourcing)

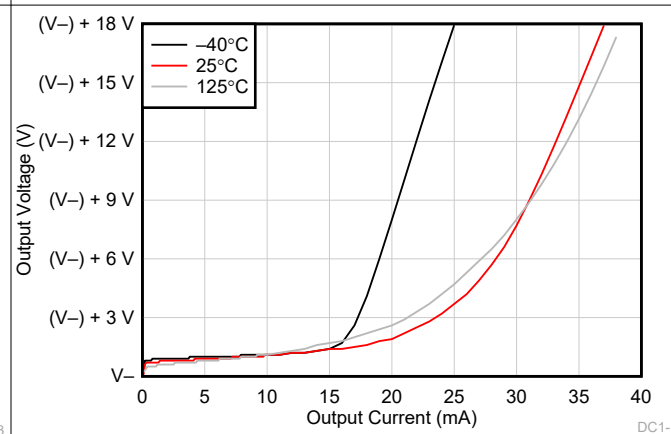
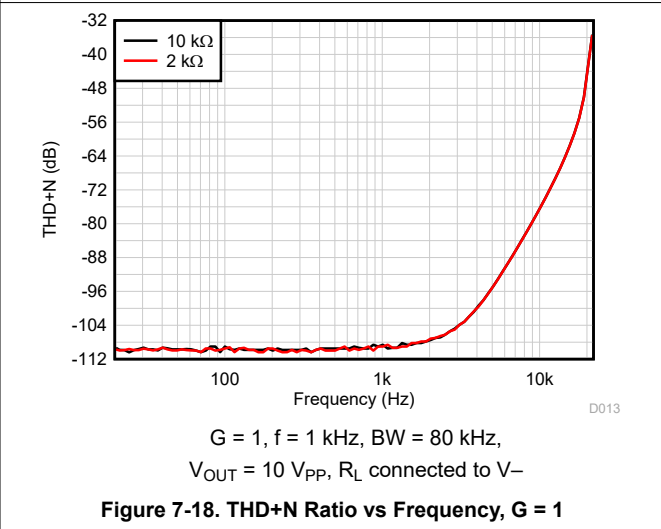
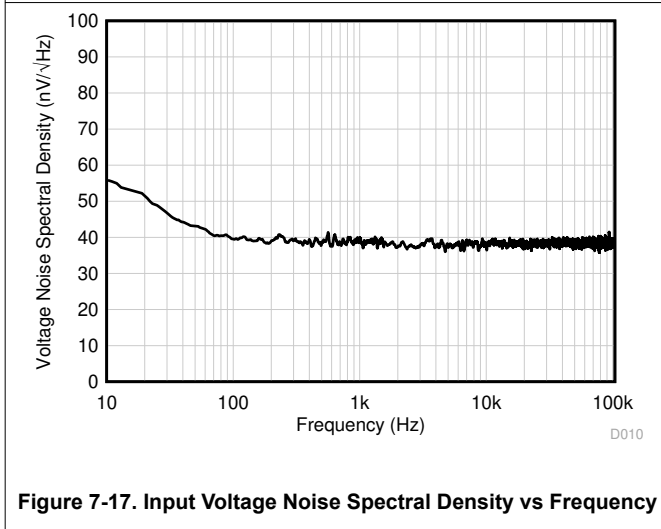
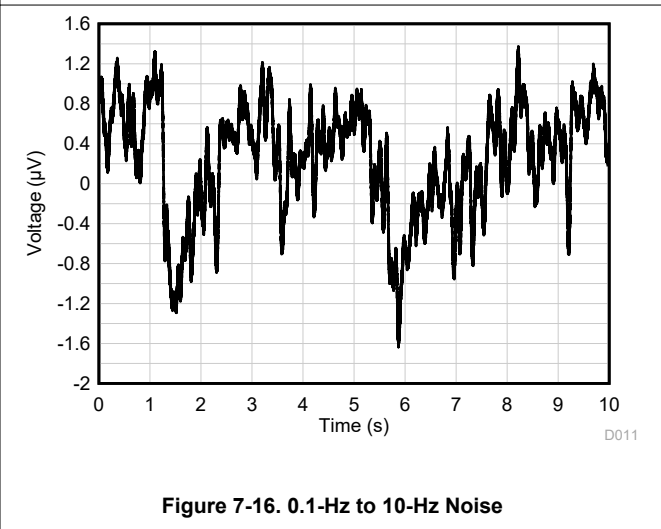
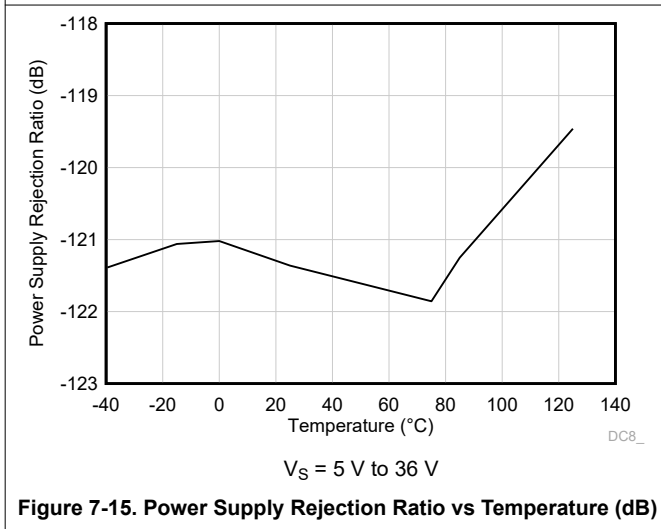
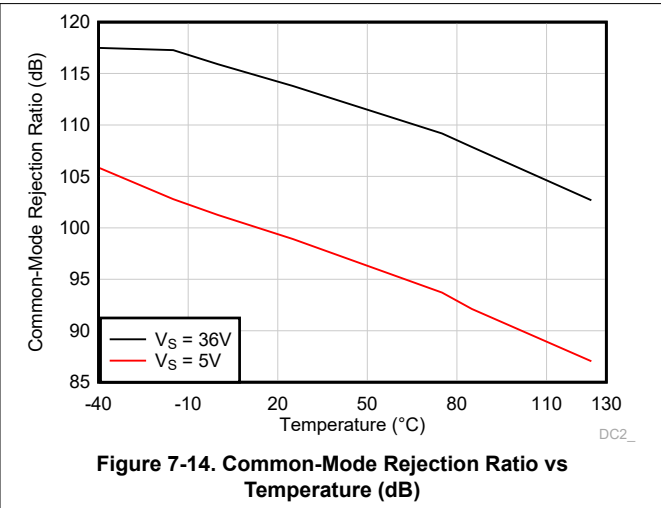
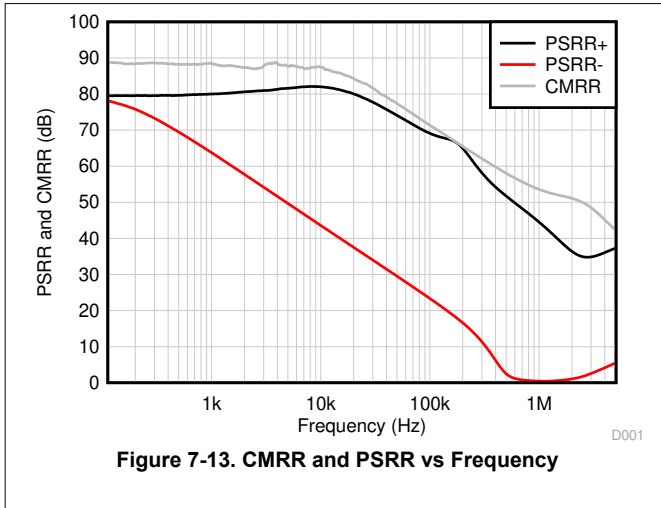


Figure 7-12. Output Voltage Swing vs Output Current (Sinking)

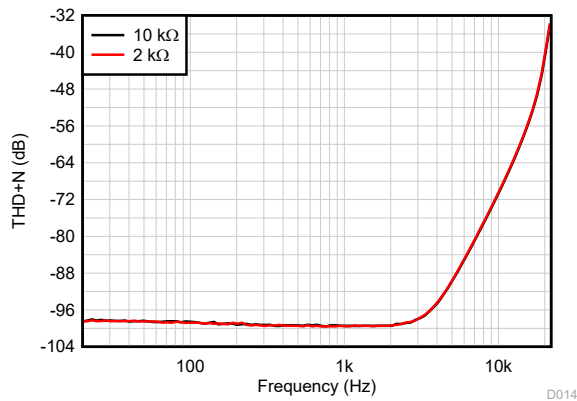
7.7 Typical Characteristics (continued)

Typical characteristics section is applicable for LM2904B-Q1. The typical characteristics data section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V} (\pm 18\text{ V})$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).



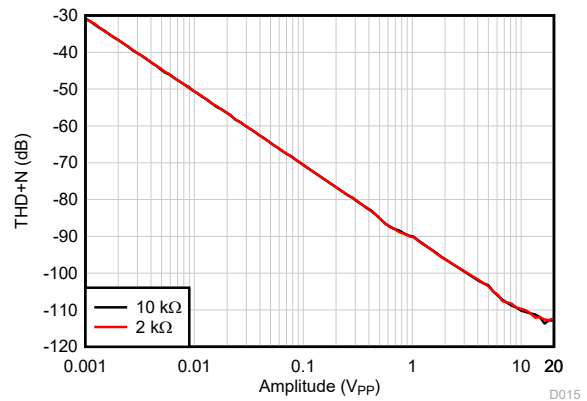
7.7 Typical Characteristics (continued)

Typical characteristics section is applicable for LM2904B-Q1. The typical characteristics data section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V} (\pm 18\text{ V})$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).



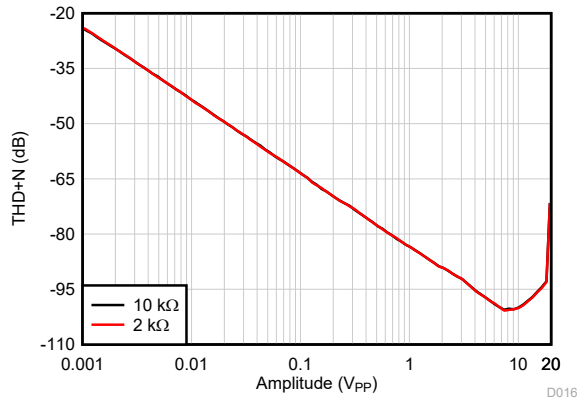
$G = -1$, $f = 1\text{ kHz}$, $BW = 80\text{ kHz}$,
 $V_{OUT} = 10\text{ V}_{PP}$, R_L connected to V_-
See [Figure 8-3](#)

Figure 7-19. THD+N Ratio vs Frequency, $G = -1$



$G = 1$, $f = 1\text{ kHz}$, $BW = 80\text{ kHz}$,
 R_L connected to V_-

Figure 7-20. THD+N vs Output Amplitude, $G = 1$



$G = -1$, $f = 1\text{ kHz}$, $BW = 80\text{ kHz}$,
 R_L connected to V_-
See [Figure 8-3](#)

Figure 7-21. THD+N vs Output Amplitude, $G = -1$

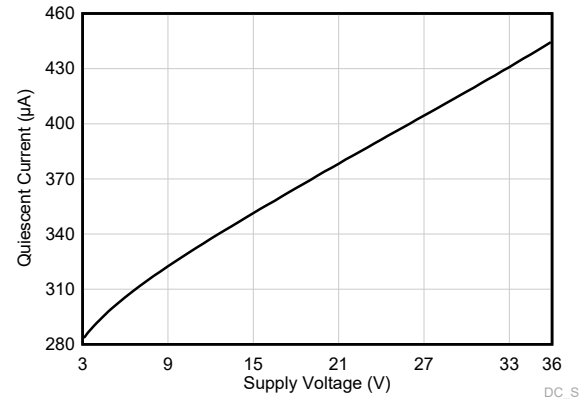


Figure 7-22. Quiescent Current vs Supply Voltage

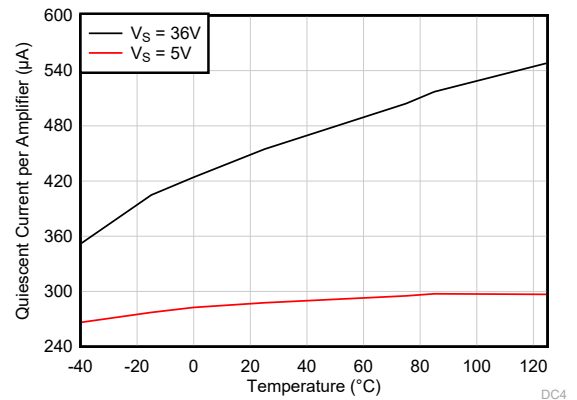


Figure 7-23. Quiescent Current vs Temperature

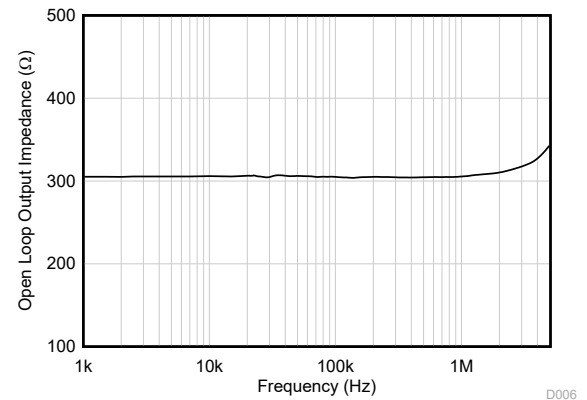


Figure 7-24. Open-Loop Output Impedance vs Frequency

7.7 Typical Characteristics (continued)

Typical characteristics section is applicable for LM2904B-Q1. The typical characteristics data section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V} (\pm 18\text{ V})$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

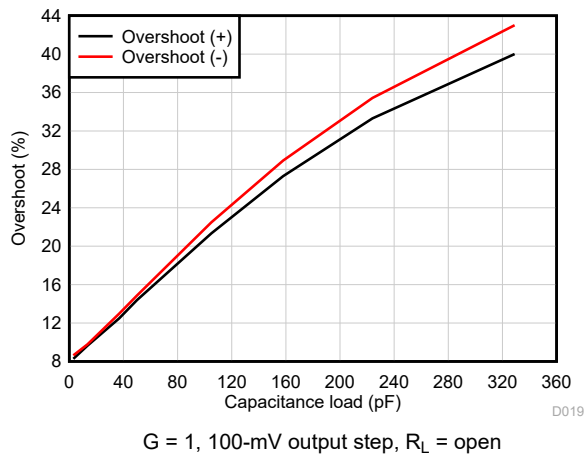


Figure 7-25. Small-Signal Overshoot vs Capacitive Load

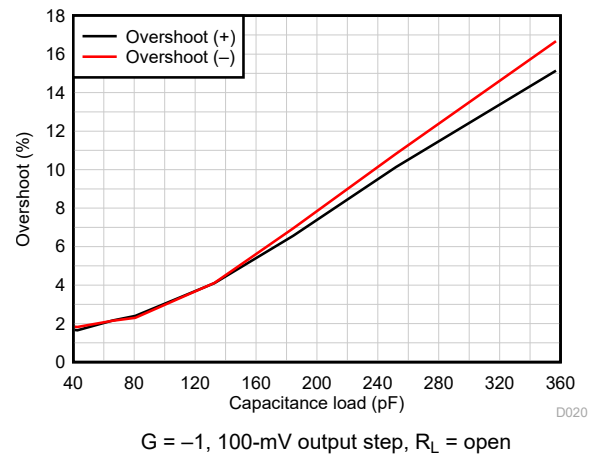


Figure 7-26. Small-Signal Overshoot vs Capacitive Load

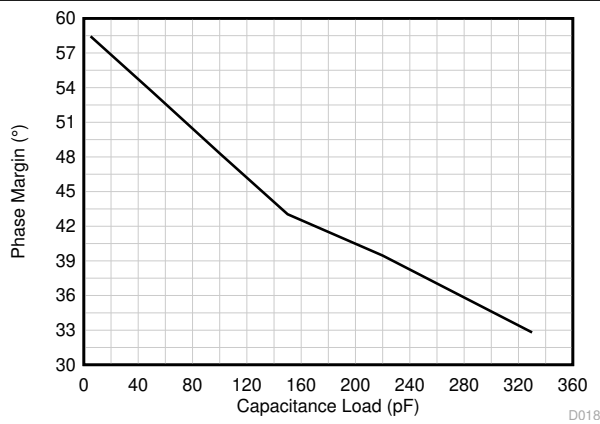


Figure 7-27. Phase Margin vs Capacitive Load

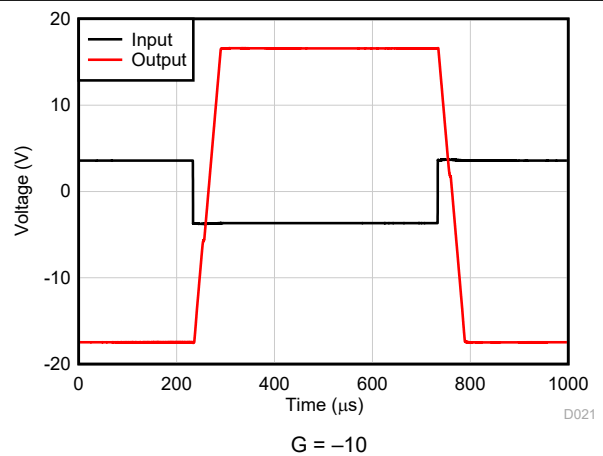


Figure 7-28. Overload Recovery

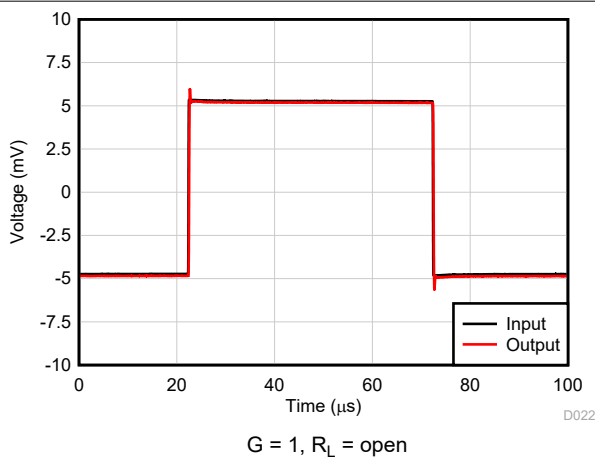


Figure 7-29. Small-Signal Step Response, G = 1

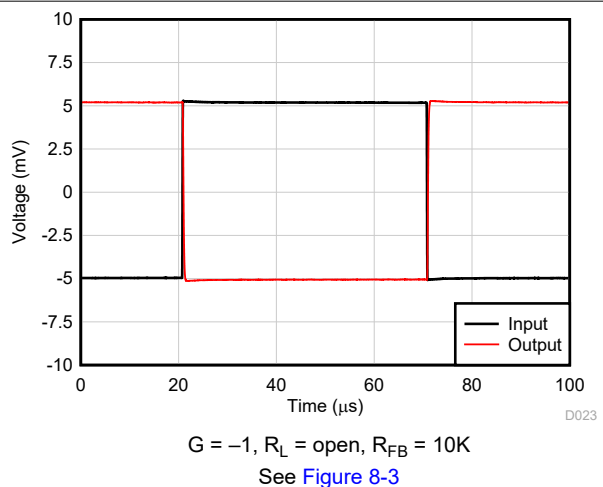
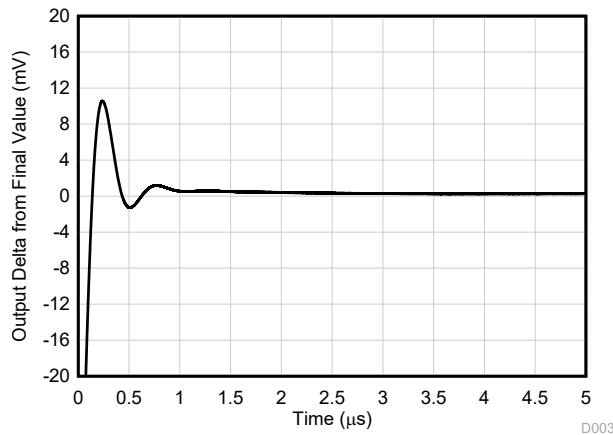


Figure 7-30. Small-Signal Step Response, G = -1

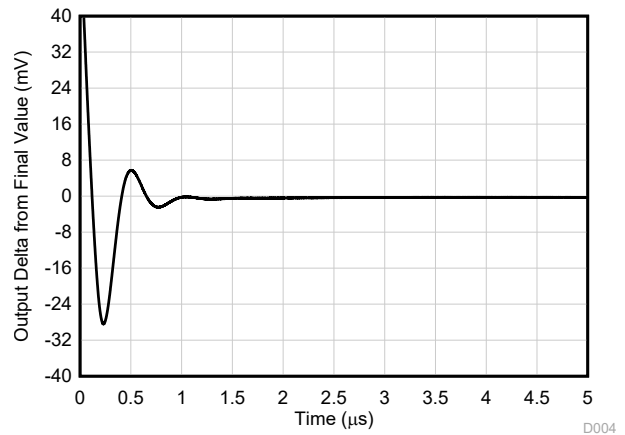
7.7 Typical Characteristics (continued)

Typical characteristics section is applicable for LM2904B-Q1. The typical characteristics data section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V} (\pm 18\text{ V})$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).



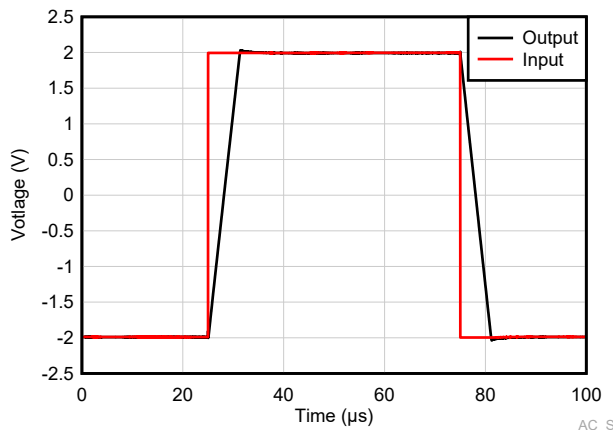
$G = 1$, $R_L = \text{open}$

Figure 7-31. Large-Signal Step Response (Rising)



$G = 1$, $R_L = \text{open}$

Figure 7-32. Large-Signal Step Response (Falling)



$G = 1$, $R_L = \text{open}$

Figure 7-33. Large-Signal Step Response

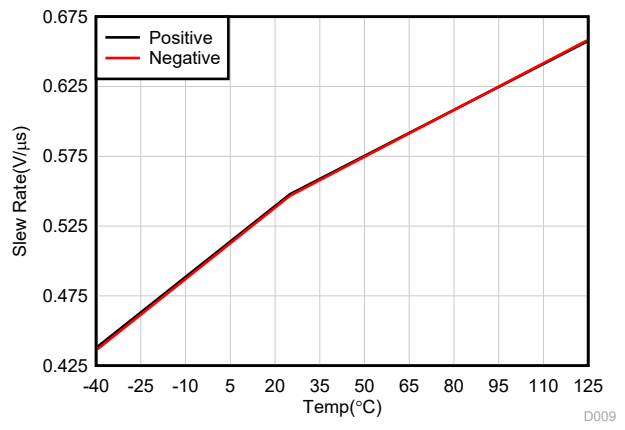


Figure 7-34. Slew Rate vs Temperature

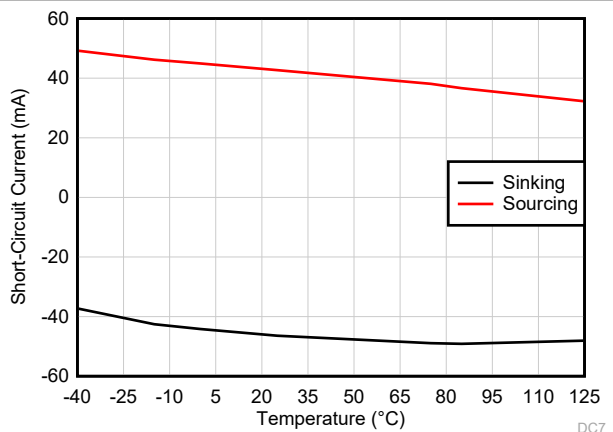
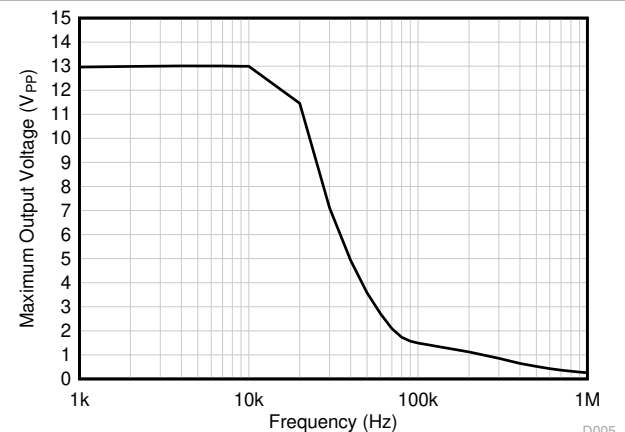


Figure 7-35. Short-Circuit Current vs Temperature



$V_S = 15\text{ V}$

Figure 7-36. Maximum Output Voltage vs Frequency

7.7 Typical Characteristics (continued)

Typical characteristics section is applicable for LM2904B-Q1. The typical characteristics data section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V} (\pm 18\text{ V})$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

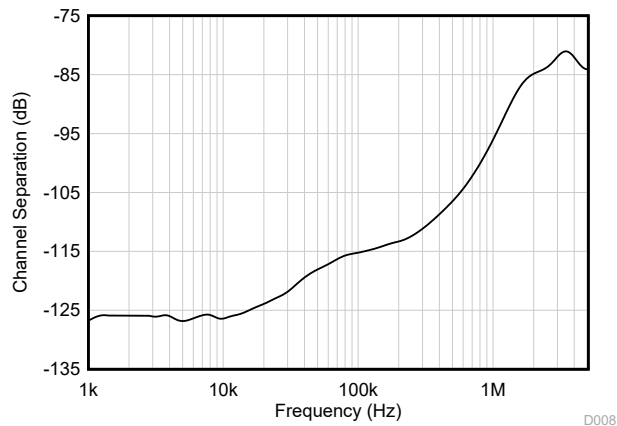


Figure 7-37. Channel Separation vs Frequency

D008

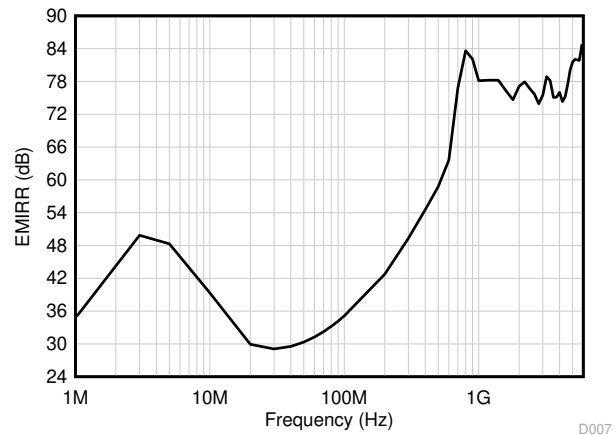


Figure 7-38. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

D007

8 Parameter Measurement Information

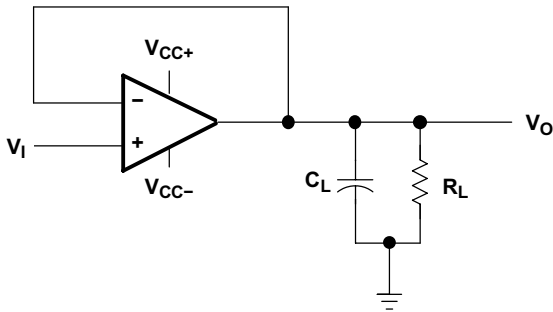


Figure 8-1. Unity-Gain Amplifier

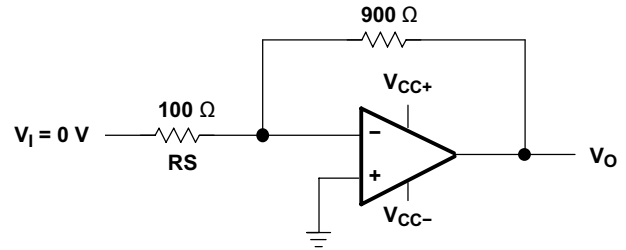


Figure 8-2. Noise-Test Circuit

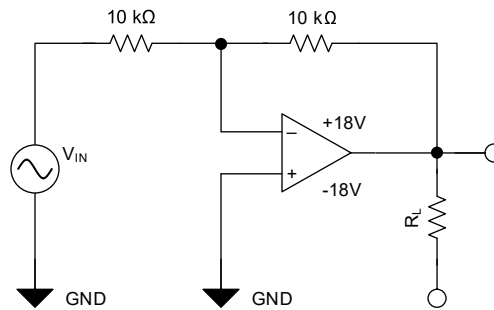


Figure 8-3. Test Circuit, $G = -1$, for THD+N and Small-Signal Step Response

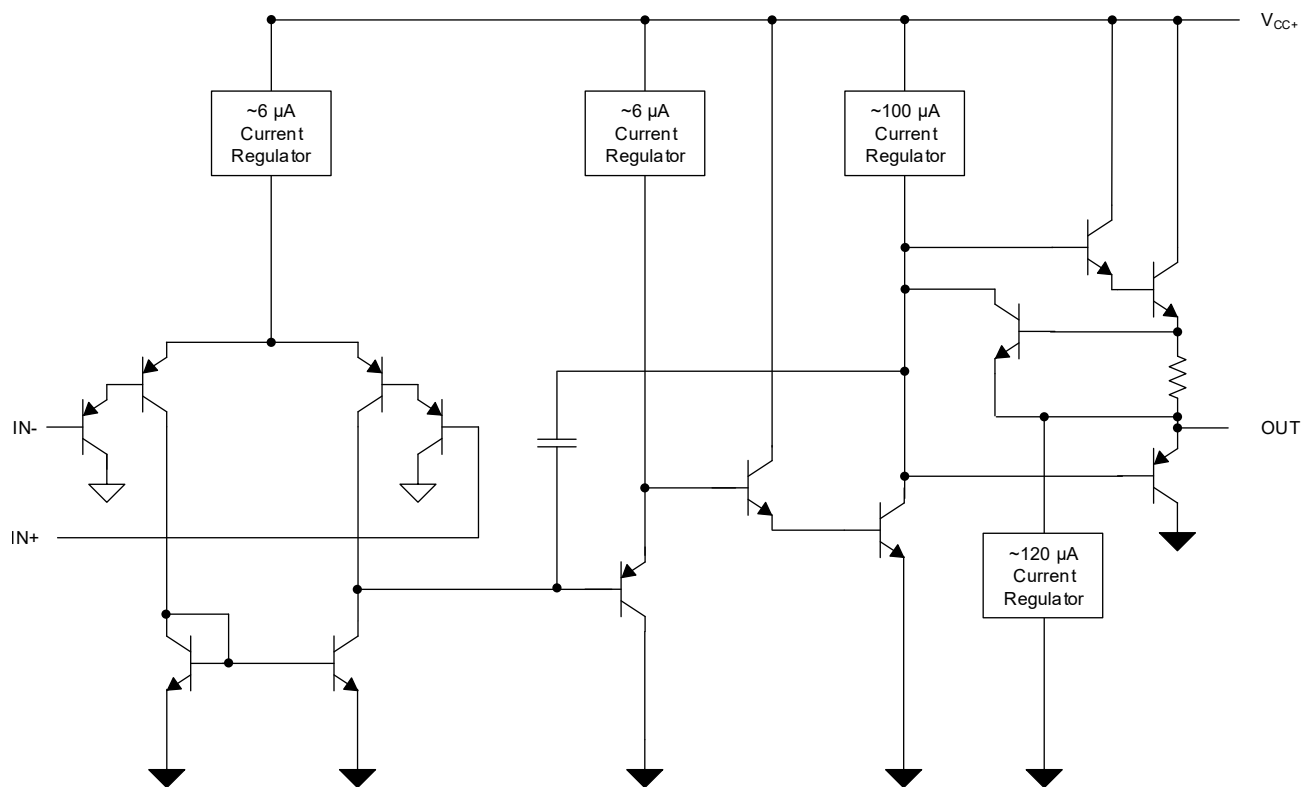
9 Detailed Description

9.1 Overview

The LM2904-Q1 and LM2904B-Q1 devices consist of two independent, high-gain frequency-compensated operational amplifiers designed to operate from a single supply over a wide range of voltages. Operation from split supplies also is possible if the difference between the two supplies is within the supply voltage range specified in [Section 7.3](#), and V_S is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, DC amplification blocks, and all the conventional operational amplifier circuits that now can be implemented more easily in single-supply-voltage systems. For example, these devices can be operated directly from the standard 5-V supply used in digital systems and easily can provide the required interface electronics without additional ± 5 -V supplies.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. These devices have a 1.2-MHz unity-gain bandwidth (LM2904B-Q1).

9.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 0.5-V/ μ s slew rate (LM2904B-Q1).

9.3.3 Input Common Mode Range

The valid common mode range is from device ground to $V_S - 1.5$ V ($V_S - 2$ V across temperature). Inputs may exceed V_S up to the maximum V_S without device damage. At least one input must be in the valid input common-mode range for the output to be the correct phase. If both inputs exceed the valid range, then the output phase is undefined. If either input more than 0.3 V below V_- then input current should be limited to 1 mA and the output phase is undefined.

9.4 Device Functional Modes

The LM2904-Q1 and LM2904B-Q1 devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier, depending on the application.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The LM2904-Q1 and LM2904B-Q1 operational amplifiers are useful in a wide range of signal conditioning applications. Inputs can be powered before V_S for flexibility in multiple supply circuits. For full application design guidelines related to this family of devices, please refer to the application report [Application design guidelines for LM324/LM358 devices](#).

10.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

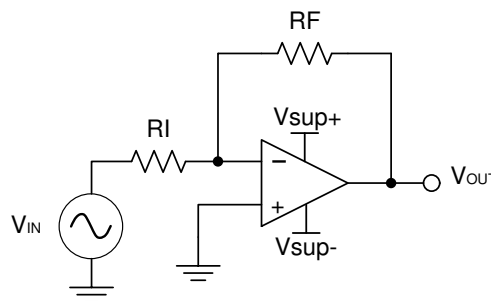


Figure 10-1. Application Schematic

10.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application scales a signal of ± 0.5 V to ± 1.8 V. Setting the supply at ± 12 V is sufficient to accommodate this application.

10.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using [Equation 1](#) and [Equation 2](#):

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for R_I or R_F . Choosing a value in the kilohm range is desirable because the amplifier circuit uses currents in the milliamperere range. This ensures the part does not draw too much current. This example uses $10 \text{ k}\Omega$ for R_I which means $36 \text{ k}\Omega$ is used for R_F . This was determined by [Equation 3](#).

$$A_V = -\frac{R_F}{R_I} \quad (3)$$

10.2.3 Application Curve

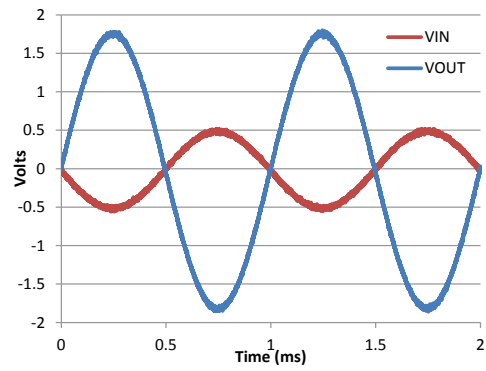


Figure 10-2. Input and Output Voltages of the Inverting Amplifier

11 Power Supply Recommendations

CAUTION

Supply voltages larger than specified in the recommended operating region can permanently damage the device (see [Section 7.1](#)).

Place 0.1- μ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [Section 12](#).

12 Layout

12.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V_+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance, as shown in Section 12.2.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

12.2 Layout Examples

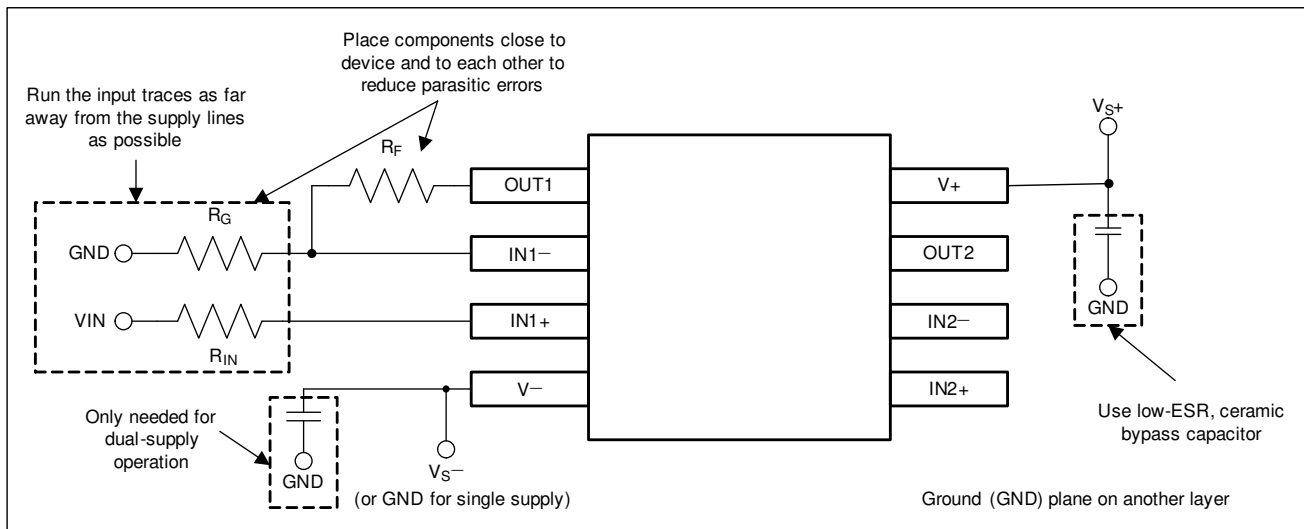


Figure 12-1. Operational Amplifier Board Layout for Noninverting Configuration

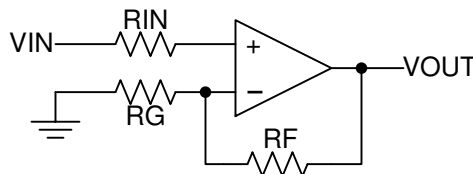


Figure 12-2. Operational Amplifier Schematic for Noninverting Configuration

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

Texas Instruments, [Application Design Guidelines for LM324/LM358 Devices application report](#)

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 13-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM2904-Q1	Click here	Click here	Click here	Click here	Click here
LM2904B-Q1	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

13.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2904AVQDRG4Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904AVQ	Samples
LM2904AVQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904AVQ	Samples
LM2904AVQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904AVQ	Samples
LM2904AVQPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904AVQ	Samples
LM2904BQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27ZB	Samples
LM2904BQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904BQ	Samples
LM2904BQPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904BQ	Samples
LM2904BTQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4BTQ	Samples
LM2904BTQDRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904TQ	Samples
LM2904BTQPWRQ1	ACTIVE	TSSOP	PW	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904BT	Samples
LM2904QDRG4Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	Samples
LM2904QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	Samples
LM2904QPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	Samples
LM2904QPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	Samples
LM2904VQDRG4Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904VQ	Samples
LM2904VQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904VQ1	Samples
LM2904VQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904VQ	Samples
LM2904VQPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904VQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LM2904-Q1, LM2904B-Q1 :

● Catalog : [LM2904](#), [LM2904B](#)

● Enhanced Product : [LM2904-EP](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

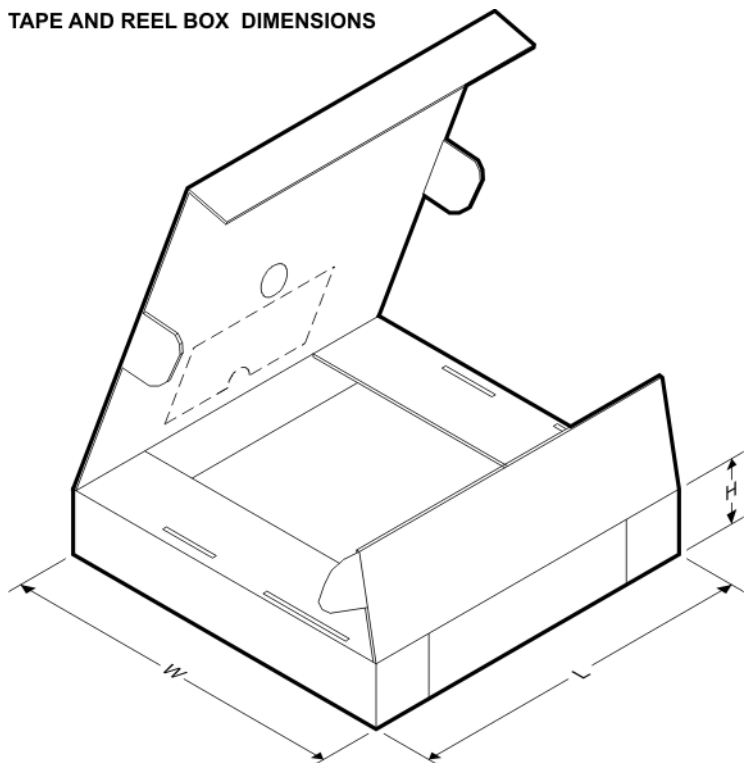
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2904AVQDRG4Q1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904AVQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904BQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904BQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904BQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904BTQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904BTQDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904BTQPWRQ1	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904QDRG4Q1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904QDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904QPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904VQDRG4Q1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904VQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2904AVQDRG4Q1	SOIC	D	8	2500	340.5	336.1	25.0
LM2904AVQDRQ1	SOIC	D	8	2500	340.5	336.1	25.0
LM2904AVQPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2904AVQPWRQ1	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2904BQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2904BQDRQ1	SOIC	D	8	2500	340.5	336.1	25.0
LM2904BQPWRQ1	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2904BTQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2904BTQDRQ1	SOIC	D	8	3000	340.5	338.1	20.6
LM2904BTQPWRQ1	TSSOP	PW	8	3000	853.0	449.0	35.0
LM2904QDRG4Q1	SOIC	D	8	2500	340.5	336.1	25.0
LM2904QDRQ1	SOIC	D	8	2500	340.5	336.1	25.0
LM2904QPWRG4Q1	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2904QPWRQ1	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2904VQDRG4Q1	SOIC	D	8	2500	340.5	336.1	25.0
LM2904VQDRQ1	SOIC	D	8	2500	340.5	336.1	25.0
LM2904VQPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2904VQPWRQ1	TSSOP	PW	8	2000	853.0	449.0	35.0



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

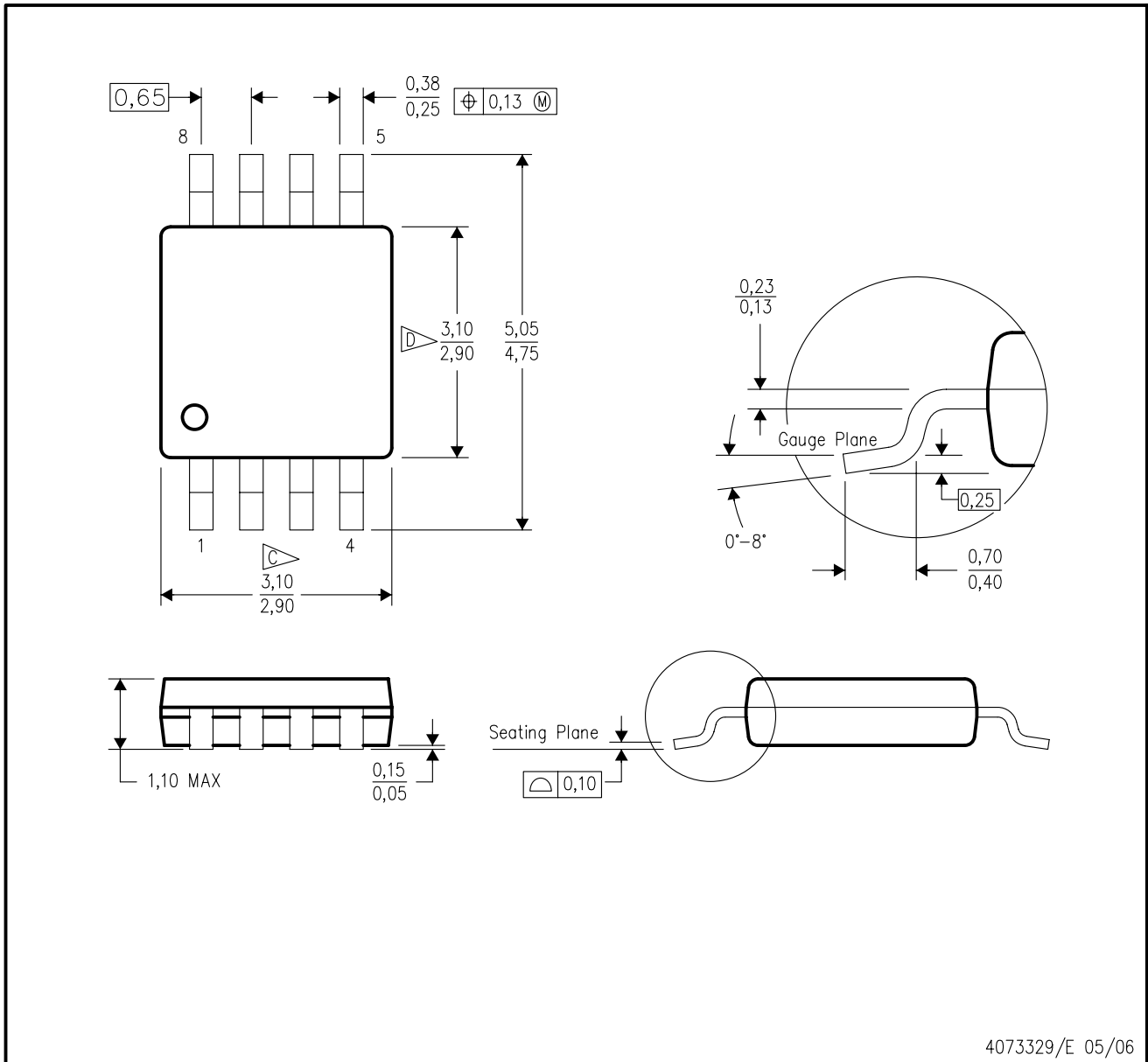
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



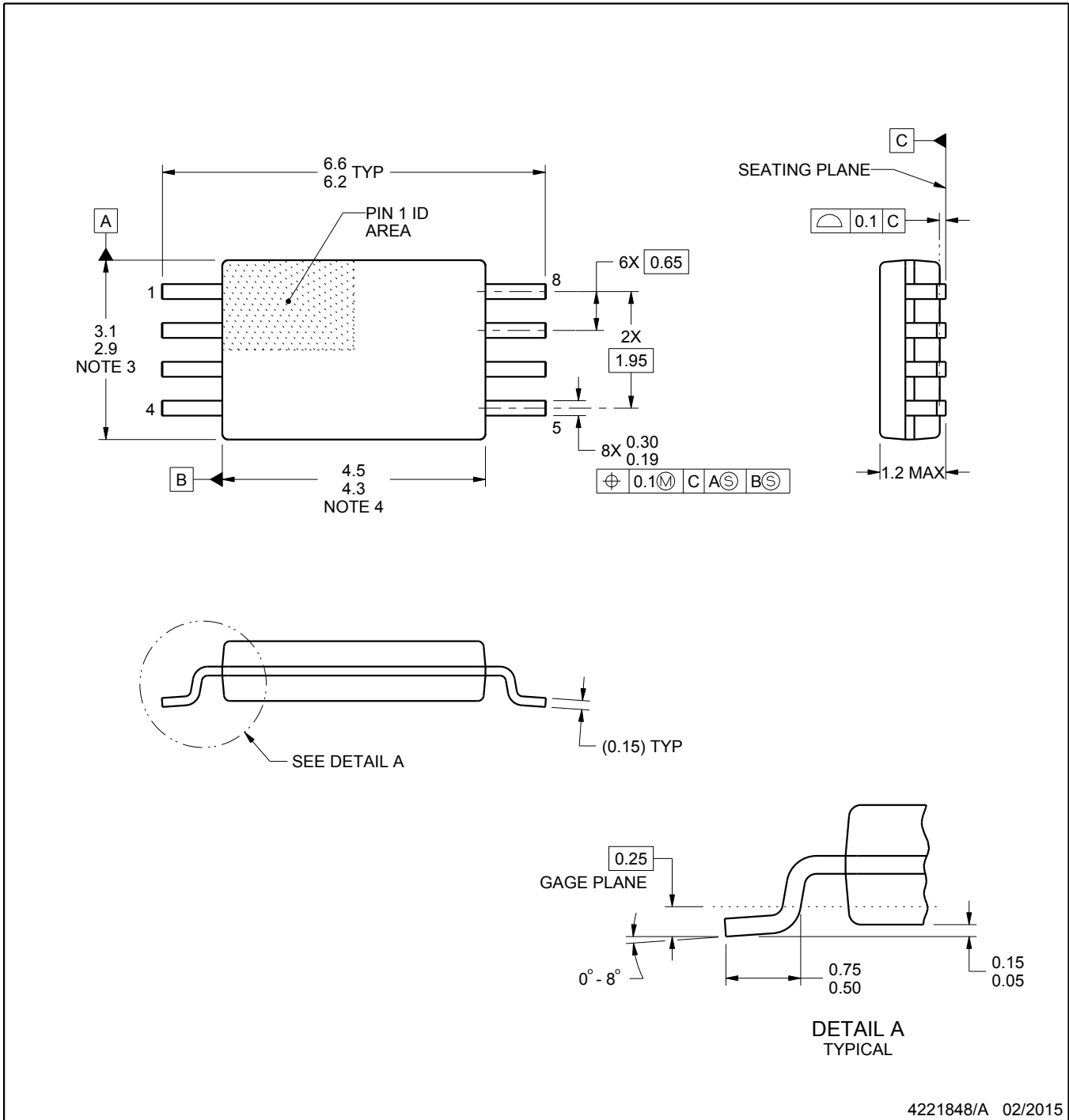
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW0008A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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