ACPL-W611/ACPL-P611

High CMR, High-Speed TTL Compatible Optocoupler

Data Sheet

Description

The ACPL-W611/ACPL-P611 is an optically coupled gate that combines a GaAsP light emitting diode and an integrated high gain photo detector. The output of the detector IC is an open collector Schottky clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 10,000 V/µs for the ACPL-W611.

This unique design provides maximum AC and DC circuit isolation while achieving TTL compatibility. The optocoupler AC and DC operational parameters are guaranteed from –40°C to +100°C, allowing trouble-free system performance.

The ACPL-W611/ACPL-P611 is suitable for high-speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

CAUTION It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

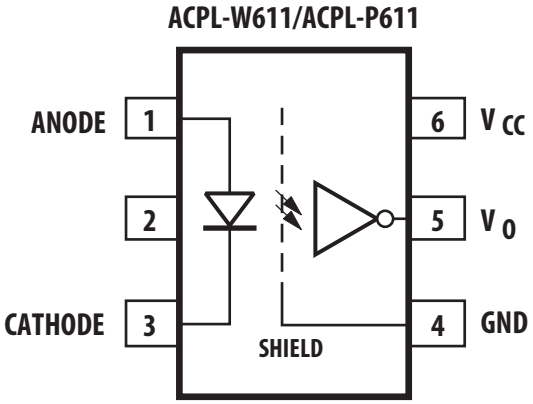
Features

- 10 kV/µs minimum Common Mode Rejection (CMR) at VCM = 1000V
- High speed: 10 MBd typical
- LSTTL/TTL compatible
- Low input current capability: 5 mA
- Guaranteed ac and dc performance over temperature: –40°C to +100°C
- Stretched SO-6 package
- Safety Approval:
  - UL Recognized: 5000Vrms for 1 minute for ACPL-W611 and ACPL-P611-020E per UL1577
  - CSA
  - IEC/EN/DIN EN 60747-5-5

Applications

- Isolated line receiver
- Computer-peripheral interfaces
- Microprocessor system interfaces
- Digital isolation for A/D, D/A conversion
- Switching power supply
- Instrument input/output isolation
- Ground loop elimination
- Pulse transformer replacement
- Power transistor isolation in motor drives
- Isolation of high speed logic systems

Functional Diagram

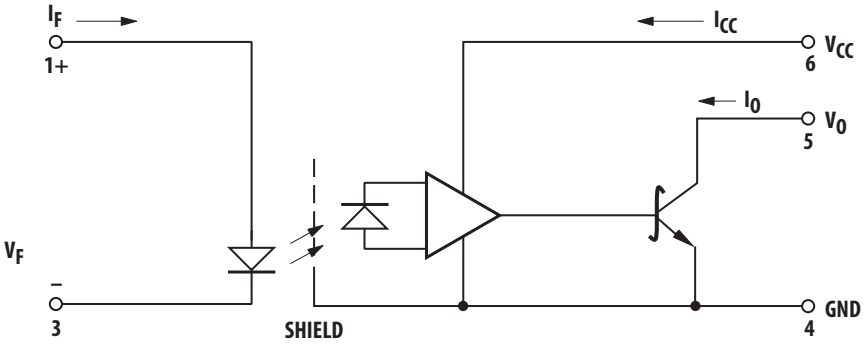


TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

NOTE Bypassing of the power supply line is required with a 0.-µF ceramic disc capacitor adjacent to each optocoupler. The total lead length between both ends of the capacitor and the isolator pins should not exceed 10 mm.

Schematic Diagram



Ordering Information

ACPL-P611 is UL Recognized with 3750 V_{rms} for 1 minute and ACPL-W611 is UL recognized with 5000 V_{rms} for 1 minute per UL1577. They are approved under CSA Component Acceptance Notice #5, File CA 88324.

Part Number	Option	Package	Surface Mount	Tape and Reel	UL 5000 Vrms/ 1 Minute Rating	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant						
ACPL-P611	-000E	Stretched SO-6	X				100 per tube
	-020E		X		X		100 per tube
	-060E		X			X	100 per tube
	-500E		X	X			1000 per reel
	-520E		X	X	X		1000 per reel
	-560E		X	X		X	1000 per reel
ACPL-W611	-000E	Stretched S0-6	X		X		100 per tube
	-060E		X		X	X	100 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry. Combination of Option 020 and Option 060 is not available.

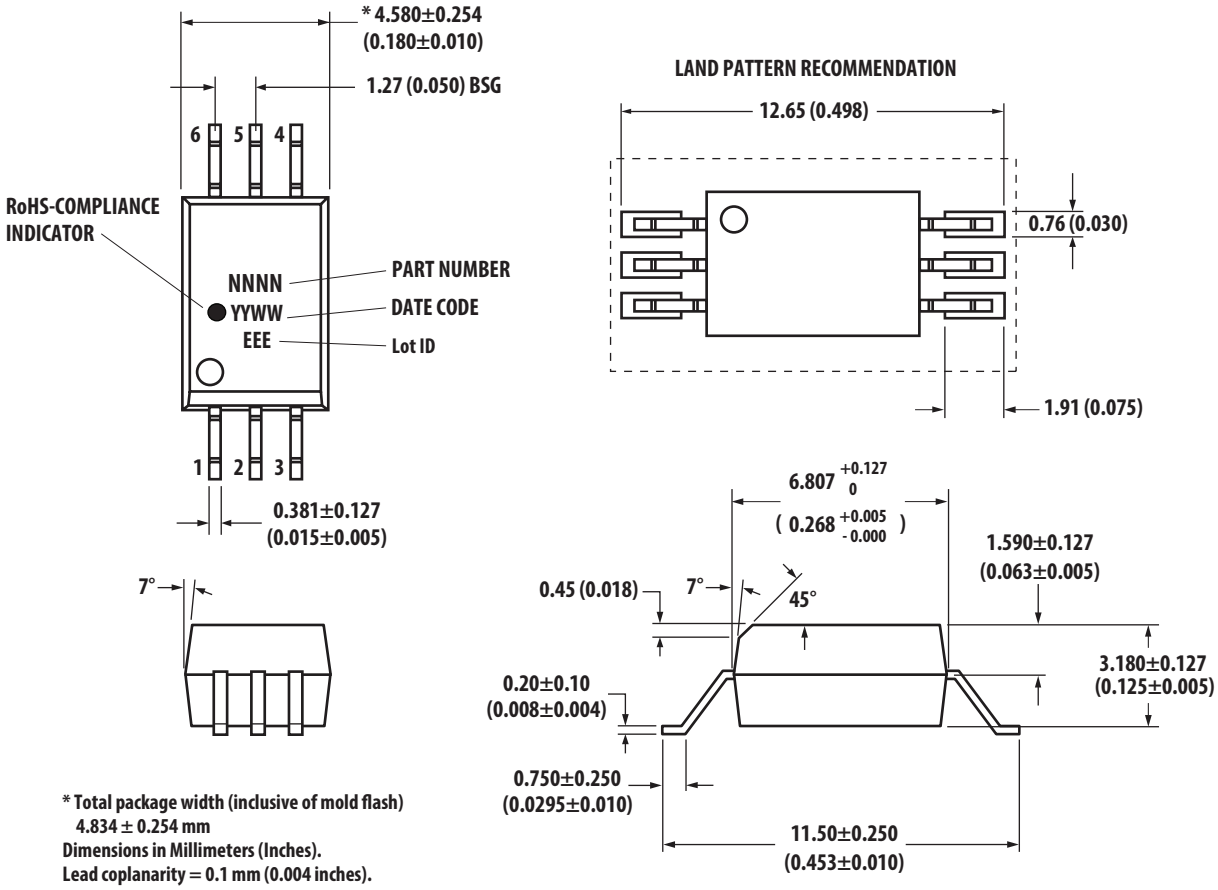
Example 1:

ACPL-P611-500E to order product of Surface Mount Stretched SO-6 package in Tape and Reel packaging with RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

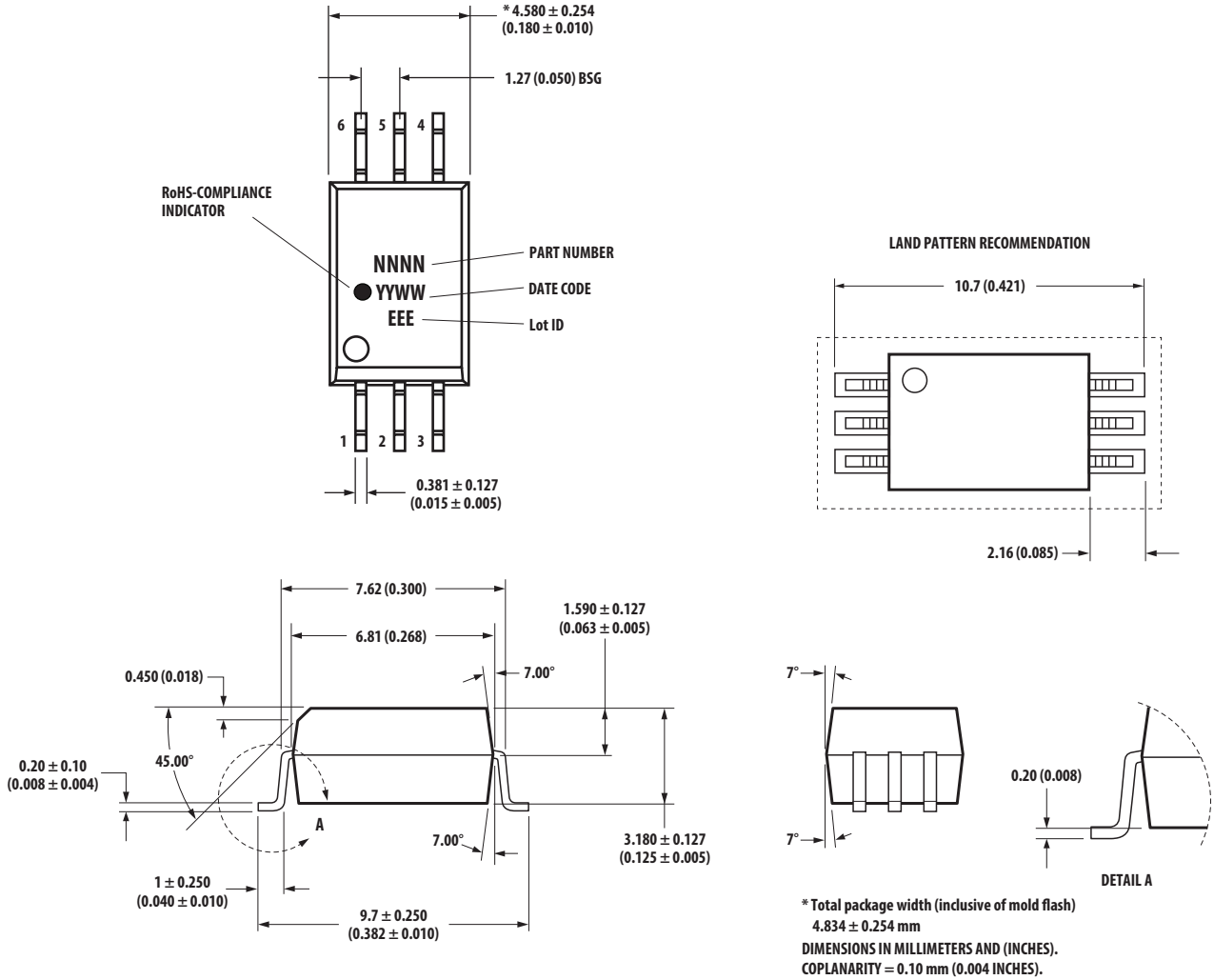
Package Outline Drawings

ACPL-W611 Stretched SO-6 Package



* Total package width (inclusive of mold flash)
  4.834 ± 0.254 mm
Dimensions in Millimeters (Inches).
Lead coplanarity = 0.1 mm (0.004 inches).

ACPL-P611 Stretched SO-6 Package



* Total package width (inclusive of mold flash)
4.834 ± 0.254 mm

DIMENSIONS IN MILLIMETERS AND (INCHES).
COPLANARITY = 0.10 mm (0.004 INCHES).

Reflow Soldering Profile

The recommended reflow soldering conditions are per JEDEC Standard J-STD-020 (latest revision). Non-halide flux should be used.

Regulatory Information

The ACPL-W611 and ACPL-P611 is approved/pending approval by the following organizations:

IEC/EN/DIN EN 60747-5-5 (Option 060 only)	Approval
UL	Approval under UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS}. File E55361.
CSA	Approval under CSA Component Acceptance Notice #5, File CA 88324.

Insulation and Safety-Related Specifications

Parameter	Symbol	ACPL-P611	ACPL-W611	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7	8	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	8	8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics (option x60, See Note [a])

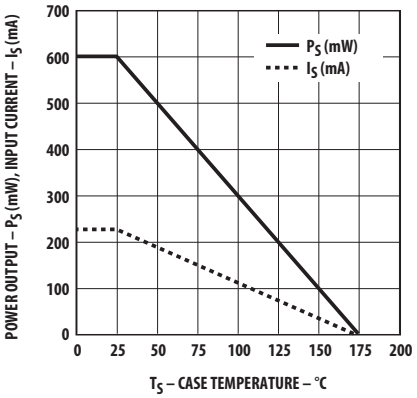
Description	Symbol	ACPL-P611	ACPL-W611	Units
Installation classification per DIN VDE 0110/39, Table 1				
for rated mains voltage ≤ 150 V_{rms}		I - IV	I - IV	
for rated mains voltage ≤ 300 V_{rms}		I - IV	I - IV	
for rated mains voltage ≤ 600 V_{rms}		I - III	I - III	
for rated mains voltage ≤ 1000 V_{rms}			I - III	
Climatic Classification		55/100/21	55/100/21	
Pollution Degree (DIN VDE 0110/39)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	891	1140	V_{peak}
Input to Output Test Voltage, Method b[a] $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m=1s, Partial discharge < 5 pC	V_{PR}	1671	2137	V_{peak}
Input to Output Test Voltage, Method a[a] $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, t_m=10s, Partial discharge < 5 pC	V_{PR}	1426	1824	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60s)	V_{IOTM}	6000	8000	V_{peak}
Safety-limiting values - maximum values allowed in the event of a failure.				
Case Temperature	T_S	175	175	°C
Input Current[b]	$I_{S, INPUT}$	230	230	mA
Output Power[b]	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	$>10^9$	$> 10^9$	Ω

a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.

b. Refer to Figure 1 for dependence of P_S and I_S on ambient temperature.

NOTE These optocouplers are suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Figure 1 Power Output vs. Case Temperature



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	–55	125	°C	
Operating Temperature	T_A	–40	100	°C	
Average Input Current	$I_{F(AVG)}$	—	20	mA	a
Reverse Input Voltage	V_R	—	5	V	
Input Power Dissipation	P_I	—	45	mW	
Supply Voltage (1 Minute Maximum)	V_{CC}	—	7	V	
Output Collector Current	I_O	—	50	mA	
Output Collector Voltage	V_O	—	7	V	
Output Collector Power Dissipation	P_O	—	85	mW	
Lead Solder Temperature	T_{LS}	—	260°C for 10s, 1.6 mm below seating plane		
Solder Reflow Temperature Profile	See Package Outline Drawings				

a. Peaking circuits may produce transient input currents up to 50 mA, 50-ns maximum pulse width, provided average current does not exceed 20 mA.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}	0	250	µA
Input Current, High Level	I_{FH}	5	15	mA
Power Supply Voltage	V_{CC}	4.5	5.5	V
Operating Temperature	T_A	–40	100	°C
Fan Out (at R_L = 1 kΩ)	N	—	5	TTL Loads
Output Pull-up Resistor	R_L	330	4k	Ω

Electrical Specifications (DC)

Over recommended operating conditions unless otherwise specified. All typicals at V_{CC} = 5V, T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}	—	5.5	100	µA	V_{CC} = 5.5V, V_O = 5.5V, I_F = 250 µA	2	
Input Threshold Current	I_{TH}	—	2.0	5.0	mA	V_{CC} = 5.5V, V_O = 0.6V, I_{OL} > 13 mA	14	
Low Level Output Voltage	V_{OL}	—	0.35	0.6	V	V_{CC} = 5.5V, I_F = 5 mA, $I_{OL(Sinking)}$ = 13 mA	3, 5, 6, 14	
High Level Supply Current	I_{CCH}	—	4	7.5	mA	V_{CC} = 5.5V, I_F = 0 mA,		
Low Level Supply Current	I_{CCL}	—	6	10.5	mA	V_{CC} = 5.5V, I_F = 10 mA,		
Input Forward Voltage	V_F	1.4	1.5	1.75	V	T_A = 25°C, I_F = 10 mA	4	
		1.3	—	1.8				
Input Reverse Breakdown Voltage	BV_R	5	—	—	V	I_R = 10 µA		
Input Capacitance	C_{IN}	—	60	—	pF	f = 1 MHz, V_F = 0V		
Input Diode Temperature	$\Delta V_F/\Delta T_A$	—	–1.6	—	mV/°C	I_F = 10 mA	13	

Switching Specifications (AC)

Over recommended operating conditions T_A = –40°C to 100°C, V_{CC} = 5V, I_F = 7.5 mA unless otherwise specified.

All typicals at V_{CC} = 5V, T_A = 25 °C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}	20	48	75	ns	T_A = 25°C, R_L = 350Ω, C_L = 15 pF		a
		—	—	100		R_L = 350Ω, C_L = 15 pF		
Propagation Delay Time to Low Output Level	t_{PHL}	25	50	75	ns	T_A = 25°C, R_L = 350Ω, C_L = 15 pF		b
		—	—	100		R_L = 350Ω, C_L = 15 pF		
Pulse Width Distortion	$\lvert t_{PHL} - t_{PLH} \rvert$	—	3.5	35	ns	R_L = 350Ω, C_L = 15 pF		c
Propagation Delay Skew	t_{PSK}	—	—	40	ns			c, d
Output Rise Time (10%–90%)	t_R	—	24	—	ns			
Output Fall Time (10%–90%)	t_F	—	10	—	ns			
Output High Level Common Mode Transient Immunity	$\lvert CM_H \rvert$	10	15	—	kV/µs	V_{CC} = 5V, I_F = 0 mA, $V_{O(MIN)}$ = 2V, R_L = 350Ω, T_A = 25°C, V_{CM} = 1000V	8, 10	e
Output Low Level Common Mode Transient Immunity	$\lvert CM_L \rvert$	10	15	—	kV/µs	V_{CC} = 5V, I_F = 7.5 mA, $V_{O(MAX)}$ = 0.8V, R_L = 350Ω, T_A = 25°C, V_{CM} = 1000V		f, g

a. The t_{PLH} propagation delay is measured from 3.75 mA point on the falling edge of the input pulse to the 1.5-V point on the rising edge of the output pulse.

b. The t_{PHL} propagation delay is measured from 3.75 mA point on the rising edge of the input pulse to the 1.5-V point on the falling edge of the output pulse.

c. See the application section, "Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew," for more information.

d. t_{PSK} is equal to the worst case differ-ence in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the worst case operating condition range.

e. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (that is, V_{OUT} > 2.0V).

f. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (that is, V_{OUT} > 0.8V).

g. For sinusoidal voltages, $(|dV_{CM}|/dt)_{max} = \pi f_{CM} V_{CM(p\text{-}p)}$.

Package Characteristics

All typicals at $T_A = 25°C$.

Parameter	Symbol	Device	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Input-Output Insulation	V_{ISO}	ACPL-P611	3750	—	—	Vrms	RH < 50% for 1 min., $T_A = 25°C$		a, b, c
		ACPL-W611	5000						
Input-Output Resistance	R_{I-O}		—	10^{12}	—	Ω	$V_{I-O} = 500V$		a
Input-Output Capacitance	C_{I-O}		—	0.6	—	pF	f = 1 MHz, $T_A = 25°C$		a

a. The device considered a two terminal device: pins 1, 2, and 3 shorted together, and pins 4, 5, and 6 shorted together.

b. In accordance with UL 1577, for $V_{ISO} = 3750\ V_{rms}$, each optocoupler is proof-tested by applying an insulation test voltage ≥ 4500 V_{RMS} for 1 second (leakage detection current limit, $I_{I-O} \leq 5\ \mu A$). For V_{ISO} 5000 $_{Vrms}$, each optocoupler is proof-tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second (leakage detection current limit, $I_{I-O} \leq 5\ \mu A$).

c. ACPL- P611 (non -020E, -520E option) is UL Recognized 3750 V_{rms}. The -020E and -520E option is Recognized 5000 V_{rms}.

Figure 2 High Level Output Current vs. Temperature

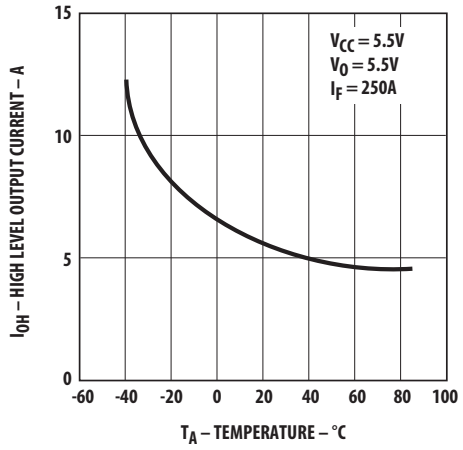


Figure 3 Low Level Output Voltage vs. Temperature

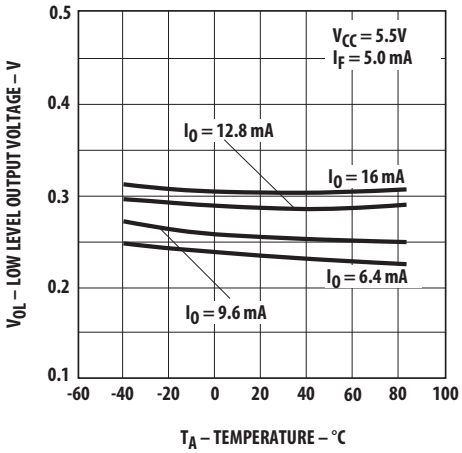


Figure 4 Input Diode Forward Characteristic

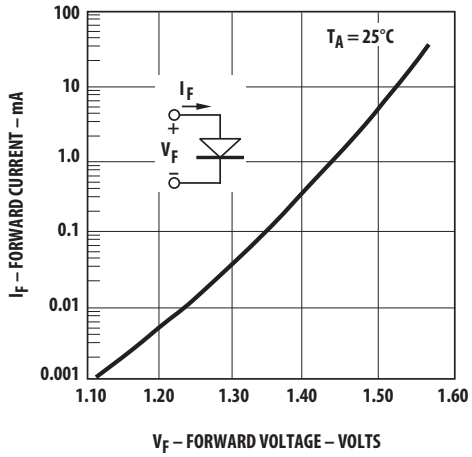


Figure 5 Output Voltage vs. Forward Input Current

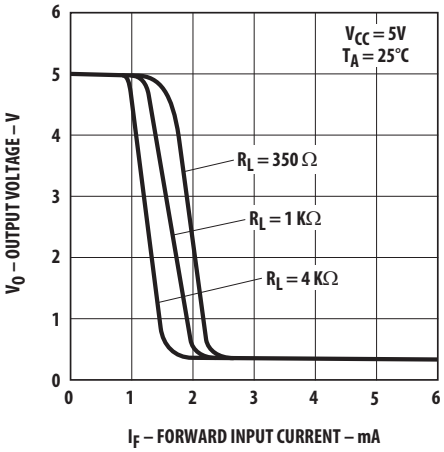


Figure 6 Low Level Output Current vs. Temperature

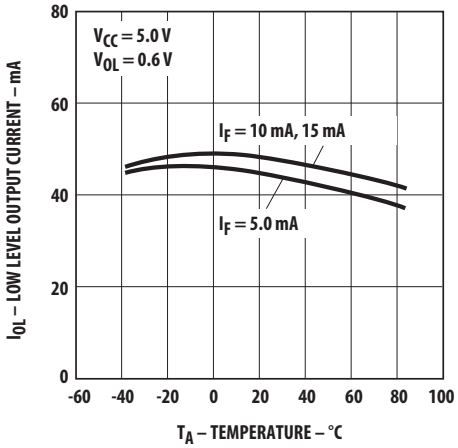
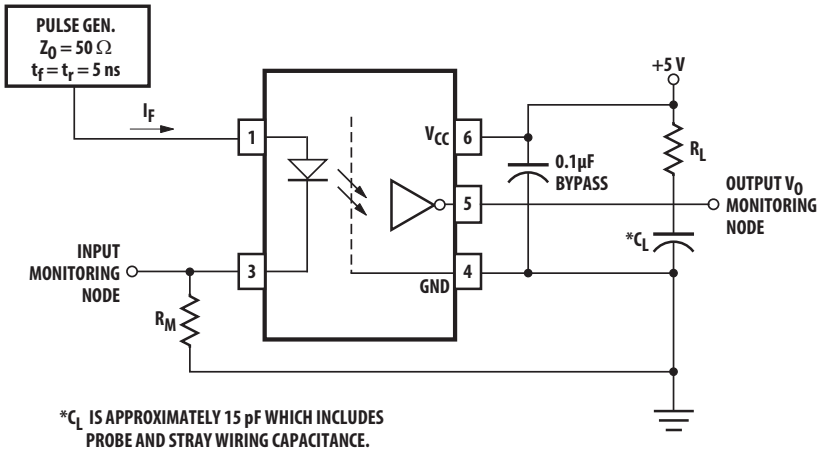


Figure 7 Test Circuit for t_{PHL} and t_{PLH}



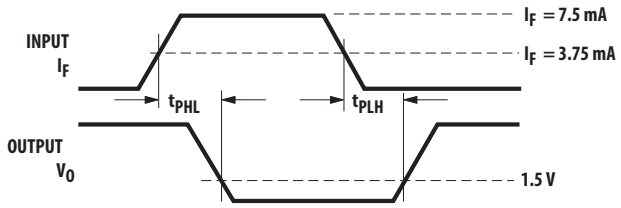


Figure 8 Propagation Delay vs. Temperature

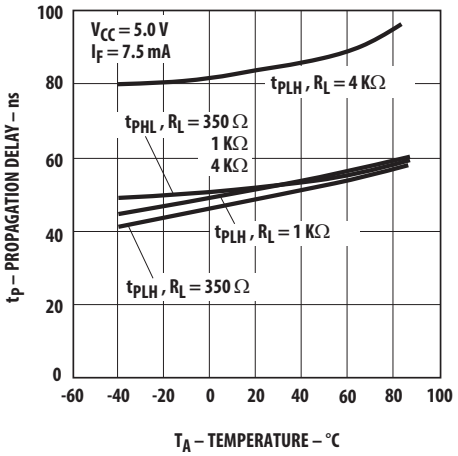


Figure 9 Propagation Delay vs. Pulse Input Current

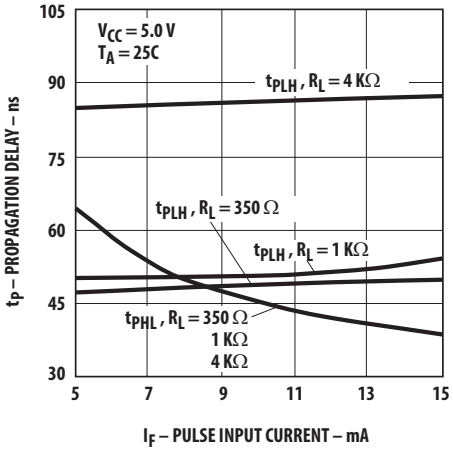


Figure 10 Pulse Width Distortion vs. Temperature

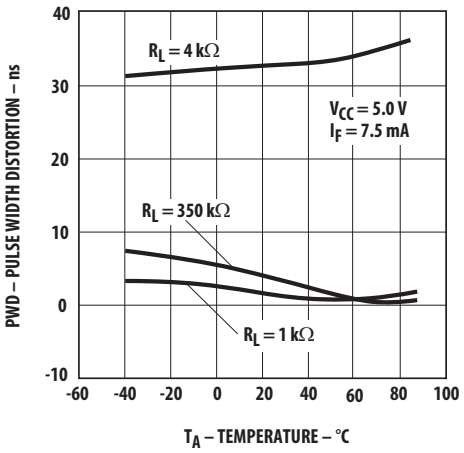


Figure 11 Rise and Fall Time vs. Temperature

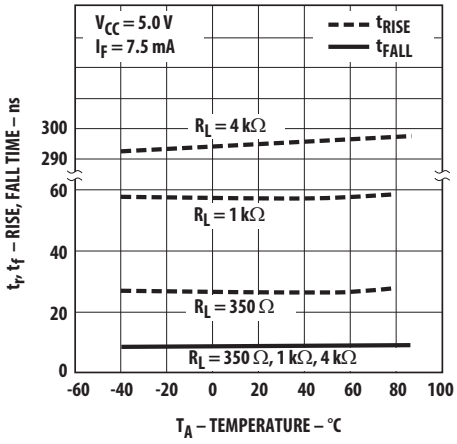


Figure 12 Test Circuit for Common Mode Transient Immunity and Typical Waveforms

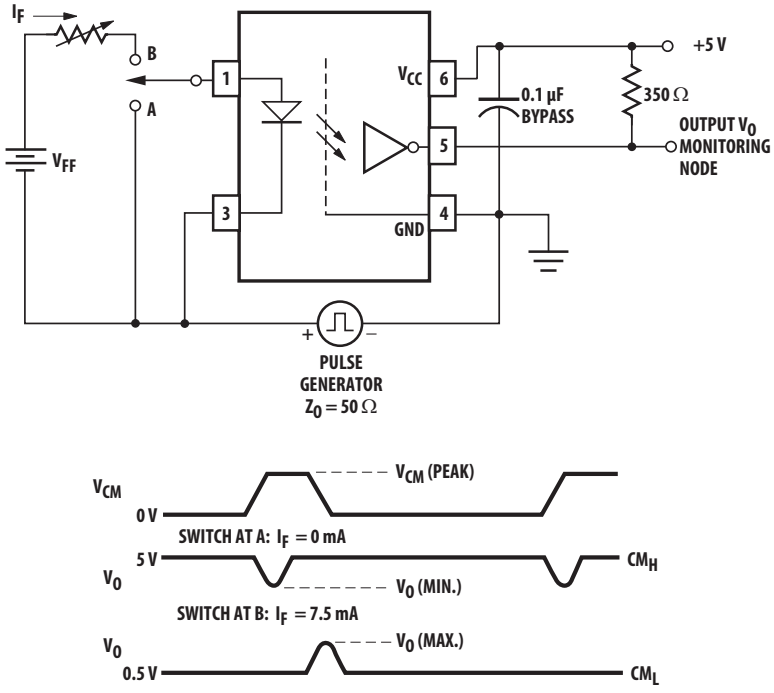


Figure 13 Temperature Coefficient for Forward Voltage vs. Input Current

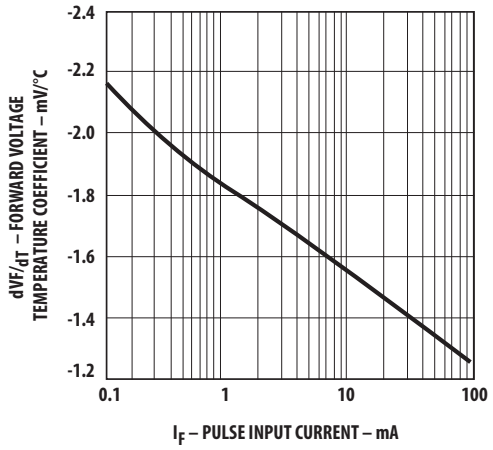
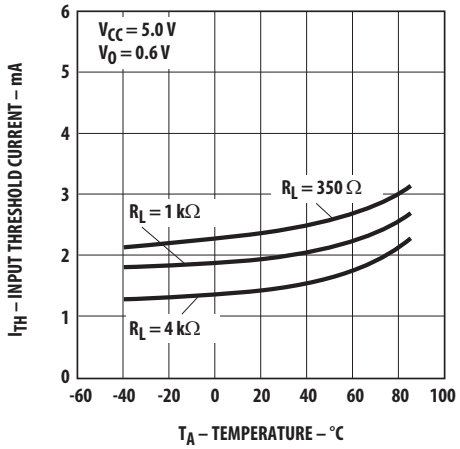


Figure 14 Input Threshold Current vs. Temperature



For product information and a complete list of distributors, please go to our web site: www.broadcom.com.

AV02-0942EN – May 11, 2017

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product