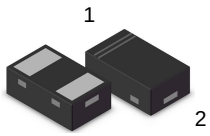
Leiditech

ULC0511DN

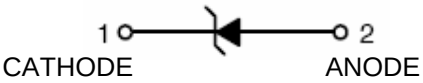
Features

- Ultra low leakage: nA level
- Operating voltage: 5V
- Low clamping voltage
- Complies with following standards:
  – IEC 61000-4-2 (ESD) immunity test
    Air discharge: ±15kV
    Contact discharge: ±10kV
- RoHS Compliant

Dimensions SOD-882



Pin Configuration



Applications

- USB 2.0 power and data line
- Set-top box and digital TV
- Digital video interface (DVI)
- Notebook Computers
- SIM Ports
- 10/100 Ethernet

Mechanical Characteristics

- Package: SOD-882
- Lead Finish: Lead Free
- UL Flammability Classification Rating 94V-0
- Quantity Per Reel:1000pcs

Absolute Maximum Ratings(Tamb=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20μs)	Ppp		W
ESD per IEC 61000−4−2 (Air)	V_{ESD}	±15	Kv
ESD per IEC 61000−4−2 (Contact)		±10	
Operating Temperature Range	T_J	-55 to +125	℃
Storage Temperature Range	T_{STJ}	-55 to +150	℃

Electrical Characteristics(TA=25°C unless otherwise specified)

Part Number	Device Marking	V_{RWM} (V)	V_{BR} (V)	I_T (mA)	V_C @1A	Vc		I_R μA (Max)	C (Pf) (Typ.)
						(Max)	(@A)		
ULC0511DN	D	5	5.4	1	9.8			1	0.5

Characteristic Curves

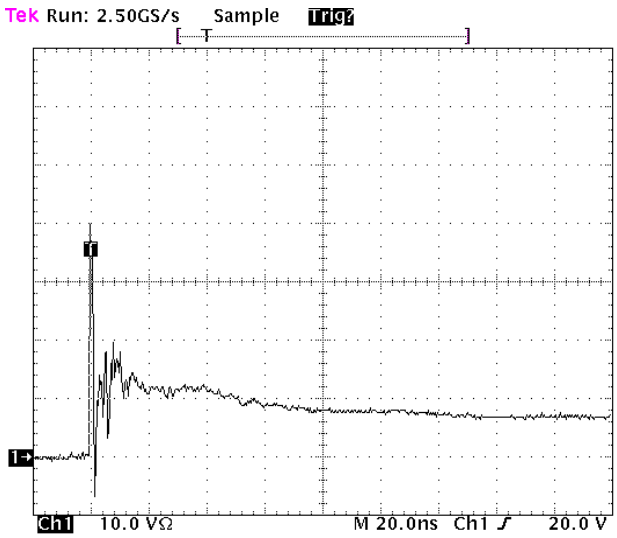


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

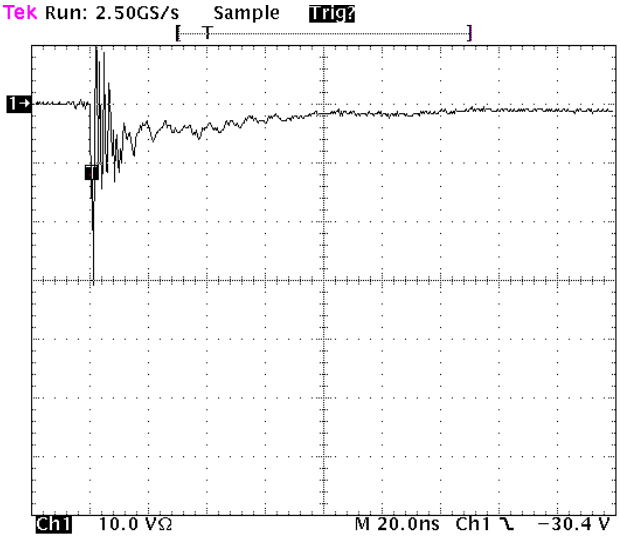


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

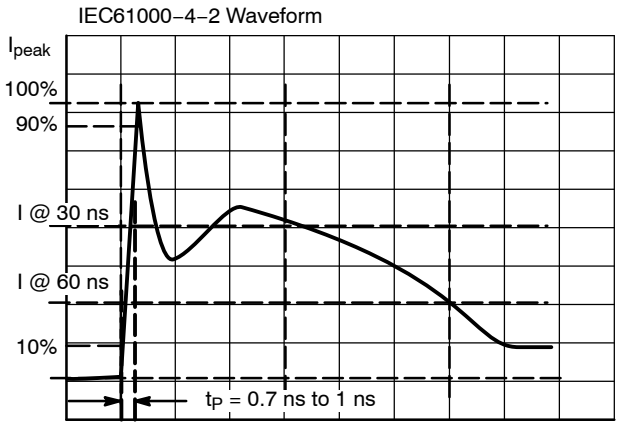


Figure 3. IEC61000−4−2 Spec

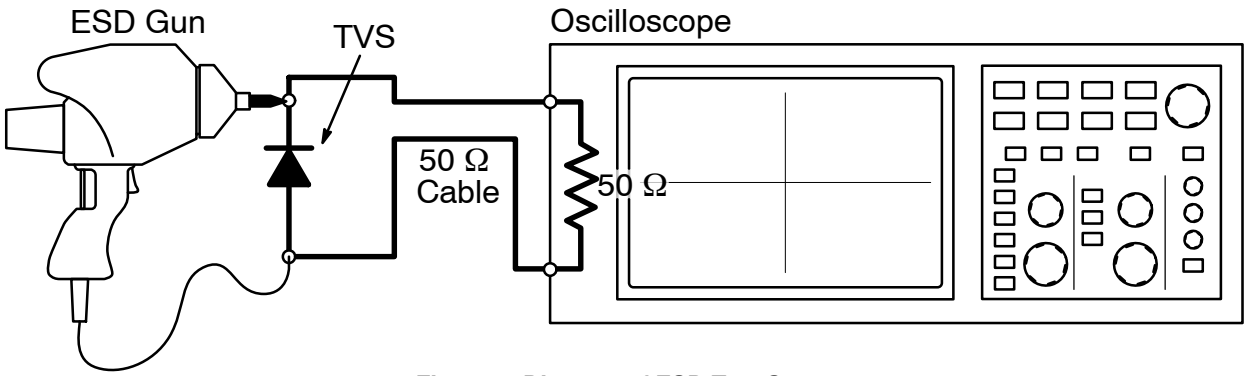


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

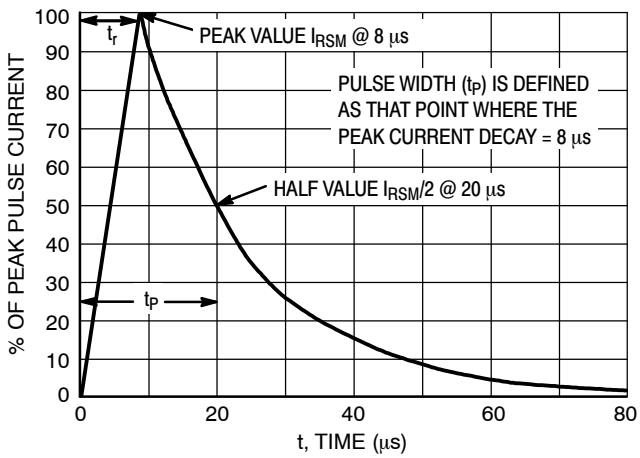
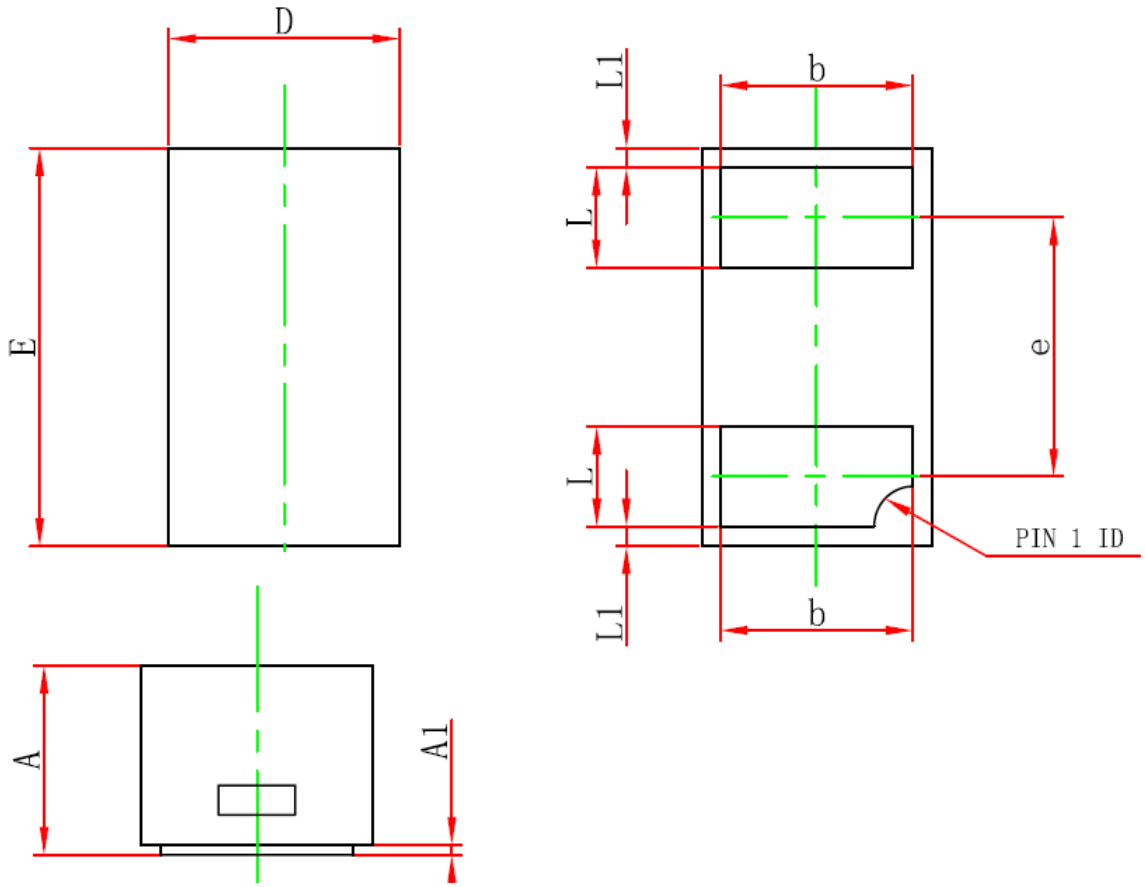


Figure 5. 8 X 20 μs Pulse Waveform

SOD882 Package Outline Drawing



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.400	0.500	0.016	0.020
A1	0.000	0.050	0.000	0.002
D	0.550	0.650	0.022	0.026
E	0.950	1.050	0.037	0.041
b	0.400	0.600	0.016	0.024
e	0.650TYP.		0.026TYP.	
L	0.150	0.350	0.006	0.014
L1	0.050REF.		0.002REF.	

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