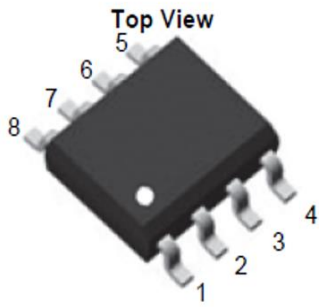
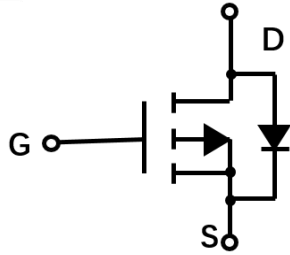
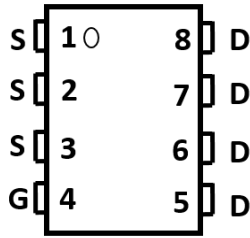


## P-Channel Enhancement Mode Field Effect Transistor



**SOP-8**



### Product Summary

- $V_{DS}$  -30V
- $I_D$  -12A
- $R_{DS(ON)}$  ( at  $V_{GS}=-20V$ ) < 10.5mohm
- $R_{DS(ON)}$  ( at  $V_{GS}=-10V$ ) < 12.5mohm
- $R_{DS(ON)}$  ( at  $V_{GS}=-4.5V$ ) < 20.8mohm

### General Description

- Trench Power LV MOSFET technology
- High density cell design for Low  $R_{DS(ON)}$
- High Speed switching

### Applications

- Battery protection
- Power management
- Load switch

### ■ Absolute Maximum Ratings ( $T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	$V_{DS}$	-30	V
Gate-source Voltage	$V_{GS}$	$\pm 25$	V
Drain Current	$I_D$	$T_A=25^{\circ}C$ @ Steady State	-12
		$T_A=70^{\circ}C$ @ Steady State	-10
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	-55	A
Single Pulse Avalanche Energy <sup>B</sup>	$E_{AS}$	105	mJ
Total Power Dissipation @ $T_A=25^{\circ}C$ <sup>C</sup>	$P_D$	3.2	W
Thermal Resistance Junction-to-Ambient @ Steady State <sup>D</sup>	$R_{\theta JA}$	39	$^{\circ}C/W$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^{\circ}C$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJS4407A	F2	Q4407B.	4000	8000	64000	13" reel



# YJS4407A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V, T <sub>C</sub> =25°C			-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±25V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.2	-1.8	-2.8	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -20V, I <sub>D</sub> =-12A		9.0	10.5	mΩ
		V <sub>GS</sub> = -10V, I <sub>D</sub> =-12A		9.3	12.5	
		V <sub>GS</sub> = -6.0V, I <sub>D</sub> =-10A		12.3	16.5	
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> =-10A		13.8	20.8	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-12A, V <sub>GS</sub> =0V		-0.8	-1.2	V
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHZ		2152		pF
Output Capacitance	C <sub>oss</sub>			308		
Reverse Transfer Capacitance	C <sub>rss</sub>			242		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = -10V, V <sub>DS</sub> = -15V, I <sub>D</sub> = -12A		40.1		nC
Gate Source Charge	Q <sub>gs</sub>			8.4		
Gate Drain Charge	Q <sub>gd</sub>			8.6		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = -12A, di/dt= 100A/us		7.8		
Reverse Recovery Time	t <sub>rr</sub>			18		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> = -10V, V <sub>DD</sub> = -15V, I <sub>D</sub> = -1A, R <sub>GEN</sub> = 2.5Ω		8		ns
Turn-on Rise Time	t <sub>r</sub>			19		
Turn-off Delay Time	t <sub>D(off)</sub>			75		
Turn-off Fall Time	t <sub>f</sub>			46		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R<sub>θJA</sub> is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJL</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

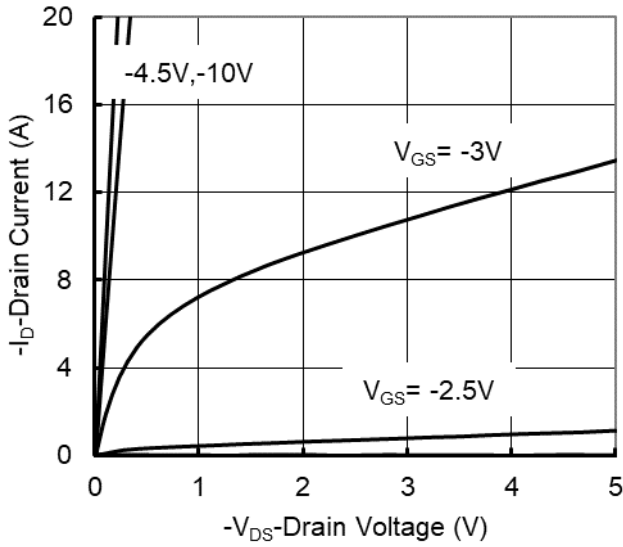


Figure 1. Output Characteristics

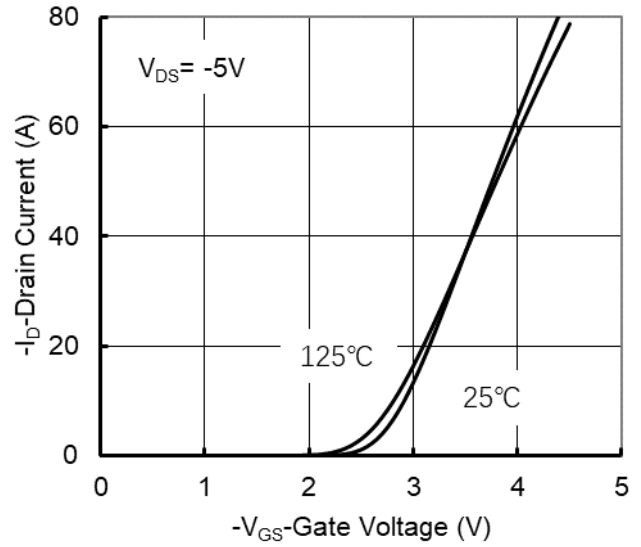


Figure 2. Transfer Characteristics

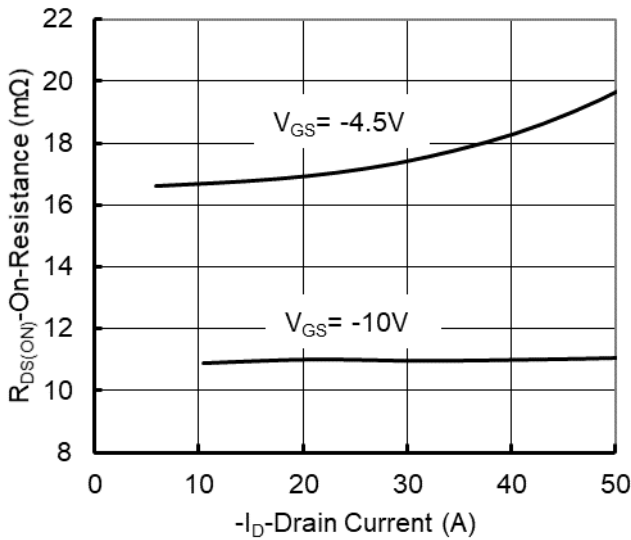


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

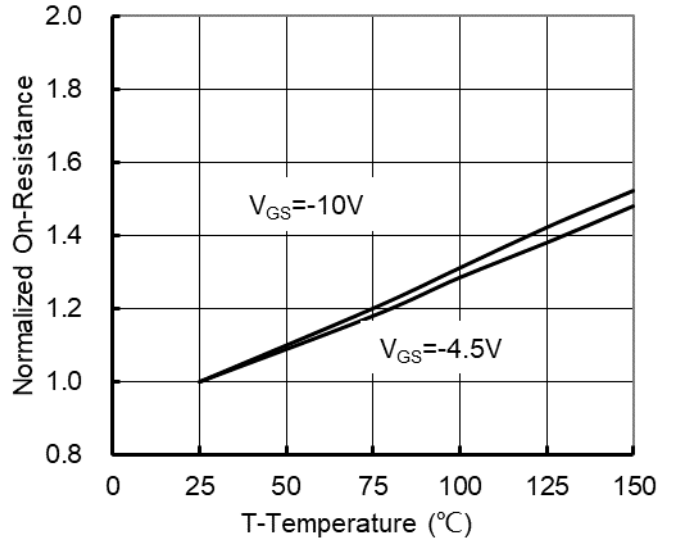


Figure 4. On-Resistance vs. Junction Temperature

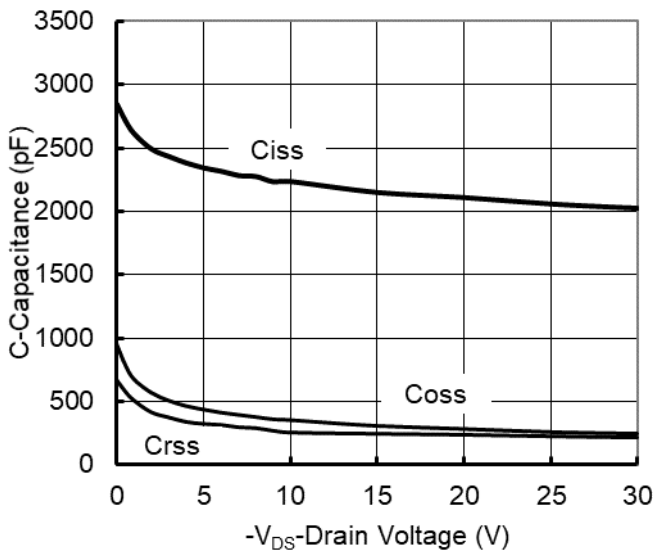


Figure 5. Capacitance Characteristics

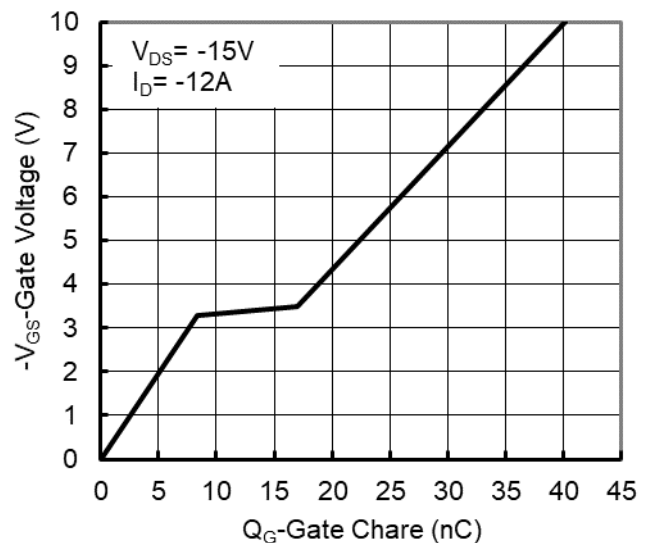


Figure 6. Gate Charge

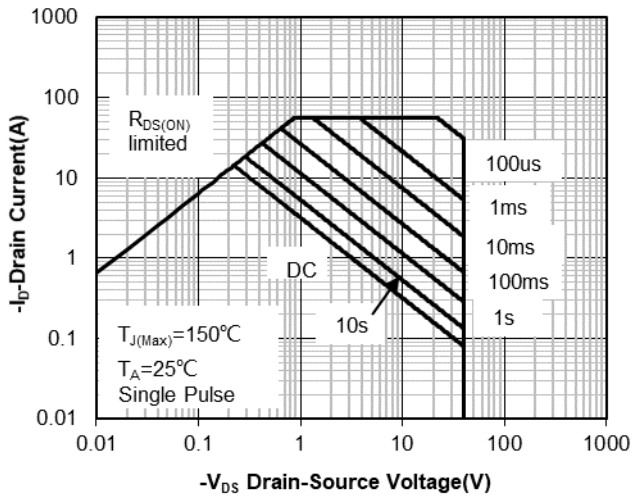


Figure 7. Safe Operation Area

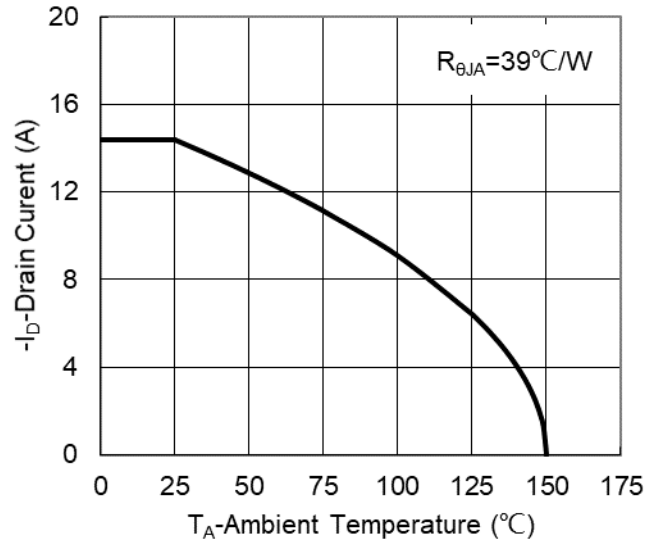


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

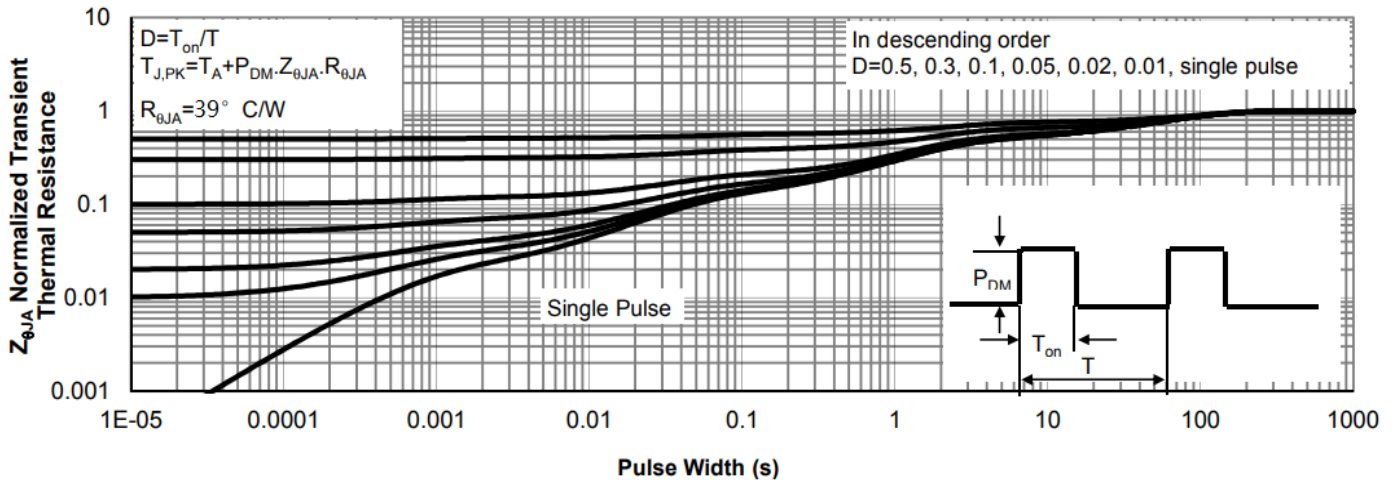
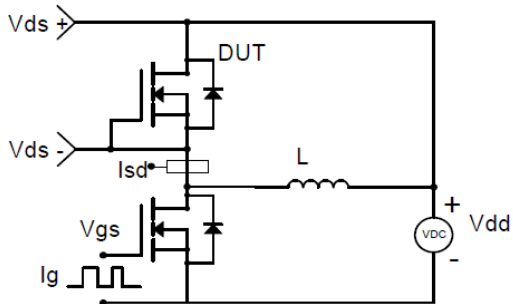


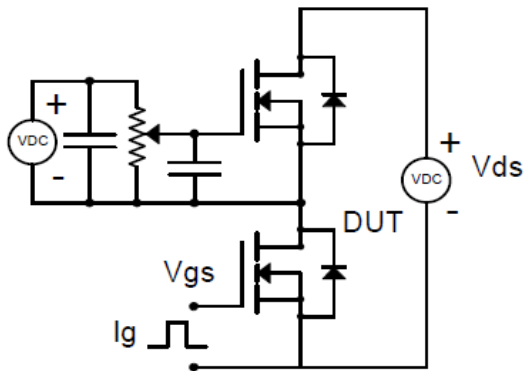
Figure 9. Normalized Maximum Transient Thermal Impedance



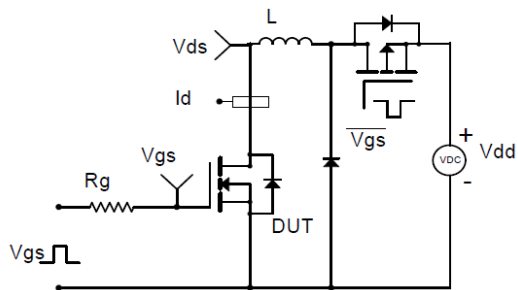
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

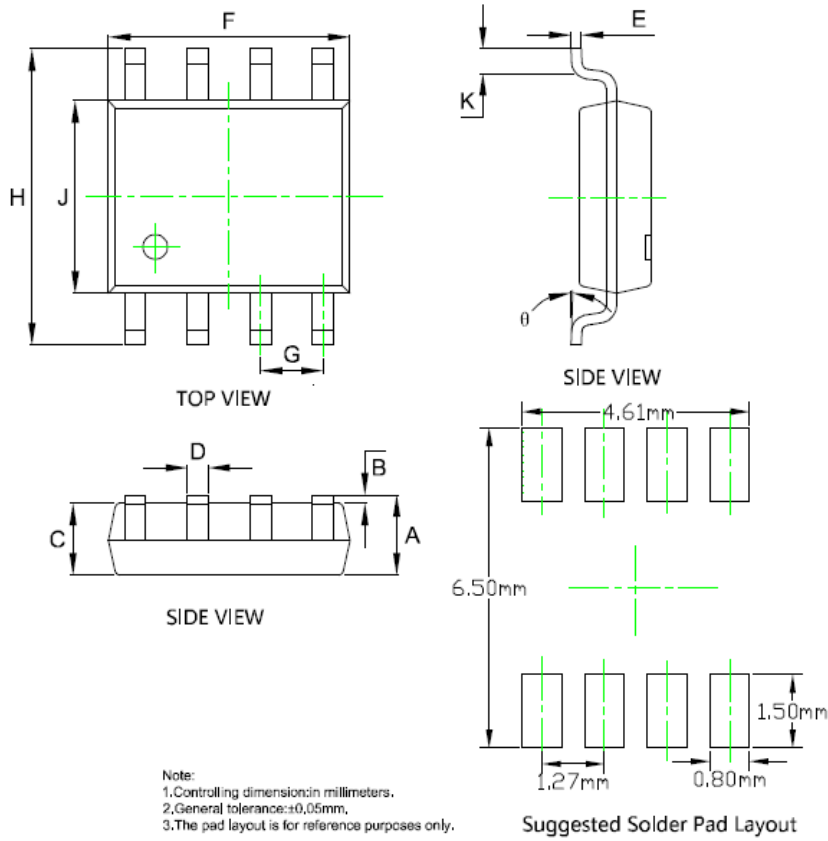


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



# YJS4407A

## ■ SOP-8 Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
$\theta$	0°	8°	0°	8°



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